

EEPROM Memory: Threshold Voltage Built In Self Diagnosis

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Abstract

Knowing, that the threshold voltage of the EEPROM memory cells is a key parameter to determine the overall performance of the memory, a built in structure to extract this information is a very relevant choice to fast diagnose failure in the memory. Thus, the objective of this paper is to present a built in self-diagnosis of EEPROM memory cells, based on threshold voltage extraction. In order to extract the threshold voltage, the modified circuit and the associated test sequence are presented. Based on the threshold voltage extraction, complementary information is proposed to improve the classical memory diagnosis methodology.

1. Introduction

The evolution of the market of portable devices such as smart card or mobile communication media has a straight impact on the use of EEPROM. Indeed, EEPROM have become over the last few years' very relevant choices for any application requiring non-volatile semiconductor memory. The core element of the EEPROM memory cell is a *Floating Gate Transistor (FGT)*. The threshold voltage of a *FGT* can be shifted repetitively from a high to a low state corresponding to the two logical values of the memory cell. The V_T of a *FGT* is shifted when the cell is programmed by a write or erase operation. When a negative charge is stored on the floating gate node, the V_T increases, the cell is then said erased. Respectively, when the charge on the floating gate node is positive, the V_T decreases, the cell is then said written. In the EEPROM industry-standard "Flotox", the charge transfer from the drain node to the floating gate node is due to Fowler-Nordheim tunneling [1]. This tunneling mechanism is completely dependant of factors like, the geometry of the cell [2], the high voltage applied to program the cell and the fabrication process quality.

All this element lead to critical problems of design and process control in the Non Volatile Memory field. Any small variations of any of this factors, among the cells in a memory array, lead directly to a spread threshold voltage distribution, limiting the overall performance of the memory and impacting the yield. Knowing that, yield improvement is a key factor to determine the success of a fabrication unit, product specific as well as general speed up techniques for diagnosis are absolutely necessary. In the case of EEPROM memory, it clearly appears that the knowledge of the threshold voltage of all the cells in a memory array is a key point to be able to develop accurate diagnosis methodology. From these facts and knowing that memories offers specific properties of regularity, failure analysis methods were proposed. AFA in [3] from D.Y.Lepejian focuses on repeated structure and is linked to an IFA program CARAFE [4]. Other methods used to enhance yield are based on digital memory bitmap, as the ones proposed in [5] by J.Segal. Those methods have a general scope and so can be used successfully with Non Volatile Memory, but they do not address the specific analog memorization mechanism, i.e. threshold voltage shifting, of the EEPROM. The fundamental discussion of this paper is to present an EEPROM dedicated diagnosis methodology. This methodology is based on a built in threshold voltage extraction features and its associated test sequence. Using this additional features, the extraction on product of the threshold voltages of all the memory cells can be rapidly and accurately achieved. The classical diagnosis methodology is then modified to take into account the threshold voltages values. The paper is organized as follows. Section 2 gives an overview, of the EEPROM memory array structure and of the functional test sequence. In section 3, the additional circuit used to extract threshold voltages is described with the modified read sequence. The section 4 is dedicated to the diagnosis method improvement based on analog bitmapping. Finally, Section 5 gives some concluding remarks.

2. EEPROM overview

The EEPROM architecture is globally similar to conventional RAM and consists in an array of memory cells identified by their row and column position. This array is classically surrounded by the following elements:

- A control logic and registers.
- A row decoder to select the active row.
- A bit line decoder for the active column.
- High voltage latches to store the data to program in the memory words.
- A sense amplifier for the read operation.

However the EEPROM architecture exhibits also some specificity directly due to the program process. To perform data storing operation, the EEPROM structure includes on chip a high voltage generator such as a charge pump. The Figure 1 summarizes the global architecture of an EEPROM memory.

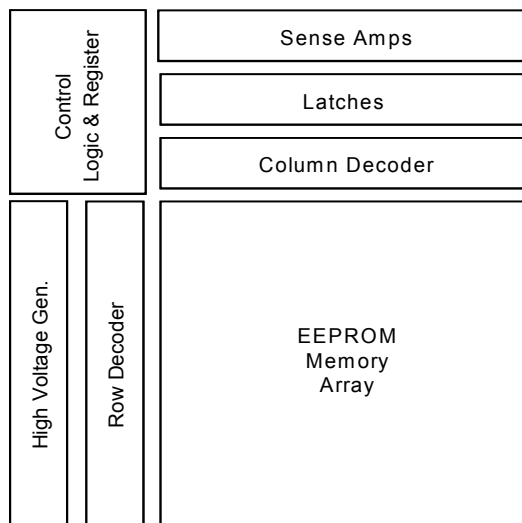
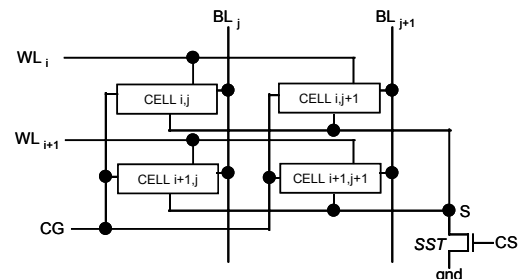


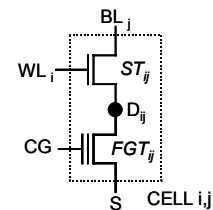
Figure 1: Overview of the EEPROM structure

Typically, the array of memory cells can be organized as NOR or NAND. In our case, the NOR organization is considered and illustrated in Figure 2.a. Depending on the array organization, different procedures are used to store data. The procedure taken into account here, consists in erasing the word that includes the bits to change and then in rewriting with the new information. In such a procedure, only a write operation can be performed bit by bit. The cell is composed of two transistor a select transistor and a sense transistor, as illustrated Figure 2.b. The core element of the EEPROM memory cell is the sense transistor, which is a Floating Gate Transistor (FGT). The threshold voltage of a FGT can be changed repetitively from a high to a low state corresponding to the two logical values of the memory cell. The V_T of a FGT is changed when the cell is **programmed** by a **write** or **erase** operation. When a negative charge is stored on the floating gate, the V_T increases, the cell is then said **erased** and its logical value

equals "1". Respectively, when the charge on the floating gate is positive, the V_T decreases, the cell is then said **written** and stores a logical "0". In order to program a cell a high voltage V_{PP} is applied on the bit line node (BL_i) of the cell for a write operation and on the control gate node (CG) for an erase operation. To perform a read operation, a given potential $V_{C_{gref}}$ is applied on the control gate of the selected cell and a read current I_{read} is applied on the bit line by the sense amplifier. On one hand, when the cell is written the current I_{read} flows through the cell and the sense amplifier switch, on the other hand when the cell is erased the FGT does not conduct so the current does not pass through the cell and no switch occurred on the output of the sense amplifier.



a. Array structure



b. Cell structure

Figure 2: Memory array and cell structure

The EEPROM functional test flow has to face more critical constraints than those of conventional RAM. Indeed, the program operation is too much time consuming to use test algorithm that are base on write, erase sequence, such as the March test. So simple test sequence [6] are preferentially used like:

- All '1', all '0'.
- Checkerboard.
- Row bar and column bar.
- Diagonal etc...

All this simple test algorithm only necessitate one erase/write operation followed by a read operation. Moreover it is important to note that the read time represents less than 0.1% of the program time. In term of diagnosis, a logical bitmapping is performed on each of this test algorithm. To summarize, the EEPROM exhibits an analog mechanism of memorization by threshold voltage shifting but are tested in using simple classical RAM test algorithm and diagnosed in using logical

bitmapping. From those facts, it appears that the EEPROM functional test does not provide any analog information to enhance the diagnosis phase.

3. Threshold voltage extraction

As presented in section 2, the memorization mechanism of the EEPROM is directly driven by the threshold voltage shifting of the FGT. So in order, to enhance the diagnosis process of the EEPROM, it is of the prime importance to be able to extract those threshold voltage values during the functional test. First of all, the threshold value has to be defined in a product conditions. The Figure 3 gives on the same plot for drain bias given by the product context:

- For an single isolated cell, the graph of the drain current I_D versus the voltage applied on the control gate V_{cg} .
- For the same cell in the product, the output of the sense amplifier versus the voltage applied on the control gate V_{cg} for a given read current I_{read} .

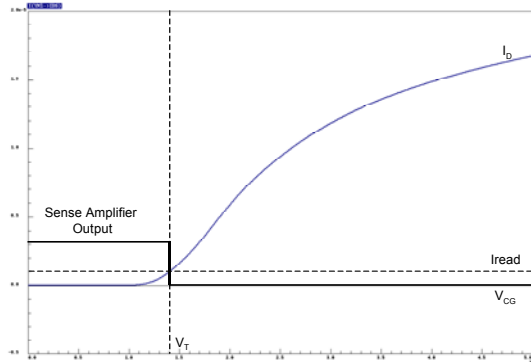


Figure 3: Threshold Voltage definition

From the plot of Figure 3, the following remarks are given in order to define the threshold voltage:

- When the V_{CG} voltage is under the threshold voltage V_T for a given read current I_{read} , the cell is not able to conduct the read current, and the output of the sense amplifier presents a high state.
- When the V_{CG} voltage is over the threshold voltage V_T for a given read current I_{read} , the cell lets flow the whole read current, and the output of the sense amplifier presents a low state.

Consequently, the threshold voltage is given by the voltage applied on the control gate of the cell V_{CG} when a switch of the sense amplifier's output occurred, for a given read current I_{read} . In the product normal working conditions, the control gate voltage is set to a value between 0V and the erase threshold voltage to differentiate a write state (the cell conducts the whole read current) and an erase state (the cell is not able to conduct the whole read current). Now, in a functional test conditions and in order to extract the virgin threshold voltage named V_{TUV} and the erased one

named V_{Terase} , the control gate voltage must be variable. The main idea is to define two measurement windows, one over the V_{TUV} specification window and the second over the V_{Terase} specification window. In controlling the steps of variation of the control gate voltage within this two measurement windows, the accurate extraction of the virgin and erase threshold voltages is possible as illustrated by the Figure 4, for a constant read current I_{read} . In the both cases, the threshold voltage value is given by the value of the control gate voltage when the sense amplifier switch.

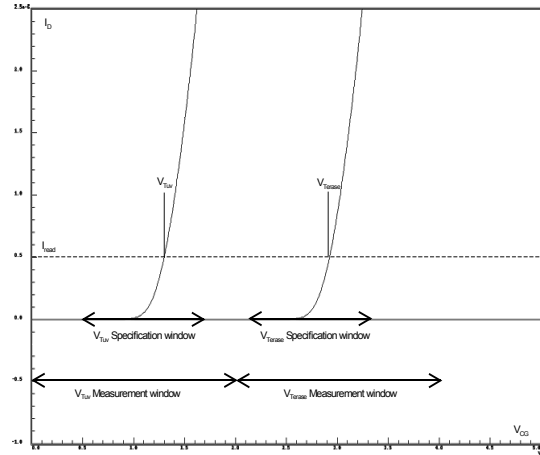


Figure 4: V_{TUV} and V_{Terase} measurement principle

In the case of the write threshold voltage, named V_{Twrite} , the extraction can not be performed directly. Indeed, V_{Twrite} is negative and a negative voltage can not be applied on the control gate. To overcome this constraint, a current measurement window is defined over the current specification window. In this case the control gate is grounded, and the read current increases step by step in the measurement window until the sense amplifier switch and gives the image in current of the threshold voltage, as illustrated Figure 5.

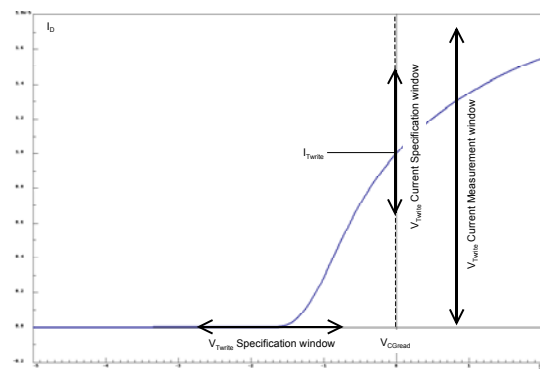


Figure 5: V_{Twrite} measurement principle

The practical realization of the three threshold voltages extraction implies some constraints, which are given below:

- The area overhead introduced by the V_T extraction features must be relatively low.
- The test time overhead due to the V_T extraction must be as limited as possible.
- The specifications of the memory has to be preserved in normal mode of operation.
- The V_T value must be provided in a digital format to be memory tester consistent or easily observable through random logic in the case of embedded EEPROM.

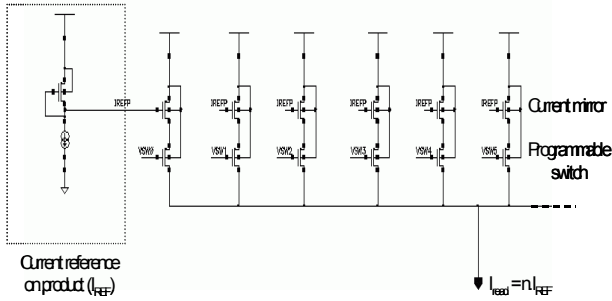


Figure 6: Multiple programmable current source

To extract the threshold voltages, the read operation has to be modified. In the case of the extraction of the V_{Twrite} , the read conditions are given below:

- The control gate is set to the ground.
- The current injected by the sense amplifier increases by steps of I_{REF} from 0 μA to I_{max} the upper limit of the measurement window.

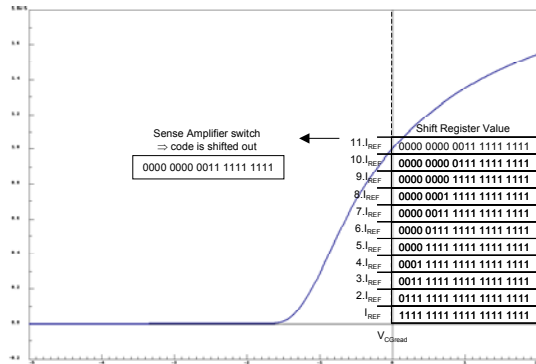


Figure 7: V_{Twrite} extraction steps

To realize the current increase by step of I_{REF} , a programmable multiple current source [7] is introduced as illustrated in Figure 6. Each step of I_{REF} is performed by switching on successively the programmable switches, moreover it is important to note that the current reference used is already on the product. The PMOS switches are controlled by a shift register, which starts with all bits at "1" and is fed with a "0" value. The shifting process stops when the sense amplifier output switch, then the shift register value are shifted serially via the sense amplifier output, as illustrated in Figure 7.

In the case of the extraction of the V_{Tuv} or the V_{Terase} , the read conditions are given below:

- The current injected by the sense amplifier is set to its nominal value I_{REF} .
- The control gate voltage increases by steps of V_{REF} from the minimal value of the measurement window to the maximal one.

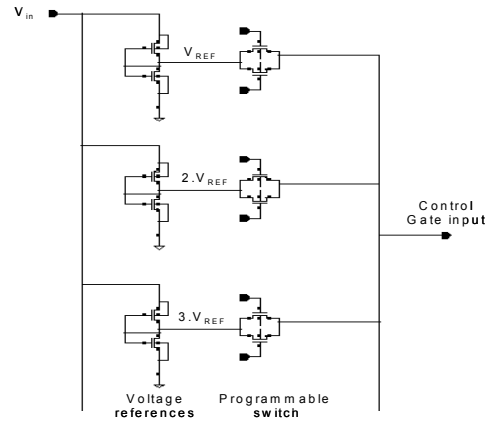


Figure 8: Multiple programmable voltage references

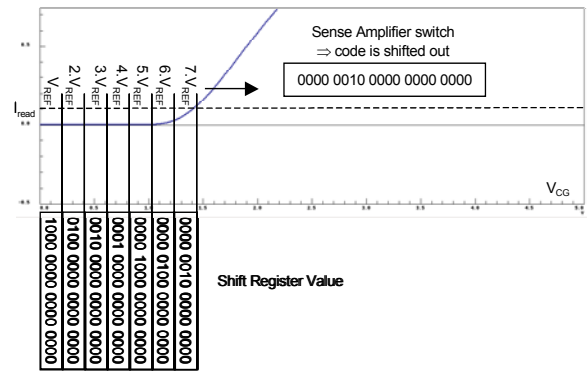


Figure 9: V_{Tuv} extraction steps

To realize the control gate voltage increases by step of V_{REF} , different voltage references [7] are introduced, the schematic of a part of this structure is given in Figure 8. By switching from one reference to the next one, the steps are performed. Here also, the transmission gates are controlled by a shift register, which shifts a "1" and has all the other bits to "0". In the same way, the shifting process stops with the sense amplifier output switch. The contents of the shift register are shifted out via the sense amplifier output. It is important to note, that partially the same structure is used for the extraction of both V_{Tuv} and V_{Terase} , the only change concerns the bias voltage V_{in} , which can be set to two different values:

- V_{boost} , given by a voltage booster generator [8] for the V_{Terase} extraction,
- V_{dd} , for the V_{Tuv} extraction.

The Figure 9 illustrates the extraction process in the case of a virgin cell (V_{Tuv}). To validate the threshold voltage extraction, ELDO [9] electrical simulations are performed on a $0.25\mu\text{m}$ technology EEPROM, with $V_{dd} = 3.3\text{V}$, from ST-Microelectronic (Rousset-France). The netlist of simulation includes:

- A 4×4 memory array with 4 bits word.
- The row decoder, word decoder.
- The sense amplifiers for each bit.
- The latches
- The threshold voltages extraction structure.

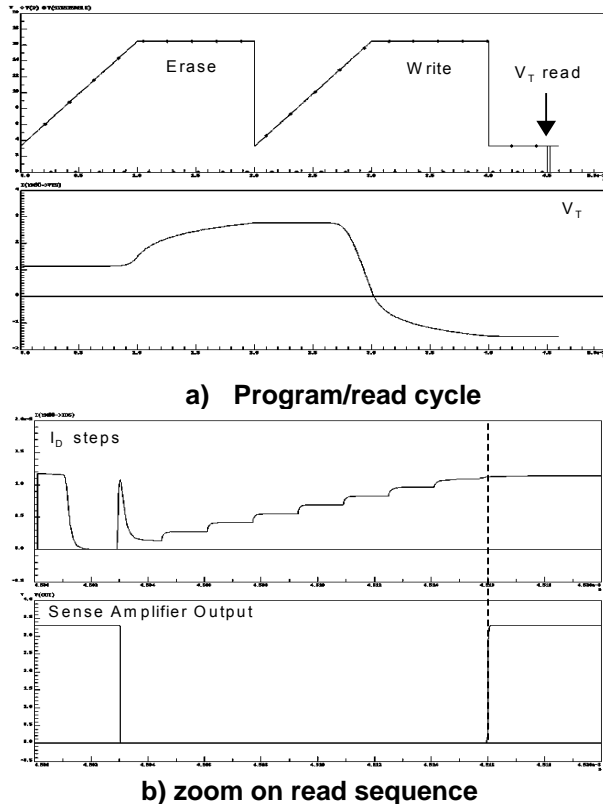


Figure 10: V_{Twrite} extraction simulation plots

The FGT simulation model is based on a MM9 core [10] and is described in HDLA. The Figure 10 shows a screen capture of a V_{Twrite} extraction, with the following curves:

- On the Figure 10.a, the evolution of the threshold voltage is given versus the time and follow the application of a high voltage. Moreover, the V_{Twrite} read sequence is given and represents less than 0.5% in the worst case of the program time.
- On the Figure 10.b, a zoom on the read sequence is given with the current steps and the sense amplifier output switch.

To summarize, the area overhead introduced by the extraction structure is relatively low compare to the memory area. The time overhead remains also very low, the read operation time increases to 0.5% of the program operation time. In the same time, the normal mode of

operation of the memory is preserved. The threshold values are given in a digital data format, so the extraction process does not required any analog pin on the tester, making it fully digital tester compliant or easily observable via the random logic in the case of embedded EEPROM.

4. Diagnosis methodology

A classical approach to diagnose and debug memory is to build a logical bitmap view of the memory array. During the functional test, the logical bitmap is built in order to check topologically the state of each cell. From this bitmap view, significant signature are categorized (Single bit, Column, Row, Partial Column etc ...) to help in the determination of root cause failure mechanism [5]. However, several failure mechanism can manifest the same signature. To minimize this limitation, a solution is to extract other significant electrical parameters. This is particularly true, when the diagnosis process targets analog cells, such as the EEPROM ones. The most informative electrical parameter in the EEPROM cell is the threshold voltage value. So, the main idea, when extracting the threshold voltage during the functional test, is to build an **Analog Bitmap**, i.e. three bitmap representations of the EEPROM memory array, one for each threshold value (V_{Tuv} , V_{Terase} and V_{Twrite}). This analog bitmap can be treated in the same way than the digital one, with signatures categorization depending on the threshold values. This signatures categorization might be very useful to characterize process and defect impact on the array. To build the analog bitmap, the digital data coming from the shift register have to be converted. The conversion of the register value to the analog threshold voltage value is straightforward for the virgin and erase cases. Indeed, the position of the "1" in the data stream gives the number of V_{REF} . In the example of the Figure 9, the register value is "0000 0010 0000 0000", which gives an analog V_{Tuv} equal to $7 \cdot V_{REF}$. For the write case, the register value gives directly the read current. Indeed, the read current is equal to the number of "0" plus one, in the example of the Figure 7, the read current is equal to $11 \cdot I_{REF}$. This current value is used as an image of the write threshold value, thus a specification window is defined in current. The Figure 11 gives the analog bitmap obtained with the simulation of our 4×4 memory array with 4 bits word. In this array, half of the cells are designed with the target geometry of the technology and the other half are randomly dimensioned with geometric parameters that present a variation contained between 5 and 50% of the target. In this example, the digital bitmap does not show any failing bit, however the analog bitmap allows to localize the cells which have not their threshold voltages included in the specification. From, this failing threshold values, specific EEPROM diagnosis tools might be used to identify the root cause(s) of the geometric defect parameters [11].

Moreover, like the digital bitmap, signatures are categorized (cell-write, cell-erase, cell-virgin, Column-write etc ...) to help here also to determine the root cause mechanism. To complete the diagnosis, the distribution of each threshold voltages can be generated for the memory array, in order to estimate the matching with the threshold voltage specifications. The distribution of our array are presented Figure 12, this distributions give information about the process control and the defect repartition over the all array.

5. Conclusion

The Non Volatile Memory are based on analog cells, that leads to critical problems of process control and design. In this paper, an integrated structure is presented to extract the analog signatures of each cell in the array i.e. the different threshold voltages. This structure allows to extract the threshold voltages during the functional test with a very low overhead in terms of area and time. Moreover, the threshold voltages are extracted in a digital format, which enable:

- To be fully digital tester compliant.
- To facilitate their observation through logical core in the case of embedded EEPROM.

From the extraction of the threshold voltages, a diagnosis methodology based on analog bitmapping is developed to be used with the classical digital bitmapping. Thus the diagnosis of the analog behavior of each cell in the array is performed more efficiently. This diagnosis methodology gives also the threshold distribution over the array, which may help to qualify the process control.

6. Reference

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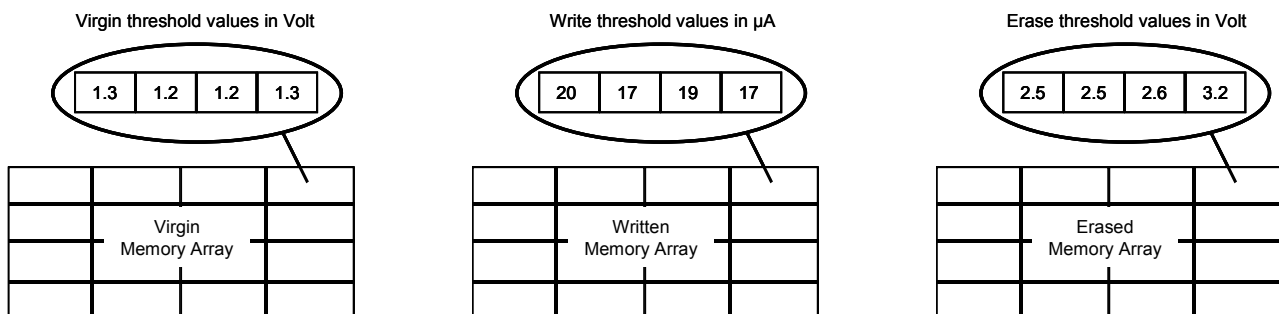


Figure 11 : Analog Bitmap representation.

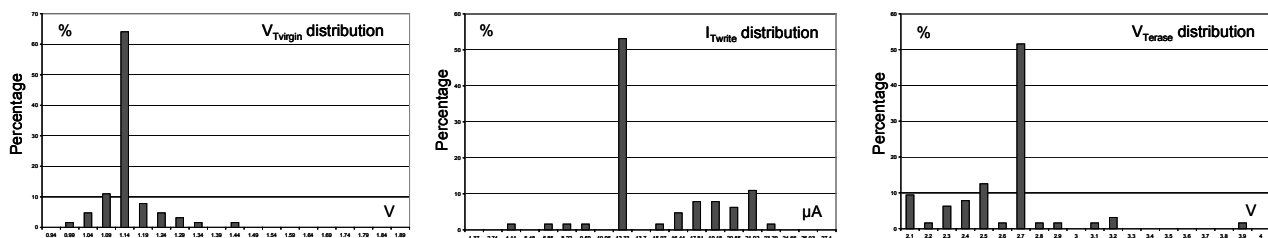


Figure 12 : Threshold Voltages distribution for the 64 bits array.