Effects of Deterministic Jitter in a Cable on Jitter Tolerance Measurements

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Abstract

This paper presents a new jitter tolerance model that includes the effect of deterministic jitter in interconnects. First, it is shown by experiment that the deterministic jitter in a cable can significantly affect its jitter tolerance. Then, the new jitter tolerance model is verified with experimental data on cables of various lengths, using both PRBS and T11 test patterns.

1. Introduction

Many new developments have occurred recently in jitter testing of communication devices. Efforts are being made to reduce test time and cost while preserving measurement accuracy. Jitter tolerance tests are commonly performed on receiver circuits using sinusoidal jitter [1]. In addition, use of both deterministic and random jitter (see definitions in Section 2) has also been proposed in jitter tolerance testing [2]. Random jitter measurement has received much attention in the past few years. However, deterministic jitter is emerging as a critical problem in both test instrumentation implementations and physical layer designs [3] such as high-frequency wireline local area networks, the PCI Express link, and interconnects.

The PCI Express interface standard [4] is being developed as a successor to the well-known 32-bit PCI bus, but with much higher bandwidth for use in future computer and communication systems. This differential serial 1-bit bus operates initially at 2.5 Gbps, with a projected growth path to 10 – 12 Gbps. It also employs the current communication scheme for data recovery. As such, PCI Express is subject to bit errors due to jitter like any other communication channel.

While protocols have been incorporated into the standard (e.g. coding scheme, design-for-test features, worst-case test patterns), there remains a need to characterize and test the PCI Express bus for jitter tolerance and bit error rate (BER) when the bus is embedded in a large-scale system. This characterization test is also required for high-frequency cables used in local area networks and in standard test systems and instrumentation. High-frequency buses, cables, and interconnects inject deterministic jitter into the data stream, and this impacts the correct recovery of transmitted data.

In this paper, we introduce a new model that includes the effect of deterministic jitter caused by an overall interconnect network on the jitter tolerance. It takes into account both the length of the interconnect (be it an on-chip bus, on-board bus, or a cable), and one of the test patterns commonly used for BER testing. The method relies on the analysis of the timing misalignment between the bit stream and the divided recovered clock. Our analysis yields an equation that models the contribution of the deterministic jitter to the overall jitter tolerance in an interconnect network.

Terminology and definitions are presented in Section 2. The theoretical model is derived in Section 3. In Section 4, jitter tolerance results obtained from testing a coaxial cable are presented. The limitations of the proposed method are discussed in Section 5.

2. Terminology

Timing Jitter [5]. Timing jitter is the uncertainty in the edge of a square wave signal, or the uncertainty in the zero-crossing point of any other signal. If the total instantaneous phase of a signal is denoted by $\phi(t)$ and the edge position or zero crossing is at a time nT, then the timing jitter is the variation of $\phi(nT)$, denoted by $\Delta\phi[n]$. $\Delta\phi[n]$ is shown in Figure 1.

Sinusoidal Jitter. Sinusoidal jitter refers to the use of a sinusoidal phase modulation provided by a sinusoidal jitter source. It is normally used in standard jitter tolerance testing [1], [2]. The sinusoidal jitter is described by $\frac{\Delta\theta_{PP}}{2}\cos(2\pi f_{PM} t)$ where $\frac{\Delta\theta_{PP}}{2}$ is the jitter amplitude ($\Delta\theta_{PP}$ is the peak-to-peak value of timing jitter) and f_{PM} is the jitter frequency [6].

Random Jitter. Random jitter (RJ) encompasses timing edge uncertainties introduced by random noise sources. Random jitter follows a Gaussian distribution, is uncorrelated with other system noise sources, and tends to be unbounded as test time increases. Random jitter has been a focus of jitter testing and design of low-jitter oscillators in the past several years [7], [8], [9].

Deterministic Jitter. Deterministic jitter (DJ) also results in timing edge uncertainties, but its values are bounded and its sources are much easier to identify. The edge deviations may be due to power supply variations, data patterns (data-dependent jitter DDJ or inter-symbol interference ISI), and systematic displacements due to interconnects, transistor switching delays, and ground loops. It is interesting to note that while the sources of DJ are easier to identify, the impact of DJ is just as severe as the impact of RJ on communication systems.

Jitter Tolerance [6]. Jitter tolerance measurement is an extension of the bit error rate (BER) testing. It is a measure of the boundary across which a deserializer starts to introduce errors due to the applied data transition jitter. This boundary separates the erroneous region and the error-free region as a function of the amplitude of the input jitter applied to the deserializer under test. The input jitter amplitude at the boundary gives an upper limit of maximum tolerable jitter [10]. A SONET jitter tolerance test uses sinusoidal jitter at a fixed frequency and a given jitter amplitude to modulate edges of a data clock [1].

3. Jitter Tolerance Model for Deterministic Jitter

If no timing jitter is applied, the ideal sampling point of a signal is at the center of the bit interval i.e. 0.5 UI (Unit Interval) offset from the edge of the bit. If deterministic jitter is applied and increased, the misalignment between the edges of the recovered clock and the bit edge will be increased proportionally from 0.5 UI. This makes the recovered clock sample the waveform of the current bit at the off-center timing. Thus, in order to recover data correctly, deterministic jitter due to an interconnect must be taken into account in the design and implementation of physical layer devices.

3.1 Modeling Deterministic Jitter due to Interconnects

The derivation of the jitter model uses the configuration depicted in Figure 2. It is assumed that a source data stream is transmitted over an interconnect of length l. For a coaxial cables with dielectric constant ε_r, the delay time as a function of length is given by [11]:

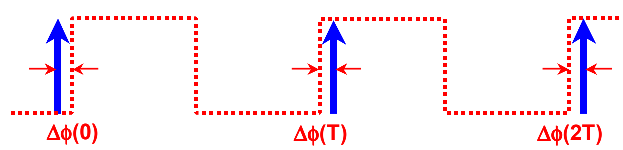

Figure 1. Illustration of timing jitter.

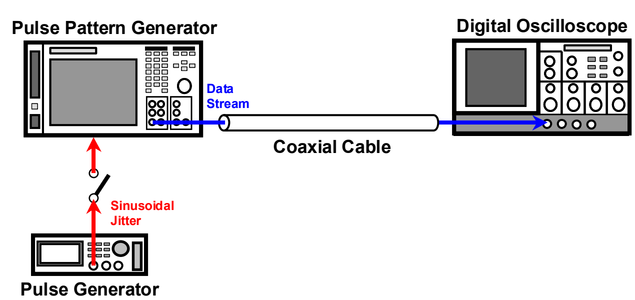

Figure 2. Interconnect topology used for theoretical derivation.

$$\tau_d = C_1\sqrt{\varepsilon_r}\ l \qquad (1)$$

The 3-dB bandwidth of the interconnect is inversely related to the length. The rise time of a step signal transmitted over this interconnect is [12]:

$$RiseTime \approx \frac{1}{2Bandwidth_{-3dB}} \qquad (2)$$

Thus the rise time is proportional to the interconnect length. For a specific run of K_{RUN} consecutive 0 or 1 bits, the rise time can be modeled by the equation:

$$RiseTime = C_2 \frac{(K_{RUN})^{\alpha}}{8} l \qquad (3)$$

where C_2 is a proportional constant depending on the type of interconnect. The exponent parameter, α is a parameter to be determined based on experimental results.

For a specific run of K_{RUN} bits, the overall delay due to both the interconnect length and the data pattern is:

$$\tau_d(K_{RUN}, l) = \tau_d + \frac{RiseTime}{2} = \left(C_1\sqrt{\varepsilon_r} + C_2 \frac{(K_{RUN})^{\alpha}}{16} \right) l \qquad (4)$$

The second term is the timing variation due to the data pattern. For a general data pattern (e.g. a PRBS or a T11 data pattern [2]) with many different runs of 0 and 1 bits, the timing uncertainty due to the entire test pattern is:

$$\Delta\tau(K_{RUN}, l) = \sum_{K_{RUN}} C_2 \frac{(K_{RUN})^{\alpha}}{16} l \qquad (5)$$

Therefore, the peak-to-peak timing uncertainty due to both the interconnect length and the test pattern is:

$$\begin{aligned}\Delta\tau_{PP}(K_{RUN}, l) &= \delta[\tau_d(\min(K_{RUN}), l)] + \delta[\tau_d(\max(K_{RUN}), l)]. \\ &= C_2 \frac{\{\max(K_{RUN})\}^{\alpha} - \{\min(K_{RUN})\}^{\alpha}}{16} l\end{aligned} \qquad (6)$$

Note that $\Delta\tau_{pp}(K_{RUN}, l)$ is generally non-zero due to the different values of K_{RUN}. This peak-to-peak timing uncertainty is the *deterministic jitter* in the data stream due to both the interconnect and the data pattern.

By using K_{RUN}, we implicitly assume adjacent run length changes from each other. Let us illustrate the data-dependent zero-crossing time. Since the duration of *max*(K_{RUN}) of *bits 1* gives sufficient time to the *sequence of bits 1* itself to reach the *100 %* amplitude level, it takes maximum time for the *following bit 0* to fall from the *100 %* level and cross the *50 %* level. Thus, the maximum delay occurs when adjacent runs change their run-lengths from *max*(K_{RUN}) to a *short* K_{RUN}, or from a *long identical-bit sequence* to a *short identical-bit sequence*. On the other hand, since the duration of *min*(K_{RUN}) of *bit 1* succeeding to *max*(K_{RUN}) of *bits 0* gives insufficient time for the *bit 1* itself to reach the *100 %* amplitude level, it takes the minimum time for the *following bit 0* to fall from the *100 %* level and cross the *50 %* level. Therefore, the minimum delay takes place when *min*(K_{RUN}) follows *max*(K_{RUN}).

For a clock transmission where the bits alternate between 1 and 0 with no runs of consecutive identical bits (e.g. $K_{RUN}=1$), Equation (6) shows that there is no deterministic timing uncertainty in the clock due to the interconnect. Furthermore, from Equation (6) it follows that the more a particular run K_{RUN} (e.g. > 4) occurs, the more that erroneous bits are likely to be encountered. Taking the adjacent-run change into account, the probability density function of an erroneous bit occurrence is given by:

$$p(ErrorBit) \equiv f\left(p(K_{RUN} \leftrightarrow 1_{RUN}), l\right) \qquad (7)$$

where $p(K_{RUN} \leftrightarrow 1_{RUN})$ is the probability density function that a run of run length K_{RUN} follows a run of run length *1* or that a run of run length *1* follows a run of run length K_{RUN}. The result provides a criterion for selecting the test pattern to generate the deterministic jitter effectively. In Section 4.2, we will validate the criterion by applying it to different test patterns.

3.2 Modeling Jitter Tolerance Including Deterministic Jitter

In our previous work [6], the lower limit of the maximum tolerable input jitter (in UI) for the case of sinusoidal jitter was derived as:

$$\inf(\Delta\theta_{PP}) = \frac{1}{2\left\| H_J(f_{PM}) \right| e^{-j\angle H_J(f_{PM})} - 1 \right|} \quad \text{UI} \tag{8}$$

where *inf* is the standard mathematical function denoting the lower bound, $\Delta\theta_{PP}$ is the peak-to-peak value of the input jitter, $H_J(f)$ is the jitter transfer function, and f_{PM} is the jittering frequency.

As mentioned above, clock timing is not susceptible to deterministic jitter. However, data timing is subject to deterministic jitter as shown in Equation (6). With deterministic jitter $\Delta\tau_{pp}(K_{RUN},l)$, the lower limit of the maximum tolerable input jitter can be reduced, namely,

$$\inf(\Delta\theta_{PP}, l) = \frac{1}{\left\| H_J(f_{PM}) \right| e^{-j\angle H_J(f_{PM})} - 1 \right|} \times \left[\frac{1}{2} - \Delta\tau_{PP}(K_{RUN}, l) \right] \tag{9}$$

Note that *1/2* corresponds to 0.5 UI, the timing offset of the ideal sampling point from the edge of the incoming bit [6]. Equation (9), therefore, gives the jitter tolerance value with respect to the jitter frequency of the applied sinusoidal jitter and the run length K_{RUN} of 0 or 1 bits in the applied test pattern.

For very short cables or interconnects, the deterministic jitter should not have a measurable impact on jitter tolerance. Thus the factor $\Delta\tau_{pp}(K_{RUN},l)$ in Equation (9) needs to be modified to be $\Delta\tau_{pp}(K_{RUN},l)u(l-l_{threshold})$, where $u(l)$ is the unit step function, and $l_{threshold}$ is the minimum cable length below which deterministic jitter has no impact on the maximum tolerable input jitter. Equation (9) then becomes:

$$\inf(\Delta\theta_{PP}, l) = \frac{1}{2\left\| H_J(f_{PM}) \right| e^{-j\angle H_J(f_{PM})} - 1 \right|} \times \left[1 - 2\Delta\tau_{PP}(K_{RUN}, l) u(l - l_{threshold}) \right] \tag{10}$$

The jitter tolerance model is now complete. Equation (10) expresses the maximum tolerable input jitter (or jitter tolerance) taking into account the injected sinusoidal jitter and the deterministic jitter of the interconnect. The deterministic jitter includes both interconnect length and data-pattern dependence.

4. Experimental Results

To validate the jitter models developed in Section 3, results are presented from experimental studies performed on cables of various lengths. The cables are SMA coaxial cables (DGM224 manufactured by Junkhosya) for high-frequency applications. Section 4.1 shows the results of cable bandwidth and rise time measurements. Section 4.2 shows the results of jitter tolerance measurements with these cables.

4.1 Cable Bandwidth, Rise Time, and Deterministic Jitter Measurements

The cable group delay values and bandwidths for various lengths up to 30 m were measured with an HP 85107A network analyzer system. As plotted in Figure 3(a), the cable group delay is exactly proportional to the cable length. Furthermore, for each length, cable group delay is constant up to 40 GHz. Although non-zero differential group delay between two sidebands induces jitter, the flat cable group delay induces no timing jitter penalty. On the other hand, Figure 3(b) shows that the bandwidth varies inversely with the cable length, as mentioned in Section 3.1. It is also clear that the curve has two slopes, with an approximate break point at $l = 10$ *m*. The change in slope is minimal so the equations developed above are still valid.

The effect of run length (K_{RUN}) on rise or fall time on the cable was measured next. The measurements were made on cables of lengths *75 cm*, *10 m*, and *20 m*, using the following test pattern:

5X<10> 15X<1> 14X<0> 1X<1>
13X<0> 2X<1> 12X<0> 1X<1>
1X<0> 1X<1> 11X<0> 4X<1>
10X<0> 1X<1> 3X<0> 1X<1>
9X<0> 2X<1> 2X<0> 2X<1>
8X<0> 1X<1> 1X<0>

The notation "5X<10>" means the pattern 10 was repeated 5 times (or 1010101010). An expression for the rise time, obtained by curve fitting the experimental data, is:

$$RiseTime \approx \frac{(K_{RUN})^{2/3}}{40} l \qquad (11)$$

The value of α = 2/3 is based on experimental results shown in Table 1 with various run lengths of 0 and 1. Column 2 is the measured rise or fall time and column 3 is the computed time based on Equation (11).

With the new run-length dependence in Equation (11), the peak-to-peak timing uncertainty in Equation (6) is as follows:

$$\Delta\tau_{PP}(K_{RUN}, l) = C_{RUN} \frac{\{\max(K_{RUN})\}^{2/3} - \{\min(K_{RUN})\}^{2/3}}{40} l \qquad (12)$$

This deterministic timing jitter is a function of cable length, and is plotted in Figure 4 for two standard test patterns [2]: a 15-stage PRBS pattern and a T11 compliant jitter tolerance pattern. The data points are connected by solid lines, while Equation (12) is plotted with dotted lines. The agreement between the experimental data and the theoretical prediction is very good in both cases.

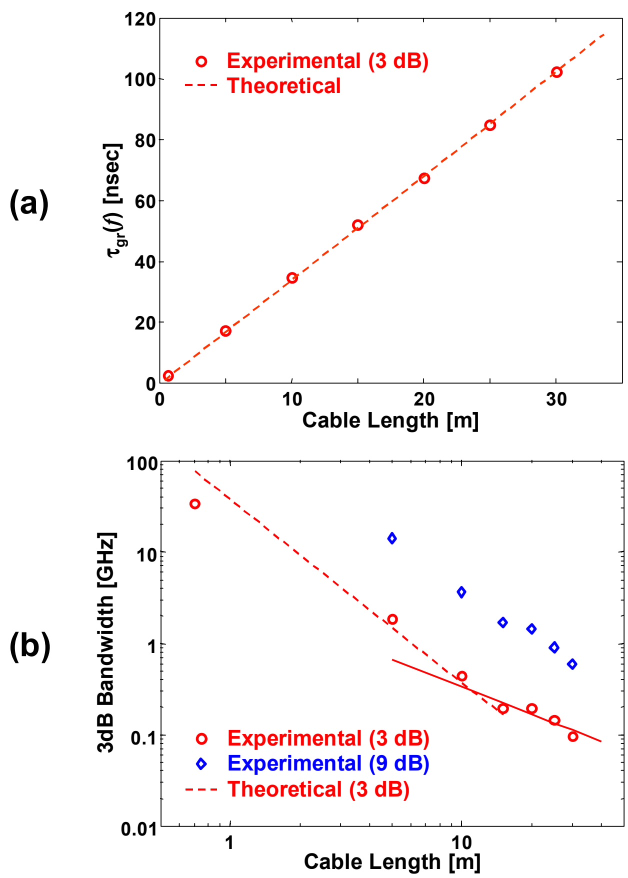

Figure 3. Cable bandwidth and group delay for DGM 224 cables. (a) Cable group delay vs. length. (b) Cable bandwidth vs. length.

Table 1. Rise time as function of run lengths.

Run Length	Measured Rise Time	Theoretical Value
15 <1>	1.50 ns	1.52 ns
14 <0>	1.50 ns	1.45 ns
11 <0>	0.90 ns	1.24 ns
10 <0>	0.80 ns	1.16 ns
04 <1>	0.75 ns	0.63 ns
02 <1>	0.45 ns	0.40 ns
01 <1>	0.30 ns	0.25 ns

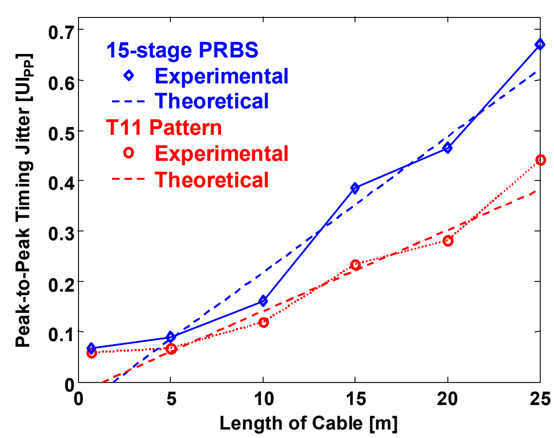

Figure 4. Deterministic timing jitter for two standard test patterns.

Note that for very short cable lengths ($l < 5\ m$), the deterministic jitter is very low, and is identical for both test patterns.

4.2 Jitter Tolerance Measurements

Figure 5 shows the experimental test setup used to measure jitter tolerance while taking into account the deterministic jitter due to the cable. The pulse pattern generator (Advantest D3371) generates both the source clock and the test patterns at 2.48832 GHz. The modulation source built into the Advantest D3371 injects sinusoidal jitter into this source clock to modulate the edges of the bit streams. The bit stream is fed into a Maxim MAX3880 deserializer [13] using cables (DGM224) of various lengths.

A limiting amplifier is used to eliminate possible amplitude modulation. The serializer is used in a loopback configuration and the error detector measures the bit error rate in the recovered data. Except for the cable under test, all the other cables are very short ($< 0.7\ m$), and therefore should

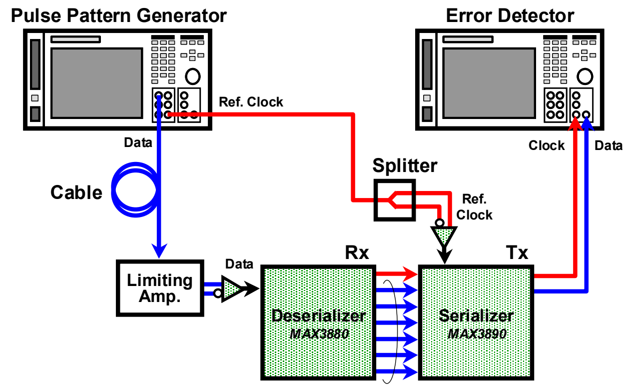

Figure 5. BER and jitter tolerance test setup.

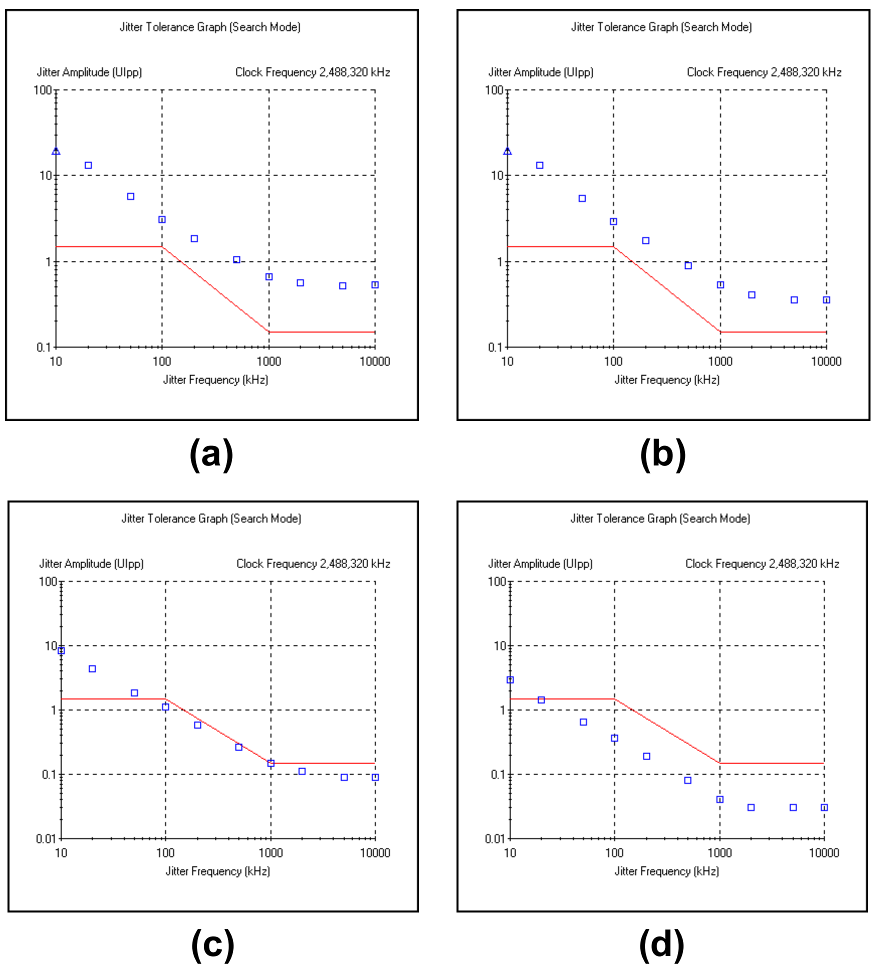

Figure 6. Measured jitter tolerance for 4 cable lengths:
(a) *0.75 m*, (b) *10 m*, (c) *15 m*, and (d) *20 m*.

have no effect on either jitter amplitude or jitter frequency.

Figure 6 shows the jitter tolerance results for 4 cable lengths. A 15-stage PRBS pattern was applied to generate deterministic jitter. Figures 6(a) and 6(b) demonstrate that at short lengths (*l = 0.75 m* and *10 m*), the deterministic jitter due to the cables has a negligible effect on the overall jitter tolerance, as expected. Figures 6(c) and 6(d) show that at longer lengths (*l = 15 m* and *20 m*), the deterministic jitter due to the cables corrupts the recovered data and introduces a large BER. The deterministic jitter uniformly shifts the jitter tolerance curves downward over the entire jitter frequency range.

Figure 7 shows the eye diagram measured by an oscilloscope (Tektronix TDS7404), of the applied PRBS at the input terminal of the device, for the case *l =15 m*.

In Figure 8, the circles or the diamonds plot the measured values of jitter tolerance estimated using the two standard test patterns: a 15-stage PRBS pattern (same measurement data as shown in Figure 6) and a T11 compliant jitter tolerance pattern. The dashed lines are the theoretical jitter tolerance values predicted by Equations (10) and (12).

In both graphs of Figure 8, a cable length of *10 m* or less does not affect the jitter tolerance value. The degradation due to the cable deterministic jitter is significant only for longer lengths. This validates the use of the unit step function *u(l)* in Equation (10).

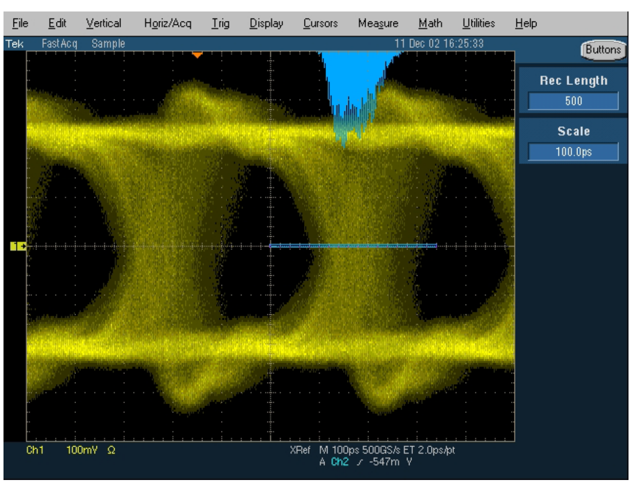

Figure 7. Eye diagram for *l = 15 m*.

We will use the word *effective DJ-cable length* to mean the difference (physical length – 10 m).

Secondly, the measured values of the cable deterministic jitter penalties caused by the 15-stage PRBS pattern agree well with the values estimated with Equation (10). Therefore, we have verified that Equation (10) can estimate the worst-case jitter penalties caused by the PRBS test pattern, which satisfies Equation (7): $p(K_{RUN} \leftrightarrow 1_{RUN})\big|_{K=4} = 6\%$.

On the other hand, Figure 8(b) shows that there is a large difference between the measured and the calculated values of the jitter tolerance using the T11 compliant jitter tolerance pattern at cable lengths of *15 m*, *20 m*, and *25 m*. This is mainly due to the insufficient occurrences of the particular runs in the test pattern: $p(K_{RUN} \leftrightarrow 1_{RUN})\big|_{K=4} = 0.5\%$.

Since 4X<0>-to-1X<1> in the T11 test pattern occurs 12 times less than 4X<0>-to-1X<1> in the 15-stage PRBS, the T11 test pattern causes the measurement to overestimate the jitter tolerance values. In other words, the combination of the *effective DJ-cable length* (*15 m* = 25 m – 10 m) and the T11 test pattern must be three times longer than the combination of the *effective DJ-cable length* (*5 m* = 15 m – 10 m) when the 15-stage PRBS is used. Note that this one-to-one correspondence is clearly shown at {*15 m, 10 kHz*} in Figure 8(a) and {*25 m, 10 kHz*} in Figure 8(b). This demonstrates the effectiveness of the criterion given by Equation (7).

5. Limitations

The experimental data verifies that the rise and fall time dependence on the run length of 0 and 1 bits can be modeled with $(K_{RUN})^{2/3}$ for SMA coaxial cables. For other types of interconnects, experiments are required in order to evaluate this dependence. Also, the length threshold over which the deterministic jitter becomes significant needs to be estimated for each type of interconnect.

The derived jitter tolerance model only includes penalties for injected sinusoidal jitter and data-dependent jitter due to interconnects, and does not include other factors such as pulse width distortion and duty cycle distortion. If these other factors are present, the equations presented in this paper will underestimate the jitter tolerance.

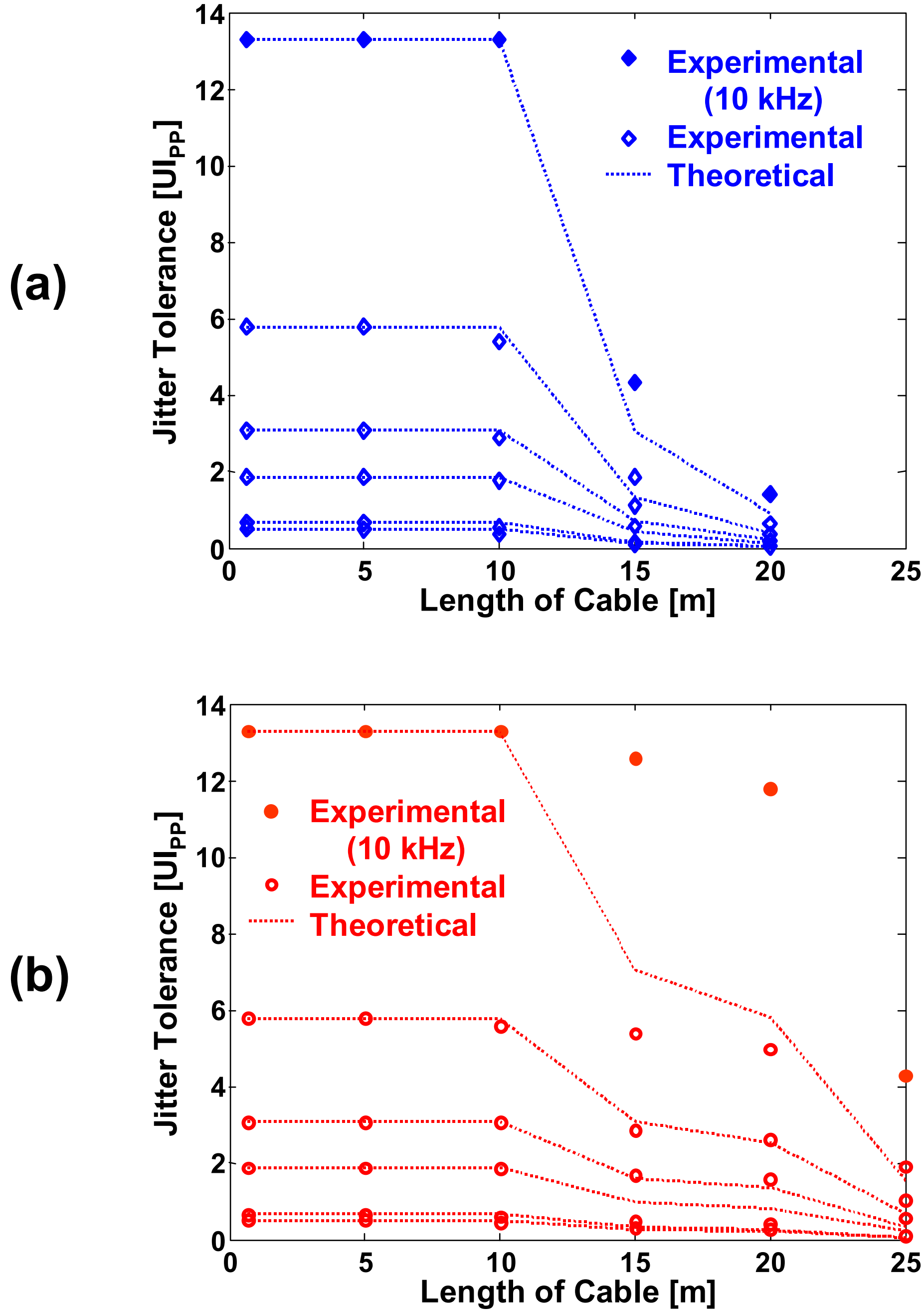

Figure 8. Jitter tolerance vs. cable length for two standard test patterns: (a) 15-stage PRBS and (b) T11 compliant jitter tolerance pattern.

6. Conclusion

A new jitter tolerance model was presented which incorporates the deterministic jitter effects of interconnects on the overall estimation of jitter, assuming that sinusoidal jitter is injected into the bit stream. The model predicts overall system jitter tolerance based on the cable length and the applied data pattern.

It was demonstrated that data-dependent jitter together with an increased interconnect length can significantly degrade the jitter tolerance, resulting in increased bit error rates in the recovered data. The new model was verified using SMA coaxial cables and two standard test patterns (PRBS and T11 compliant jitter tolerance pattern).

The verification process also validated a better model for the rise and fall times of the signal as a function of the data patterns and run lengths of 0's and 1's in the bit stream. A criterion for effectively selecting a test pattern to generate deterministic jitter was also provided.

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