The PXI Modular Instrumentation Architecture

Eric Starkloff, Tim Fountain, Garth Black
National Instruments, 11500 N.Mopac Expwy, Austin, TX. 78759, USA

Abstract

This paper is a technology review of PXI. It describes the basic PXI architecture and looks in more detail at the features of the slot 2 timing and triggering module.

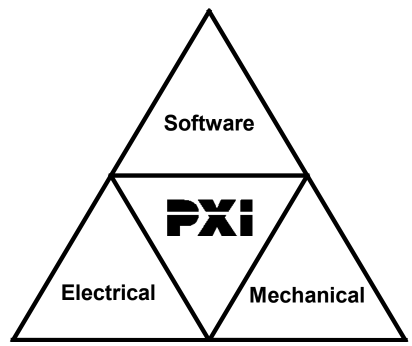
1. Objectives of the PXI Standard

PXI was created in response to the needs of a variety of instrumentation and automation users who require ever increasing performance, functionality, and reliability from compact rugged systems that are easy to integrate and use. Existing industry standards are leveraged by PXI to benefit from high component availability at lower costs. Most importantly, by maintaining software compatibility with industry-standard personal computers, PXI allows industrial customers to use the same software tools and environments with which they are familiar.

PXI leverages the electrical features defined by the widely adopted Peripheral Component Interconnect (PCI) specification. It also leverages the CompactPCI form factor, which combines the PCI electrical specification with rugged Eurocard mechanical packaging and high-performance connectors. This combination allows CompactPCI and PXI systems to have up to seven peripheral slots per bus segment versus four in a desktop PCI system. Systems with more expansion slots can be built by using multiple bus segments with industry-standard PCI-PCI bridges. For example, a 13-slot PXI system can be built using a single PCI-PCI bridge (see Section 2.3.3). The PXI specification adds electrical features that meet the high-performance requirements of instrumentation applications by providing triggering, local buses, and system clock capabilities. PXI also offers two-way interoperability with CompactPCI products. By implementing desktop PCI in a rugged form factor, PXI systems can leverage the large base of existing industry-standard software. Desktop PC users have access to different levels of software, from operating systems to low-level device drivers to high-level instrument drivers to complete graphical APIs. All of these software levels can be used in PXI systems. PXI defines software frameworks (for Microsoft Windows 95, 98, NT, 2000 and XP) for complete systems and requires appropriate device driver software for all PXI peripheral modules to ease system integration. Furthermore, PXI implements the Virtual Instrument Software Architecture (VISA). VISA is used to locate and communicate with serial, VXI, and GPIB peripheral modules. PXI extends VISA beyond these interfaces to allow for the location and control of PXI peripheral modules. This extension preserves the model for instrumentation software that has been adopted by the instrumentation community. The result is a very powerful software commonality that spans PXI, CompactPCI, desktop PCI, VXI, GPIB, and other instrumentation architectures.

2. PXI Technical Features

2.1 Overview



The PXI (PCI eXtensions for Instrumentation) specification defines a rugged PC platform for measurement and automation. PXI modular instrumentation leverages the high-speed PCI (Peripheral Component Interconnect) Bus which is the de facto standard driving today's desktop computer software and hardware designs. As a result, PXI users can enjoy all the benefits of PCI within an architecture that supports mechanical, electrical, and software features that make sense for test and measurement, data acquisition, and industrial computing applications.

The PXI specification, now at revision 2.1, leverages the CompactPCI specification, which defines a rugged form factor for PCI that offers superior mechanical integrity and easy installation and removal of hardware components. PXI products offer higher and more carefully defined levels of environmental performance required by the vibration, shock, temperature, and humidity extremes of industrial environments. PXI adds mandatory environmental testing, EMC testing, and active cooling to the CompactPCI mechanical specification to ease system integration and ensure multi-vendor interoperability.

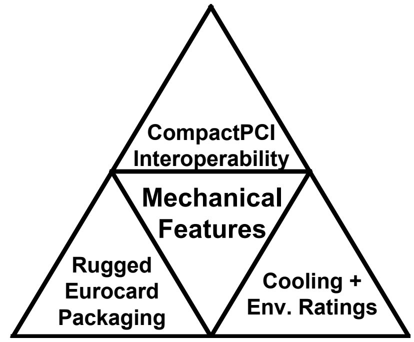
PXI offers the same high-performance electrical features as PCI including 132 MB/sec data rates and Plug-and-Play functionality. The most compelling benefit for PXI, however, is PCI's dominance in the desktop PC marketplace which is served by over 800 suppliers. The result is widespread availability of PCI-based silicon, firmware, drivers, operating systems, and software applications – all of which can be applied cost-effectively in PXI-based systems. As with CompactPCI, PXI offers nearly twice as many peripheral slots as desktop PCI systems per bus segment. Thus, multiple-segment PXI systems can offer far more slots than extended desktop systems resulting in far more I/O capability. Additionally, PXI meets the more specific needs of instrumentation users by adding an integrated Trigger Bus and Reference Clock for multi-board synchronization, a Star Trigger Bus for very precise timing, and Local Buses for side-band communication between adjacent peripherals.

PXI defines system-level software requirements for standard frameworks such as Microsoft Windows which already have millions of users of thousands of applications. This preserves multi-vendor compatibility and eases system integration tasks. Furthermore, all PXI peripherals must include appropriate device driver software eliminating costly end-user development efforts.

As a result of PXI's mechanical, electrical, and software features, instrumentation system developers acquainted with applications designed for desktop PCs can immediately leverage these resources in a more rugged PXI form factor at an incremental cost.

2.2 Mechanical Features

PXI modular instrumentation offers mechanical features that make PXI systems well-suited for industrial environments and make them easy to integrate. The rugged Eurocard packaging system and high-performance IEC connectors called out by CompactPCI are also used in PXI. PXI adds specific cooling and environmental requirements. Finally, two-way interoperability with standard CompactPCI systems is offered through the PXI specification.



The following PXI mechanical features are shared with CompactPCI:

2.2.1 High Performance Connector System

PXI employs the same advanced pin-in-socket connector system called out by CompactPCI. These highly dense (2mm pitch) impedance-matched connectors are defined by the International Electrotechnical Commission (IEC-1076) and offer the best possible electrical performance under all conditions. These connectors have seen widespread use in high-performance applications particularly in the telecommunications field.

2.2.2 Eurocard Mechanical Packaging and Form Factors

The mechanical aspects of PXI and CompactPCI are governed by Eurocard specifications (ANSI 310-C, IEC 297, and IEEE 1101.1) which have a long history of application in industrial environments. A small (3U=100mm by 160mm) and a large (6U=233.35mm by 160mm) form factor are supported. Figure 1 shows the two primary form factors and the associated interface connectors for PXI peripheral boards. The most recent additions to the Eurocard specifications (IEEE 1101.10 and 1101.11) address electromagnetic compatibility, user-defined mechanical keying, and other packaging issues that apply to PXI systems. These electronics packaging standards define compact, rugged systems that can withstand harsh industrial environments in rack mount installations.

All PXI features are implemented on the J2 connector of a 3U board and may selectively be used by peripheral boards. PXI compatible backplanes must implement the complete PXI feature set. 6U PXI boards and PXI chassis only need to implement connectors J1 and J2. Future additions to the PXI specification may define the pinouts for connectors J3 and J4 for additional functionality in 6U. Note that any 3U peripheral board can work in a 6U chassis by using a simple adapter panel. Note also that PXI features are located on pins not defined by CompactPCI. This is a key enabler for interoperability. See Section 2.2.4

PXI defines the system slot location to be on the far left end of the bus segment as shown in the system diagram of Figure 2. This defined arrangement is a subset of the numerous possible configurations allowed by CompactPCI (a CompactPCI system slot may be located in any single position on a backplane). Defining a single location for the system slot simplifies integration and increases the degree of compatibility between controllers and chassis from multiple vendors. Furthermore, the PXI specification stipulates that the System Controller board should expand to the left into what are defined as controller expansion slots. These expansion slots do not have any CompactPCI connectors associated with them on the backplane and are basically expansion space. Expanding to the left prevents system controllers from using up valuable peripheral slots.

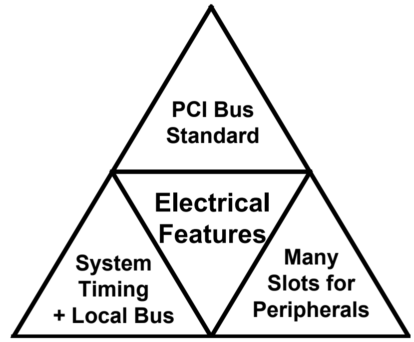
2.2.3 Additional Electronic Packaging Specifications

All mechanical specifications defined in the CompactPCI specification apply directly to PXI systems; however, PXI does include additional requirements that simplify system integration. As discussed above, the system slot in a PXI chassis must be located in the leftmost slot and controllers should be designed to expand to the left to avoid using up peripheral slots. The airflow direction for required forced-cooling of PXI boards is defined to flow from the bottom to the top of a board. The PXI specification recommends complete environmental testing including temperature, humidity, vibration, and shock for all PXI products and requires documentation of test results. Operating and storage temperature ratings are required for all PXI products. Electromagnetic emissions and susceptibility testing is also required by the PXI specification to ensure compliance with international standards.

2.2.4 Interoperability with CompactPCI

An important feature offered by PXI is that it maintains interoperability with standard CompactPCI products. Many PXI compatible systems may require components that do not implement PXI-specific features. For example, a user may want to use a standard CompactPCI network interface card in a PXI chassis. Likewise, some users may choose to use a PXI compatible plug-in card in a standard CompactPCI chassis. In this case the user will not be able to implement PXI-specific functions but will still be able to use the plug-in card's basic functions. Note that interoperability between PXI compatible products and certain application-specific implementations of CompactPCI (other sub-buses) is not guaranteed. Of course both CompactPCI and PXI leverage the PCI Local Bus which ensures software and electrical compatibility. See the PXI Specification for more details.

2.3 Electrical Features



Many instrumentation applications require system timing capabilities that cannot be implemented directly across standard ISA, PCI, or CompactPCI backplanes. PXI modular instrumentation adds a dedicated system reference clock, bused trigger lines, star triggers, and slot-to-slot local buses to address the need for advanced timing, synchronization, and side-band communication. PXI adds these instrumentation features while maintaining all of the advantages of the PCI bus. Finally, PXI offers three more peripheral slots per bus segment than desktop PCI for a total of seven.

2.3.1 System Reference Clock

PXI defines the means to distribute a 10 MHz system reference clock to all peripheral devices in a system. This reference clock can be used for synchronization of multiple cards in a measurement or control system. The implementation of the reference clock on the backplane is strictly defined. As a result, the low skew qualities afforded by this reference clock make it ideal for qualifying individual clock edges of trigger bus signals for sophisticated trigger protocols.

2.3.2 Trigger Bus

PXI defines eight highly flexible bused trigger lines that may be used in a variety of ways. For example, triggers can be used to synchronize the operation of several different PXI peripheral boards. In other applications, one board can control carefully timed sequences of operations performed on other boards in the system. Triggers may also be passed from one board to another allowing deterministic responses to asynchronous external events that are being monitored or controlled. The number of triggers that a particular application requires varies with the complexity and number of events involved.

2.3.3 PCI Bridging in Multi-segment PXI Chassis

A PXI system can be built with more than one bus segment by using standard PCI-PCI bridge technology. The bridge device takes up one PCI load on each of the bus segments that it links together. Thus, a 33 MHz system with two bus segments offers 13 expansion slots for PXI peripheral modules.

(2 bus segments) × (8 slots per segment) – (1 system controller slot) – (2 slots for PCI-PCI Bridge) = 13 available expansion slots

Similarly, a three-bus segment 33 MHz system would offer 19 expansion slots for PXI peripheral modules.

The trigger architecture defined by PXI has implications for systems with multiple bus segments. The PXI trigger bus provides connectivity within a single bus segment and does not allow physical connection to an adjacent bus segment. This maintains the high performance characteristics of the trigger bus and allows multi-segment systems to partition instruments into logical groups. Multiple segments may be logically linked by providing buffers between physical segments. The star trigger provides the means to independently access all 13 peripheral slots in a two-segment system for applications in which a high number of instruments require synchronization and controlled timing. In PXI systems where there are more than two segments, it is recommended that the star triggers are only routed to the slots in the first two segments, but other routings are allowed. Figure 3 shows the PXI trigger architecture for a PXI system with two bus segments.

The estimated propagation delay across chassis PCI-PCI bridges is approximately 10 ns. This delay will vary with chassis vendor.

2.3.4 Star Trigger

The PXI star trigger bus offers ultra-high performance synchronization features to users of PXI systems. The star trigger bus implements a dedicated trigger line between the first peripheral slot (adjacent to the System Slot) and the other peripheral slots. An optional star trigger controller can be installed in this slot to provide very precise trigger signals to other peripheral boards. Systems that don't require this advanced trigger can install any standard peripheral board in this slot. Note that the star trigger can be used to communicate information back to the star trigger controller as in the case of reporting a slot's status as well as responding to information provided by the controlling slot.

PXI's star trigger architecture gives two unique advantages in augmenting the bused trigger lines. The first is a guarantee of a unique trigger line for each card in the system, or for most cards in a very large system. For large systems, this eliminates the need to combine multiple card functions on a single trigger line or to artificially limit the number of trigger times available. The second advantage is the low-skew connection from a single trigger point. The PXI backplane defines specific layout requirements such that the star trigger lines provide matched propagation time from the star trigger slot to each card for very precise trigger relationships between each card.

One example of star trigger implementation is triggering multiple digitizers to initiate simultaneous signal acquisition. By designating one digitizer in the chassis to be the master device (located in slot 2 or slot adjacent to system slot), precise triggers are passed to all other digitizers in the chassis with minimal slot-to-slot skew.

2.3.5 Local Bus

The PXI local bus is a daisy-chained bus that connects each peripheral slot with its adjacent peripheral slots to the left and right. Thus, a given peripheral slot's right local bus connects to the adjacent slot's left local bus and so on. Each local bus is 13 lines wide and can be used to pass analog signals between cards or to provide a high speed side-band communication path which does not affect the PCI bandwidth.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 volts. Keying of adjacent boards is implemented by initialization software that prohibits the use of incompatible boards. Boards are required to initialize their local bus pins in a high-impedance state and can only activate local bus functionality after configuration software has determined that adjacent boards are compatible. This method provides a flexible means for defining local bus functionality that is not limited by hardware keying.

The local bus lines for the leftmost peripheral slot on a PXI backplane is used for the star trigger. This is represented in the local bus schematic in Figure 4.

2.3.6 Peripheral Component Interconnect (PCI) Features

PXI offers the same performance features defined by the desktop PCI specification with one notable exception. A PXI system can have up to eight slots per segment (1 system slot + 7 peripheral slots), whereas most desktop PCI systems only offer three or four available peripheral slots. Multiple-segment PXI systems built using PCI-PCI bridges offer this increased number of slots per segment making very high slot count systems possible (256-slot theoretical maximum). The capability to have additional peripheral slots is defined in the CompactPCI specification upon which PXI draws. Otherwise all of PCI's features transfer to PXI:

- 33 MHz performance
- 32- and 64-bit data transfers

- 132 MB/sec (32-bit) and 264 MB/sec (64-bit) peak data rates
- System expansion via PCI-PCI bridges
- 3.3 volt migration
- Plug-and-play capability

2.4 Software Features

Like other bus architectures, PXI defines standards that allow products from multiple vendors to work together at the hardware interface level. Unlike many other specifications, however, PXI defines software requirements in addition to electrical requirements to further ease integration. These requirements include the support of standard operating system frameworks such as Windows. Appropriate configuration information and software drivers for all peripheral devices are also required. Clearly, the PXI software specification is motivated by the benefits achieved through leveraging existing desktop software technology.

2.4.1 Common Software Requirements

The PXI specification presents software frameworks for PXI systems including Microsoft Windows. A PXI controller operating in either framework must support the currently available operating system and must support future upgrades. As a result, the controller will be able to use industry-standard application programming interfaces including LabVIEW, LabWindows/CVI, Visual Basic, Visual C/C++ and Borland Turbo C++.

PXI requires that all peripheral cards have device driver software that runs in the appropriate framework. Hardware vendors for other industrial buses that do not have software standards often do not provide any software drivers for their devices. The customer is often only given a manual, which describes how to write software to control the device. The cost to the customer, in terms of engineering effort, to support these devices can be enormous. PXI removes this burden by requiring that manufacturers, rather than customers, develop this software.

2.4.2 Other Software Requirements

PXI also requires certain software components to be made available by peripheral board and chassis vendors. Initialization files that define a system's configuration and capabilities are required for PXI components. This information is used by the operating software to ensure proper configuration of a system. For example, this mechanism is used to identify whether or not adjacent peripheral boards have a compatible local bus. If any information is missing, the local bus functionality cannot be accessed. Finally, implementation of the Virtual Instrument Software Architecture (VISA), which has been widely adopted in the instrumentation field, is specified by PXI for configuration and control of VXI, GPIB, serial, and PXI instruments.

3. Conclusions

PXI modular instrumentation makes sense because it defines an industrial computing platform for instrumentation users that clearly leverages the technology advancements of the mainstream PC industry. By leveraging the PCI Bus, PXI modular instrumentation systems can benefit from widely available software and hardware components. The software applications and operating systems that run on PXI systems are already familiar to end-users as they are already in use on common desktop PCI computers. PXI meets the needs of instrumentation users by adding rugged industrial packaging, plentiful slots for virtually unlimited I/O, and features that provide advanced triggering, timing, and side-band communication capabilities.

4.References

- *PCI Local Bus Specification*, Rev. 2.2
- *PICMG 2.0 R3.0 CompactPCI Specification*
- VXI*plug&play* Specifications (VPP-3.*x* and VPP-7)
- IEC 61326-1:1998, *Electrical equipment for measurement, control, and laboratory use—EMC requirements—Part I, General requirements*,International Electrotechnical Commission
- IEC 1010-1:1990 + A1:1992, *Safety requirements for electrical equipment for measurement, control, and laboratory use—Part 1, General requirements*,
- International Electrotechnical Commission
- IEC 60068-1, *Environmental testing*, International Electrotechnical Commission

5. Latest Revision of the Standard

Revision 2.1, February 4, 2003
This is the first public revision of the PXI specification.

6. Useful contact addresses

http://www.pxisa.org/ - PXI specifications
http://www.picmg.org/ PICMG specifications
http://www.ieee.org/ - IEEE specifications
http://www.iec.org/ - IEC specifications
http://www.pcisig.com/ - PCI specifications
http://www.vita.com/ - VME specifications
http://www.vxi.org/ - VXI specifications
http://www.vxipnp.org/ - VISA specifications

7. Application Note :- Pin electronics test and debug using PXI test station

Brian Foley, Staff Test Engineer
Fairchild Semiconductor, 333 Western Ave, South Portland, ME 04106

7.1 Introduction

Fairchild is one of the largest independent semiconductor companies focused solely on multi-market products. Fairchild designs, develops, and markets analog, mixed signal, discrete, logic, interface, optoelectronic, and non-volatile memory semiconductors. To test these products, Fairchild utilizes many test systems with different architectures and topologies. One of these testers, a 1980's vintage logic test system required upgrading due to maintenance and obsolescence issues. The system had 64-Pin Electronics Cards (PEC), each with one Parametric Measurement Unit (PMU) and one functional channel for a total of 64 tester channels. A new PEC, designed by Fairchild with the assistance of students and staff of the University of New Hampshire, needed a tester for debug, verification, and repair. The new PEC uses current industry standard ATE components to replace the older discrete designs.

The new PEC design, has four mini (low current ± 40mA) PMUs and one ± 500mA main PMU. The system wide reference levels for VIL, VIH, VOL, VOH, and threshold voltage have been replaced with per pin DACs for these functions, enabling per pin input and output functional levels. The number of functional test channels has also increased from one to four per PEC. This increases the total test channels from 64 to 256. This allows Fairchild to test up to four times more devices in parallel than the older system with better resolution and accuracy without any additional floor space requirements. The only other option would have been to purchase a new ATE tester at a much higher cost per system.

7.2 The test requirements

The new PEC cards require both analog and digital stimuli/response to perform an effective functional test. The PEC test set required the following signals. There are 64 Digital I/O Lines. The application requires up to 15 MHz Data and Clock Rate at TTL levels (Geotest GX5150 and GX5151 DIO, 6U PXI 50 MHz Data Rate). The Digital I/O is used to control and setup all functions and measurements of the PEC under test. All of the register loading, memory data and control, DAC and ADC control, and read back are performed using these two cards. They have a very flexible command set that allows all functions of the DIO to be reconfigured without having to load a new pattern file. This application uses some of these features:

- A blank pattern is written to memory on the first pattern load.
- The address, page, and data are written to each corresponding memory location.

The memory pointer is set to the start address of the same pattern and run, eliminating the need for additional patterns or pattern loads. Each DIO card can be used in either a read or write mode – this can be changed only when no patterns are executing. This method is used to read and write data to the bi-directional bus. A different memory location is used to load the read and write patterns, the card mode is changed, and the memory pointer set to the corresponding address. The following is a listing of the digital control signals that are used in this application (Digital I/O requirements for PEC debug and repair station):

- 18 Digital Control Lines
- 7 Digital Input Lines
- 16-Bit Bi-directional Bus
- 12-Bit Address Bus
- 4 Lines ECL to TTL and 3 Lines TTL to ECL Conversion (performed with logic conversion ICs)

7.3 Selected test equipment

128-Channel Scanner/Multiplexer:
Used to connect internal references, external power supplies, temperature sensors, and flying probe prober to the test system (GeoTest GX6264, 6U PXI). This multiplexer can be connected in several configurations, including 128 single-ended or 64 differential channels.

24 Relay Control Channels: Used to control resistive loads for force current; measure voltage, force voltage, current verification; power supply control and verification (National Instruments 6527 Optically Isolated Digital I/O, 3U PXI).

Using an optically isolated relay controller allows relays of different voltage levels and signals of different levels to be used in the same application. This also allows the use of external supplies to be used, removing the additional load on the chassis supplies, and eliminating the switching current of the relays from affecting the overall noise level of the system.

6 1/2 Digit Digital Multimeter: Used for accurate voltage, current, resistance, capacitance, impedance, frequency, and leakage measurement (Geotest SMX2044 6-Digit DMM/LCR, 3U PXI). The SMX2044 is not just a standard DMM. It also has functions most often seen only on LCR meters. It also has a force voltage – measure current function is useful for leakage measurements.

Other functions include pulse width, totalizer, temperature, 6 wire ohms, AC and DC voltage source, as well as DC current source.

16 Voltage References (DACs), 16-Bit resolution each: Used as external voltage references and calibration references (Alphi DAC 16, CompactPCI). This card was added to the test system to allow debug and verification of the older design PEC, which requires external references for input and output voltage,
voltage, current, and threshold levels. These DACs can also be used as reference and control voltages as needed.

Chassis/mainframe: A PXI Chassis with an embedded controller is used to accommodate the selected PXI cards (Geotest GX7000 6U PXI Chassis). The PXI chassis provides an internal hard drive, floppy, CD-ROM, and uses several PCI bridges to extend the PCI Bus up to 20 slots. Slot 1 is dedicated for either an embedded controller or a PCI to PXI remote controller card. In this application, an embedded controller is used to reduce system space (Geotest GX7900, 6U PXI). This controller has a Pentium CPU, VGA, Ethernet, serial, parallel, and USB ports. Flying probe prober with 1 mil (.001 inch) accuracy and camera for probe to PCB alignment: This prober was selected to enable testing of the very fine pitch surface mount components. A standard meter or oscilloscope probe is several times larger than the space between pads. This can result in shorted leads and device failure. The prober (Huntron ProTrack Prober II) also enables increased throughput using automation. This prober is both accurate and a small enough platform to be used as part of a bench-top test system. The prober is connected to both the DMM and Digital I/O through the scanner allowing the probe to be used to measure all functional, DC, and analog functions on the PCB under test.

7.4 External test hardware

The test instrumentation is connected to the PCB under test using two circuit boards that connect the 100-pin edge connector at one end and the spring probes on the other. The PCB on the edge connector side has all of the power supply control and measurement relays as well as the ECL–TLLand TLL–ECL translators. All signals have a protection circuit that consists of the series resistor and voltage clamp (Zener diode). This prevents a defective board from back driving signals or exceeding the maximum rated voltage for any of the I/O. This PCB also contains the two precision voltage references that are used to calibrate the main ADC of the board under test. The latches used for the low speed inputs on the board under test are also contained on this PCB.

The second PCB that is connected to the spring pins (load board connections) consists of several relays and precision resistors that are used to verify and calibrate both the mini and main PMUs. The DMM is used to verify accuracy and calibrate all voltage and current forces and measurements. The functional driver and loads are also verified and calibrated using this PCB. All functional input and output data from the functional drivers are cabled back to the Digital I/O cards for input and output data verification. The last function that is performed on this PCB is the load resistors that are used to simulate the maximum coil resistance of relays controlled by the open collector relay drivers. The scanner channels are used measure across each of these resistors in order to verify proper operation.

7.5 Why PXI was chosen over VXI or GPIB

To determine which platform would be most suitable for this application, Fairchild evaluated GPIB, VXI, and PXI with the following considerations:

- GPIB, while still a viable interface for certain applications, proved inadequate for this application due to data frequency, triggering, and integration requirements.
- Both VXI and PXI met the application requirements; therefore the selection came down to cost. AVXI system would have cost at least $20,000 more than its PXI equivalent.

Since that amount was nearly 100 percent more, the selection was easy.

7.6 The test program

The test program for this application combines several different types of equipment and interfaces. This includes the PXI and CompactPCI instruments, the prober, camera, and networking. All PCBs are tracked by serial number and date tested. This generates a running history of all boards that are tested and a database that is used to debug all future PCBs. This data is used to in an automated failure lookup table that will grow as more failures are debugged. Initially most cards will require a semi-automatic debug process of all test nodes to evaluate their normal signature.

The camera in the Huntron Prober is used to align the PCB to the flying probe. This is done using a two-point alignment, two targets are selected on the PCB and stored. The same two targets are then aligned on the board under test and global X and Yoffsets are generated. These offsets are used to correct for any variation in the PCB placement in the test fixture and variation from board to board.
All CompactPCI, PXI, and prober DLLs were used as received from the vendor. The DLL is simply added to the compiler along with the required files and that device is ready for use.

An untested PEC is first checked for shorts across all the power supplies to each other and ground. This is performed to prevent powering up a PCB with direct supply shorts that can damage the board itself and possibly the test station. If all supply connections pass verification, the board is powered up and the programmable gate arrays are programmed from an on-board EEPROM. The next step is a quick verification of all the subsystems to verify that they are all operational and accessible. Any subsystem failure will flag additional verification of that circuitry, when the quick verification is complete. The Huntron Prober test probe is then run though the circuitry comparing each node to its normal electrical signature. This could include any of the following: VAC, VDC, frequency, pulse width, duty cycle, capacitance, inductance, and functional pattern verification. The failure signature is then compared to failures of previous boards tested and a repair recommendation generated. This could include inspecting and reworking the board for possible solder shorts at a particular node, replacement of a failing part, or manual verification if the failure mode had not been encountered before. This is when the Sun-up PCB Viewstation is very helpful. The software can be used to show all connections to a failing node. These connections many times are on both sides of the PCB and can span the entire PCB. Manually tracking down these nodes using schematics is time consuming as the technician must keep referring to the schematic and assembly drawings in order to track down all connections to a failing node. This information is then added to the database so that any future failures of the same type are flagged for the same repair.

7.7 Software packages used in this test application include the following:

■ National Instruments LabWindows/ CVI. Used to write all C-based test and control code for the test system, as well as the GUI interface used to control and display all of the data including the camera image and PCB component and pad location.

■ Sun-Up PCB Viewstation. Used to view PCB layout files after conversion of Pads files. Indicates PCB device and pin locations, as well as all connections to a given node. The Viewstation is useful in PCB debug as all connected nodes can be viewed at once. This tool is also used to generate the X and Y coordinate list from the PCB layout file that is used by the prober.

■ Huntron PCB Converter. Converts PCB pads data file to X, Y, and Z coordinate files for Huntron Prober. ■ Huntron Control Software. Used to control both the prober and camera using a serial port for the prober and a custom interface for the camera.

7.8 Conclusion

This project has been the first use of a PXI or CompactPCI test system by our engineering department and likely not the last. The integration and operation of equipment from several different vendors was seamless, all equipment operational, and performed as specified. Fairchild will definitely consider PXI and CompactPCI instrumentation for future test requirements.

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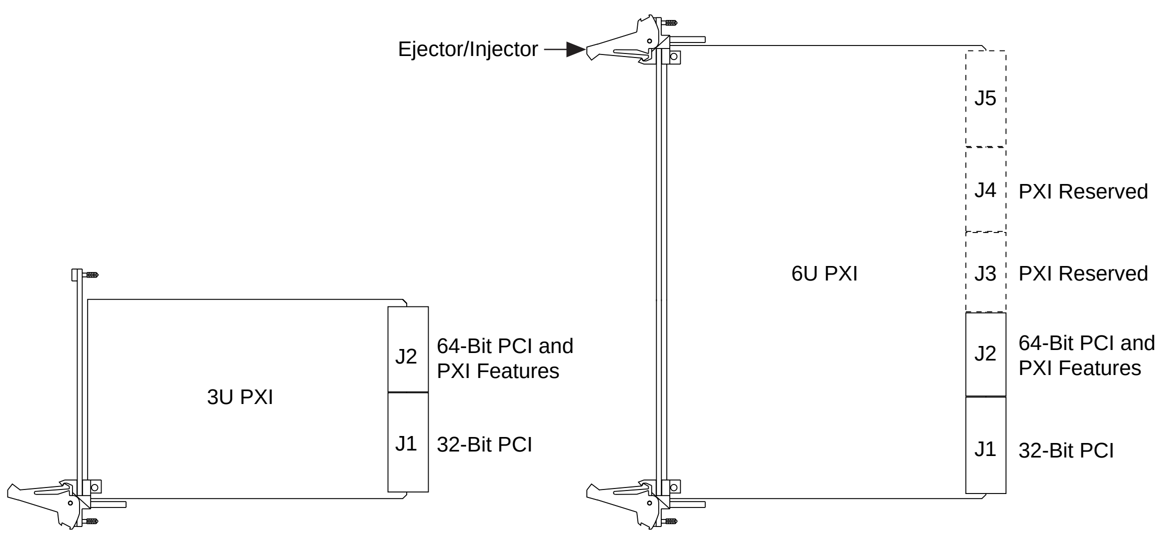

Figure 1. PXI Peripheral Board Form Factors and Connectors

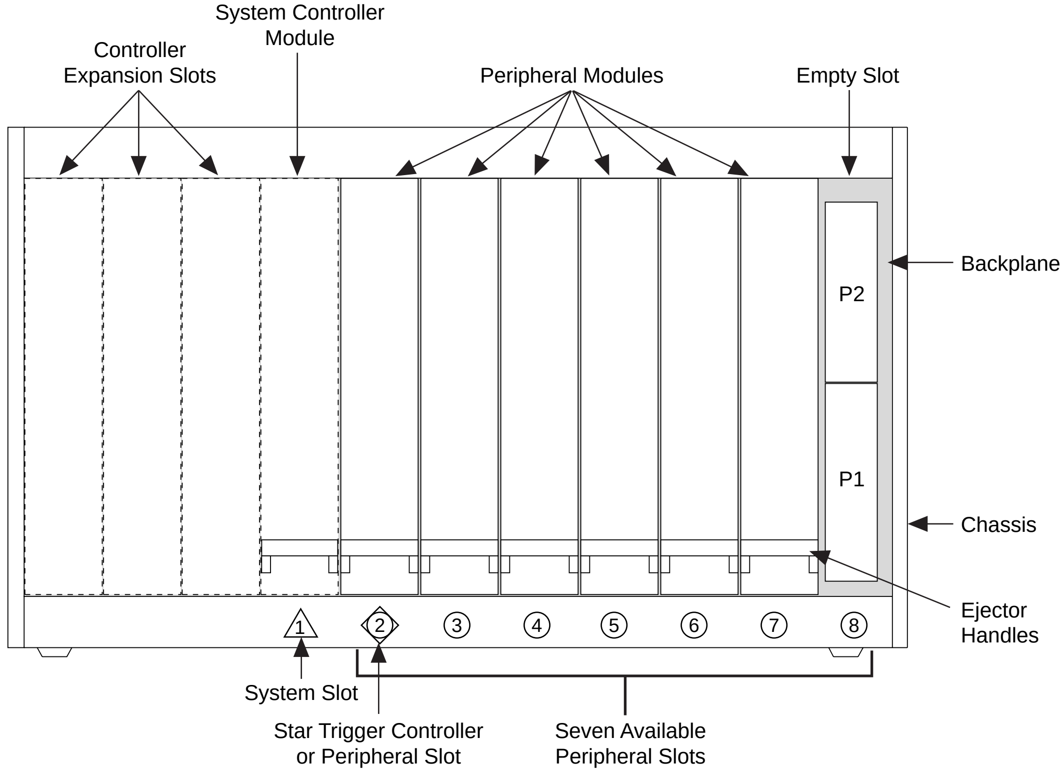

Figure 2. Example of a 3U PXI Chassis

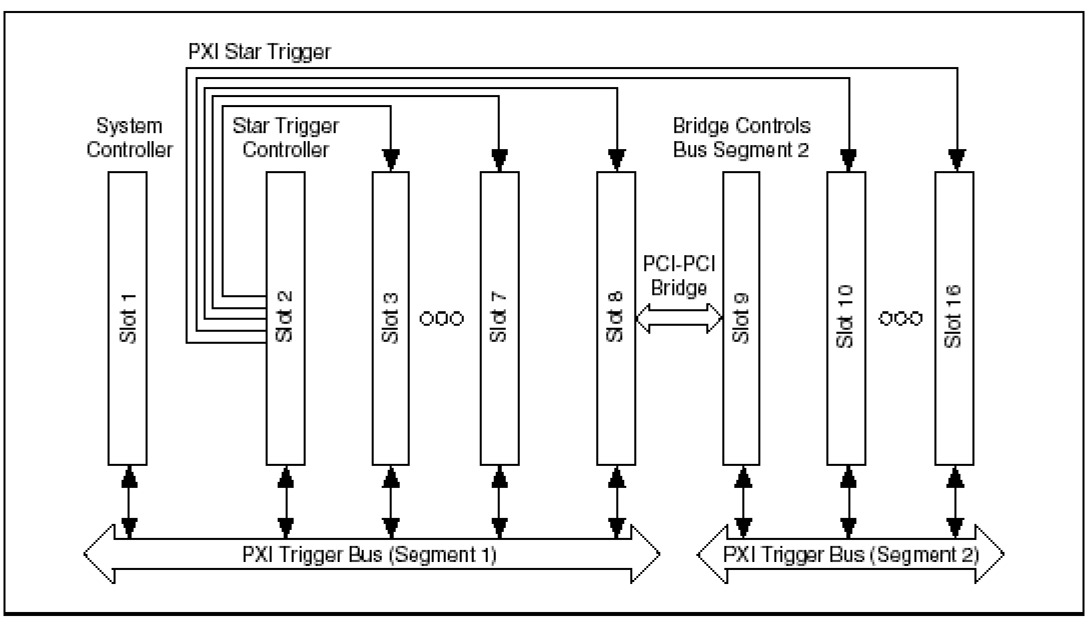

Figure 3. PXI Trigger Architecture for a PXI System with two bus segments

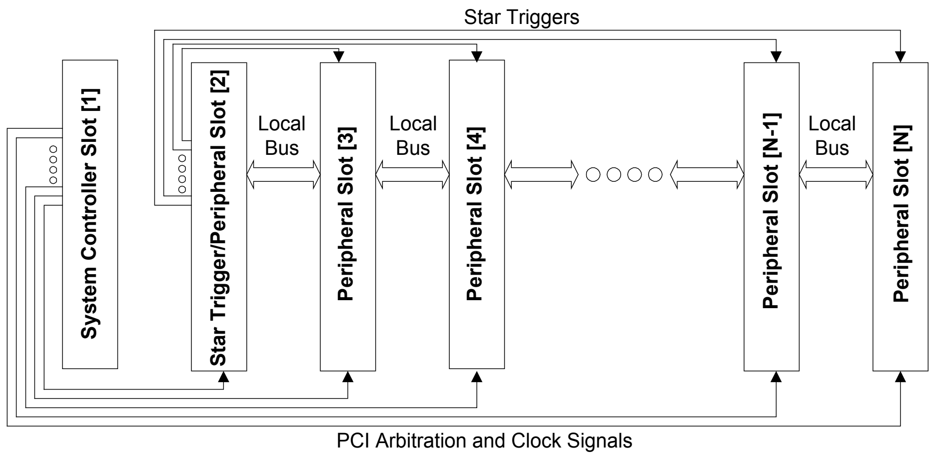

Figure 4. PXI Local Bus Routing