

# RIC/DICMOS-- Multi-channel CMOS Formatter

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## Abstract

*NPTest CMOS formatter, embedded within the new timing generation IC, can provide formatted levels and internal strobe markers for eight independent pin-electronics channels at up to 800 Mbps. The timing accuracy for both the formatted edges, and the strobe markers, is specified at +/- 81ps. The drive side minimum pulse-width is 1 ns, and the receive side can strobe pin-electronics comparator outputs as narrow as 800 ps. This paper describes the major features and operation of the new CMOS formatter.*

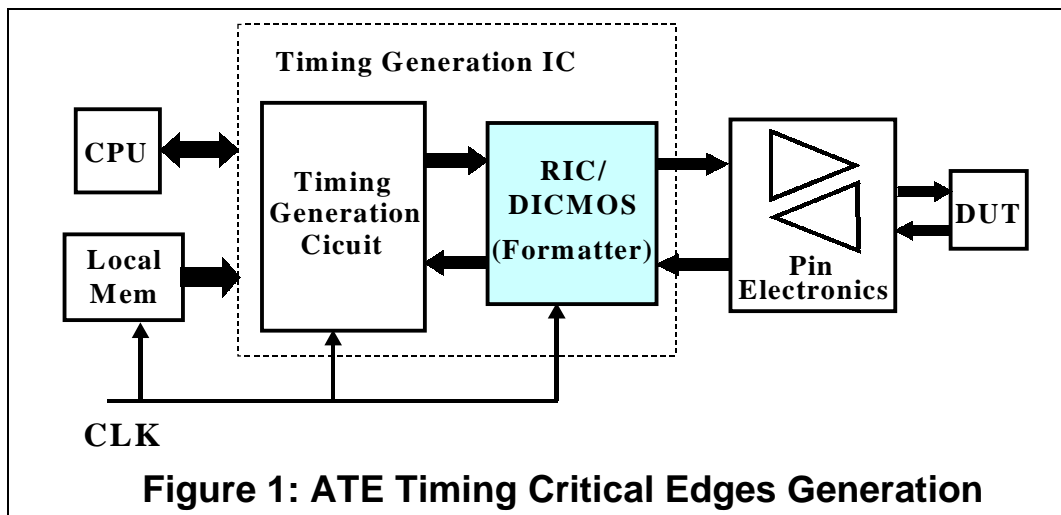
## 1 Introduction

Formatters play a crucial role in establishing the accuracy, and indeed, the functionality of a test system. Evolving system architectures, testing paradigms, and DUT specifications have posed new challenges and requirements on the design of timing critical circuitry. Pre-eminent among these requirements is the ability of current and future test systems hardware to bring the total cost of test down through better hardware integration and software support. Briefly, modern test systems hardware needs to be both modular and flexible. Judicious allocation of timing resources needed for the generation of drive and strobe edges, and the ability to utilize these edges for multiple channels, are few of the ways to achieve both flexibility and cost efficiency.

To address the issue of ever-rising cost-per-pin of testing complex devices with hundreds of pins, such as microprocessors and complex SOCs, a highly integrated architecture for "formatters" is proposed. Formatters [1], in the context of ATE hardware, pertain to a set of complimentary Drive and Response circuits (figure 1). Briefly, the Drive side generates accurate timing critical formatted levels required by pin-electronics to drive a DUT pin to a predefined logic state-- high, low or tri-state. The Response side, on the other hand, strobos the status of a DUT pin output, via the comparator block of the pin-electronics [2,3]. DUTs with high pin counts that need to be tested at speed, demand highly integrated ATE architecture to keep the overall cost of test low. Towards

achieving this goal, the new architecture includes eight independent embedded formatter channels inside the timing generator IC. In addition to avoiding the usage of discrete formatter ICs (which incur substantial penalties both in terms of design and development, time and cost), the resulting savings in PCB real-estate through the deployment of a combined timing generator-formatter IC have allowed for more functionality and higher fanout to be incorporated inside the testhead at a lower overall cost. Such an architecture is particularly suitable for functional and structural testing of high pin count SOC devices with I/O data rates of 800 Mbps (Mega bits per second) or below, and with less than +/-100ps EPA (edge placement accuracy) testing requirement.

Traditionally, in test systems architecture, Drive and Response ICs [4] are dedicated resources per DUT pin, configured to drive or strobe at some fixed (usually the system) frequency. On a variation to the theme, outputs of several Drive ICs are externally OR'd together to attain a higher edge rate required to drive a DUT pin. Similarly, external gating and muxing techniques are deployed to strobe high data rate signals coming off of a pin-electronics comparator using multiple Response ICs. However, NPTest new formatter named RIC/DICMOS (Response and Drive Circuit in CMOS), implemented in 0.18 micron CMOS process, simultaneously provide drive or strobe stimuli for up to 8 independent DUT pins at once. Each complimentary drive and response circuit pair is contained in what is called a "slice" within the timing generation IC. Furthermore, the eight slices can be independently software programmed to deliver formatted levels at upto 800 MTPS (Mega Transitions Per Second). Conversely, each slice can strobe the status of a DUT pin at upto 800 MTPS in both edge and window strobe modes. R4X/D4X [4], bipolar predecessors of RIC/DICMOS, do provide 800 MTPS drive and strobe channels per discrete IC pair. On the other hand, RIC/DICMOS provide eight such channels integrated inside one timing generator IC, while occupying one-twentieth the area (compared to an equivalent eight R4X/D4X pairs) on the PCB.



In this paper a description of RIC/DICMOS is followed by a discussion of how the new formatter accomplishes its task of producing timing critical edges necessary for the accurate production of drive levels or strobe markers. An overview of the impressive new specifications and simulation results is also included in the end.

## 2 Physical Description and Operation

### 2.1 DICMOS

DICMOS (figure 2) consists of the following main components--

- Eight Independent Run-time Interface blocks called Event Logic Interface or ELICIF
- Thirty-two Independent Tapped Delay Elements (TDLEs) or "barrels"
- A Drive Logic Block
- Two Timing Measurement Unit Multiplexers (TMU-MUXs).

#### 2.1.1 ELICIF

During run-time operation at 400MHz, two 8 bit half-words are transmitted over successive clock cycles from the timing generation IC core to each of the eight ELICIF blocks. The thirty-two 8-bit (parallel) run-time data access ports to DICMOS are labelled as DA0..3, DB0..3, DC0..3 and DD0..3 in figure 2. Buses DA, DB, DC and DD carry 8 bits of delay data, 2 bits of event type[1:0] and 2 status bit called "tag." The "tag" bits signal the end of a digital word. The four LSB delay data bits received in the second half of the timing word are ignored, as they represent timing resolution finer than the minimum delay step size that can be achieved by DICMOS. Essentially, ELICIF decodes the timing delay information (8 bits) as well as the event type (2 bits) needed to generate the desired formatted level, DHI/DINH (see table 1). In calibration mode (see section 3), ELICIF also generates the

necessary trigger pulses and or levels to control the built-in delay line auto-calibration circuit.

Type[1:0]	Description
0 1	Tri-state (DINH = 1)
1 0	Drive Low (DHI = 0)
1 1	Drive High (DHI = 1)

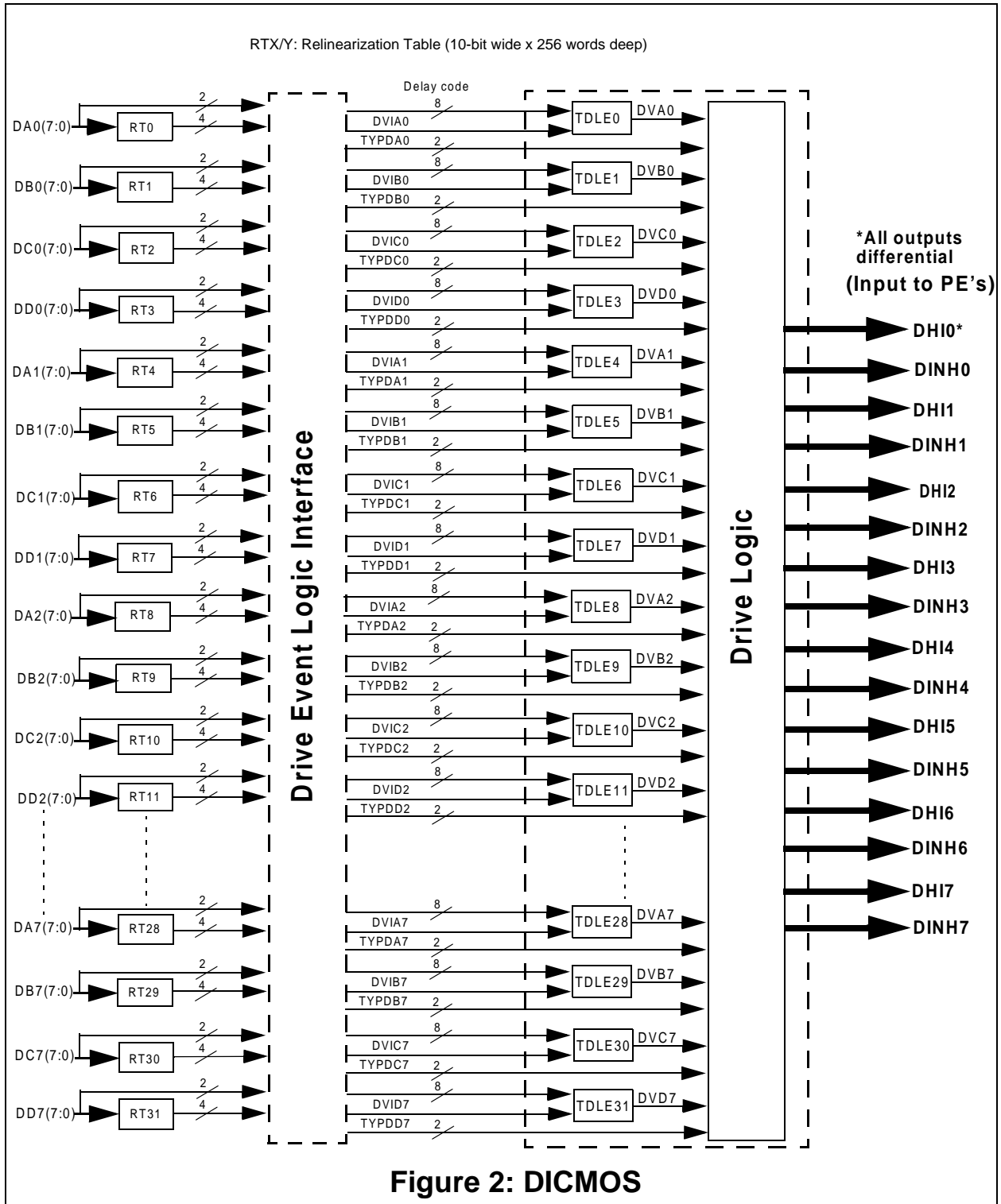
**Table 1: DICMOS Event Types**

#### 2.1.2 Tapped Delay Line Elements (TDLEs) or "Barrels"

Each TDLE can move edges in approximately 20 ps steps between the edges of a 385 MHz--420 MHz system clock. It generates timing markers in response to the delay and event type information relayed to it by the ELICIF. Each TDLE consists of a string of PVT (process, voltage and temperature compensated) buffers to provide coarse (~200ps) "taps" for delays, and a timing interpolator circuit to generate ~20.833ps fine time intervals. The delay value is extracted by ELICIF from the 12-bit run-time word. Initially, the run-time delay values generated in the timing generator core are used to "look-up" delay codes in reallinearization tables (RT) that in turn allow a TDLES to generate the correct timing step. The retrigger rate for each TDLE is 4 ns.

#### 2.1.3 Drive Logic block

DICMOS provides formatted drive levels for eight independent PEs. This implies that four barrel (or TDLE) outputs are merged to form a single pair of formatted levels named DHI and DINH. Each 2-bit run-time event type is decoded as either one of the internal markers setdhi, resetdhi, setdinh or resetdinh (see figure 4). DHI and DINH can be as narrow as 1 ns wide pulses. The maximum data rate for these signals is 800 MTPS, delivered



to the pin-electronics with an edge placement accuracy of +/-81 ps or better, with respect to the master clock driving the timing generation IC. Either the rising or the falling edges of the formatted levels can be moved in steps of 20ps over a delay range of 0-2.5 ns. Alternatively, the DHI and DINH levels can also be "forced" at the

output(s), by setting appropriate bits in a software register called PECONTROL. This feature is activated during the calibration of pin-electronics.

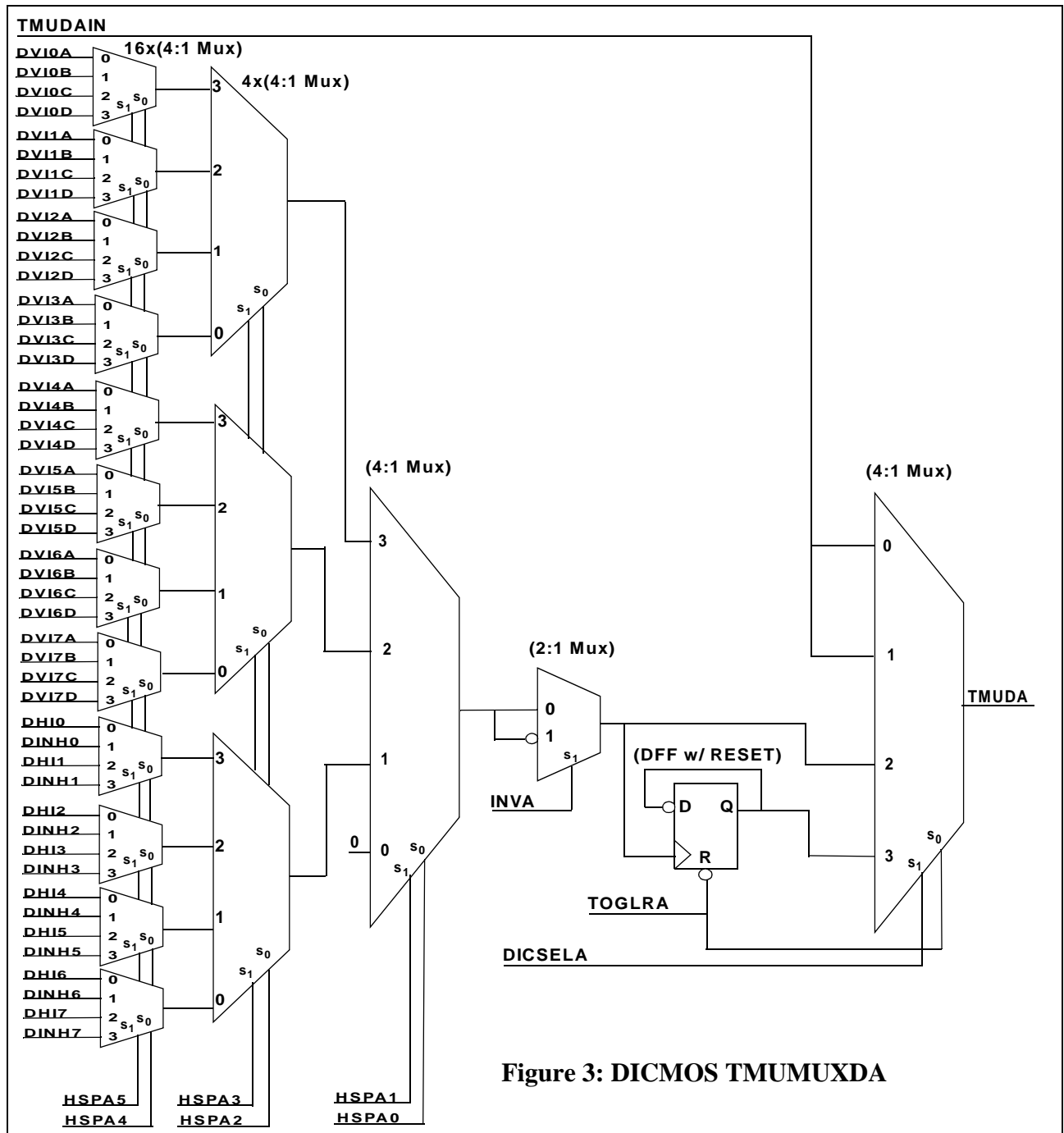
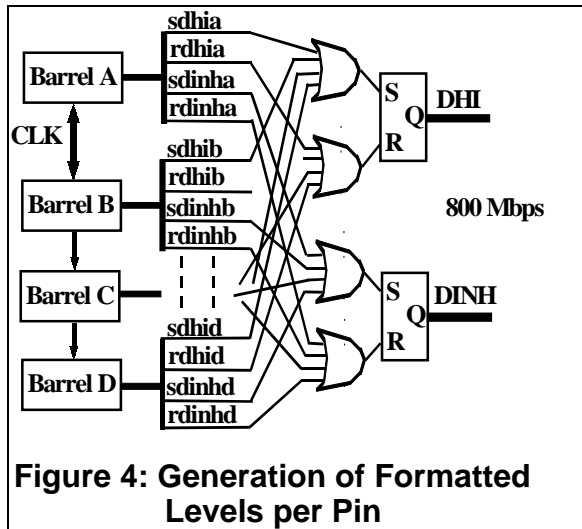


Figure 3: DICMOS TMUMUXDA

### 2.1.4 TMUMUXs

DICMOS contains two high speed TMUMUXs for the purpose of high speed system diagnostics. In figure 3, one of the two drive side muxes, TMUMUXDA, is shown. The two outputs, TMUDA and TMUDB, are supposed to be routed to an off-chip TMU (Timing Measurement Unit) where their edge or marker locations can be measured with a high degree of accuracy and resolution. The toggle flipflops located after the last layer of 4-1 muxes select either the very short pulses or generate

levels whose edges are timed by them. The DHI/DINH levels are routed through the muxes in such a way that the toggling can take place on either their leading or their trailing edge. Extreme care was exercised during the layout phase of DICMOS to match on-chip propagation delays for all internal TDLE markers (DVO\*), which routed are through TMUMUXDB (not shown), and their triggers (DVI\*), shown in figure3, to preserve accuracy and to assure proper marker alignment under various PVT (Process Voltage Temperature) conditions.



**Figure 4: Generation of Formatted Levels per Pin**

## 2.2 RICMOS

RICMOS (figure 5) consists of--

- Eight Independent Run-time Interface blocks called Event Logic Interface or ELICIF
- Thirty-two Independent Tapped Delay Elements (TDLEs) or "barrels"
- A Strobe Logic Block
- Two Timing Measurement Unit Multiplexers (TMUMUXs)

### 2.2.1 ELICIF

RICMOS uses exactly the same ELICIF circuit as DICMOS (see section 2.1.2). Run-time data for RICMOS (CA, CB, CC and CD), however, consists of delay values associated with strobe marker generation. And the event type extracted from the 12 bit word contains the information whether the marker to be generated is StbOff, StbZ, StbLo or StbHi.

Type[1:0]	Description
0 0	Strobe Off
0 1	Strobe Z
1 0	Strobe Lo
1 1	Strobe Hi

**Table 2: RICMOS Event Types**

Strobes cause a pass or fail according to the state of the compare signals at strobe time:

- Strobe Z passes if ACH is a 0 and BCL is a 0 during strobe time, else causes a fail
- Strobe Lo passes if BCL is a 1 during strobe time, otherwise causes a fail
- Strobe Hi passes if ACH is a 1 during strobe time, otherwise causes a fail

erwise causes a fail

Note that if both BCL and ACH are 1, either Strobe Lo or Strobe Hi will pass - this is normally an invalid condition.

### 2.2.2 TDLEs

RICMOS shares exactly the same TDLE architecture, as DICMOS, and the operation is alike, as well, except that the TDLEs generate strobe markers instead, in response to the timing delay values received from ELICIF.

### 2.2.3 Strobe Logic Block

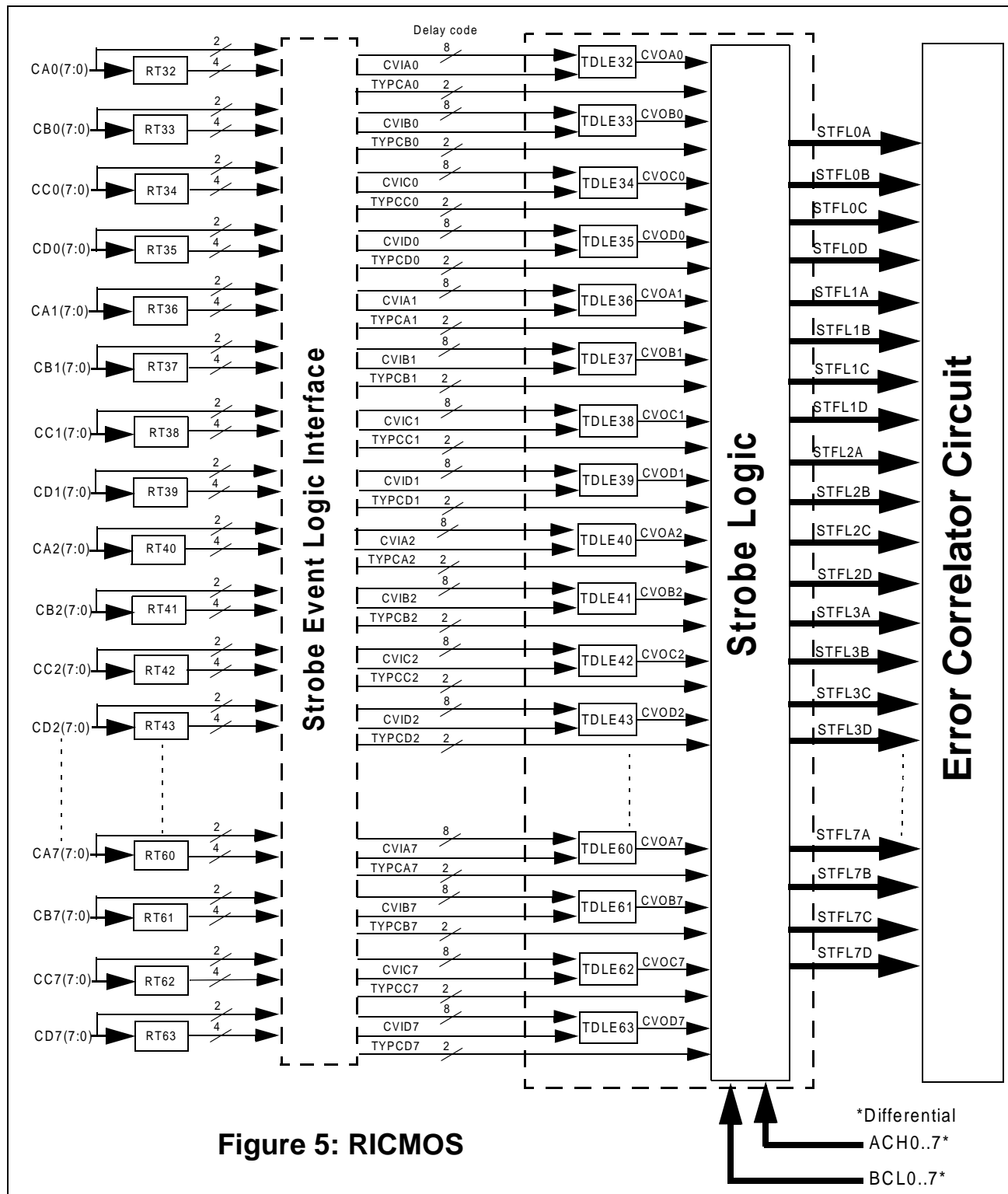
RICMOS receives outputs ACH (Above Comparator High) and BCL (Below Comparator Low) from pin-electronics comparator(s). At the same time, it uses event type information and the strobe markers generated by the TDLEs in response to the run-time data, to sample ACH and BCL signals. If the state of these signals is different from that which is indicated by the event type, a "fail" signal is generated. Figure 6 demonstrates how similar event types from the four TDLEs are merged together to strobe ACH/BCL outputs from a pin-electronics comparator corresponding to a DUT pin.

RICMOS is capable of comparing outputs (ACH/BCL) from up to eight independent DUT channels, in both edge and window strobe modes. Moreover, any combination of pins can be strobed in either window strobe or edge strobe mode. In edge strobe mode, for a given DUT pin, the leading edge of the TDLE output pulse, CV0X (X=A,B,C,D) decides pass or fail. Fails are associated with the TDLE channel which caused the strobe. In window strobe mode, however, the TDLE channel receiving the strobe-off event reports a pass or fail which occurred on any one of the other three TDLEs prior in time. The strobe events can occur simultaneously on all four TDLEs during edge strobe mode. The minimum time separation between a "Strobe-On" (Strobe-Hi, Strobe-Lo or Strobe-Z) event and a "Strobe-Off" event must be greater than or equal to 800ps in window strobe mode. Additionally, pulses as narrow as 800ps on ACH/BCL lines can be compared for an expected pass or a fail in window strobe mode.

The four fail outputs, one per TDLE, are called STFLX (X=A,B,C,D). These run-time fail signals are correlated with the events in the timing generator circuit, so that the user can obtain a comprehensive event-by-event pass/fail information about the test.

### 2.2.4 TMUMUXs

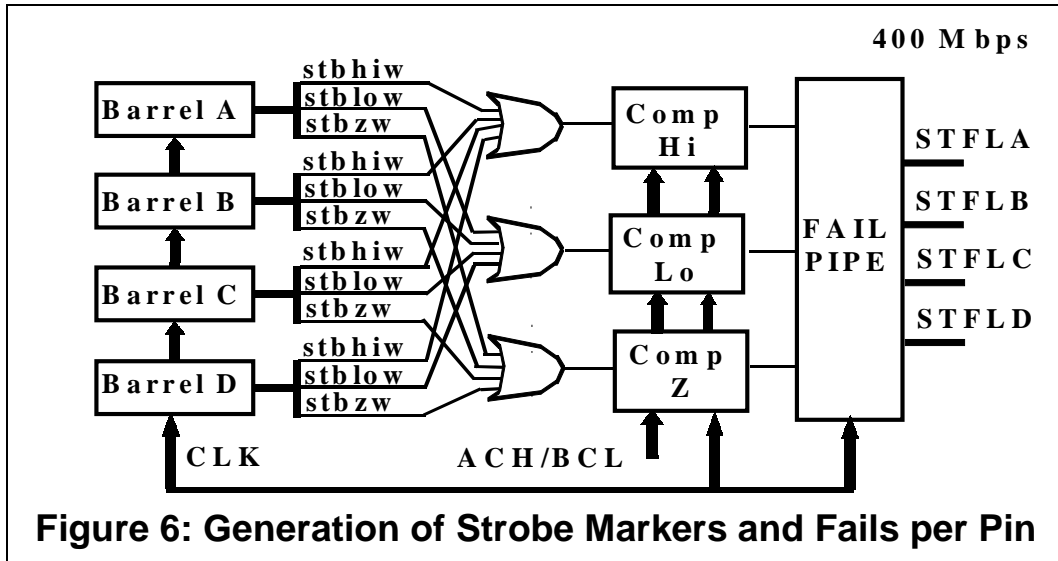
The two RICMOS TMU muxes, TMUMUXCA and TMUMUXCB, have a similar architecture to that shown in figure 3 for DICMOS. In addition to providing observability for internal timing critical signals, the muxes can also be selected to pipe out run-time event failures for di-



agnostic purposes. In "loop-back" mode, DHI/DINH signals generated by the complimentary DICMOS circuit are internally looped-back onto the strobe-side, for a first-level, self-diagnostic validation of the drive and response-side functionality and timing accuracy.

### 3 Auto-calibration

Programmable delays are established by connecting eight TDLEs in a loop, for a total of eight loops per RIC/DICMOS (64 TDLEs). The loops are triggered (see figure 7a) when the ring oscillator bit (RINGO) inside a lo-



cal register is asserted, and an event to start oscillation is received. The ring oscillator output is directly connected to an on-chip gate/event counter circuit for highly accurate time measurements (see architecture below). Actual TDLE delay is estimated to range from about  $0.9ns$  to about  $1.4ns$  under all program conditions. So the loop delay is estimated to be from about  $7.2ns$  to about  $9.7ns$  (assuming all TDLEs except the one being calibrated are set to their fastest position). The resolution of the time measurement is determined by the programmable width of the gate counter. Registers GATECOUNT and EVENTCOUNT are used to set the counters to a predefined count value, prior to commencing calibration. Upon reaching the desired gate count, the event counter shuts off and the time count value is dumped into off-chip capture memory. For diagnostic purposes, current gate and event count can always be obtained by reading back the contents of registers GATECOUNT and EVENTCOUNT, respectively.

In calibration mode, bit settings for the delay line elements are auto generated via a state machine which adds the contents of the register TDLEOFFSET to that of TDLEINIT (figure 7b). Both of these registers are loaded during chip setup, prior to calibration. For each of the

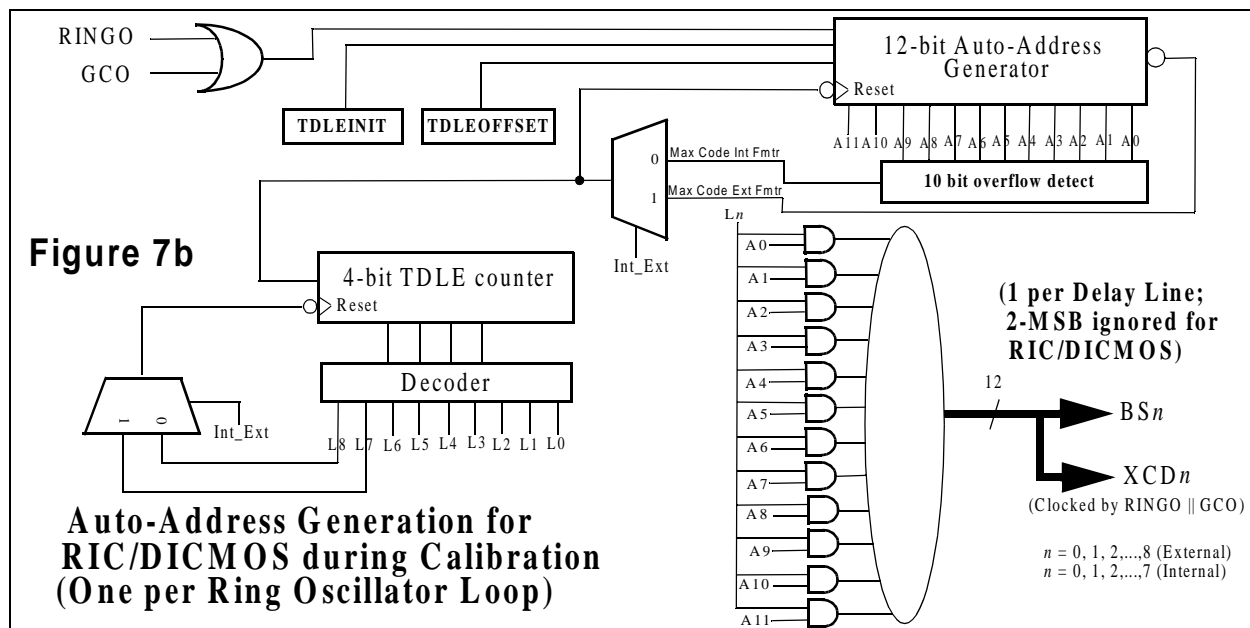
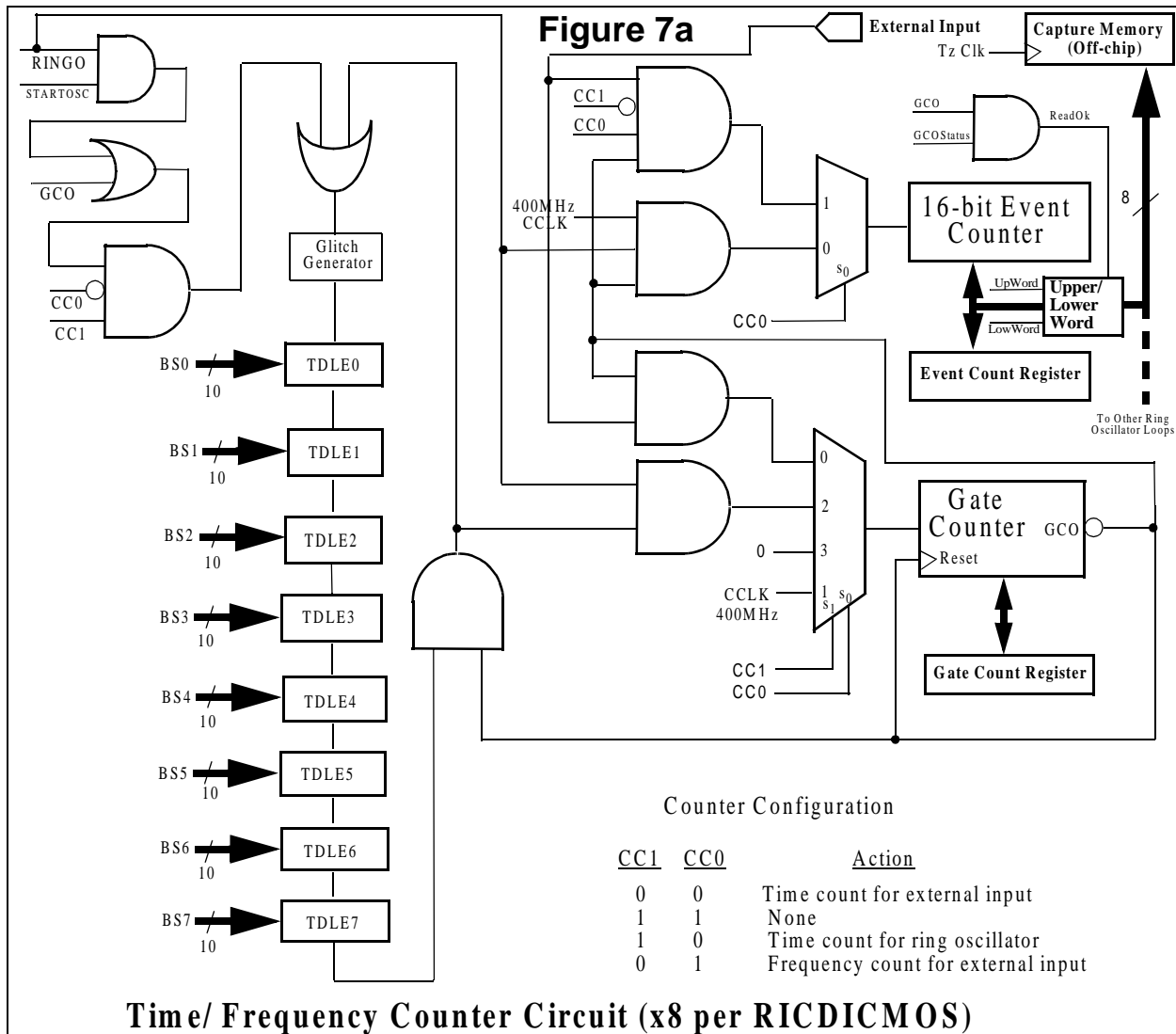
TDLEs, the state machine advances the bit settings by the offset amount till the last bit combination is achieved. This process is sequentially repeated for all of the delay lines inside the loop. In case of RIC/DICMOS, once the “raw” event-count time values are linearized by software, the delay codes corresponding to the 256 out of 1024 linearized time values (spanning 0-- $2.5ns$ ) are transferred back into the relinearization tables via CPU bus using block writes.

To estimate how long it would take to acquire data for calibration, assume that each TDLE has a total of 10 selection bits and produces binary delays for each of the bit settings. If the minimum and maximum propagation delays are  $0.9ns$  and  $1.4ns$  (obtained via SPICE simulation over all relevant PVT conditions), respectively, then the resolution of the delay line is given by approximately  $r=0.4883 ps/bit$ . Now, each TDLE except the one which is being calibrated, is set to its minimum delay setting (900ps). Then, the time required to acquire the delays for all 1024 ( $2^{10}$ ) values using a 14 bit gate counter is given by,

$$T_{acquire} = \sum_{k=0}^{k=2^{10}-1} 2^{14} (7 \cdot (900) + (900 + 0.4883k)) ps \quad 0.097s$$

Since there are 8 TDLEs in a loop, the total time required for acquiring data is simply  $8 \times 0.097s = 0.776s$ . Furthermore, since there are eight such independent loops per RIC/DICMOS, it will still take  $0.776s$  to acquire data for all of the TDLEs when calibrated in parallel. Indeed, it would take exactly  $0.776s$  to acquire TDLE data for the

entire system, when all timing generation ICs in the system are calibrated in parallel. This scheme improves the overall calibration data acquisition time by a factor of 500. It is important to note that this estimate for acquisition time doesn't take into account data transfer off chip, or transfer of relinearized data from CPU to the relinear-



ized tables. Also, with a 14-bit gate counter, a resolution of  $0.61\text{ps}/\text{count}$  (or, equivalently,  $1.64\text{ counts}/\text{ps}$ ) can be achieved.

The delay time counts stored in the capture memory are sorted and linearized between 0 and  $2.5\text{ns}$  by the software. Prior to run-time operation, for each of the TDLEs, the linearized delay values along with their corresponding bit settings are uploaded onto relinearization tables (figures 2 and 5) inside the timing generation IC. During runtime operation, user generated delay values (with a resolution of  $20\text{ps}$ ) are compared with the entries in the look-up tables to pick out the delay line bit settings which would most closely yield the programmed delay value.

### 3.1 Generalized Use of Gate and Frequency Counters

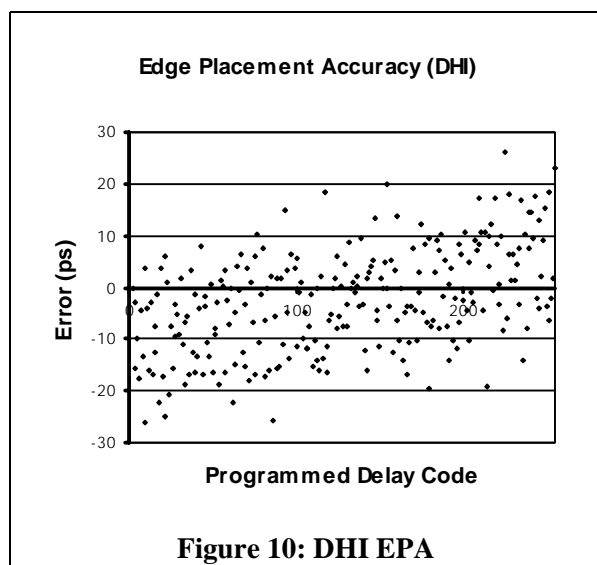
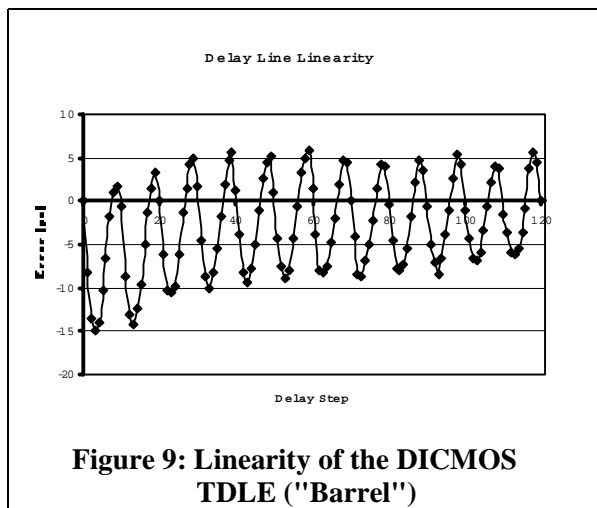
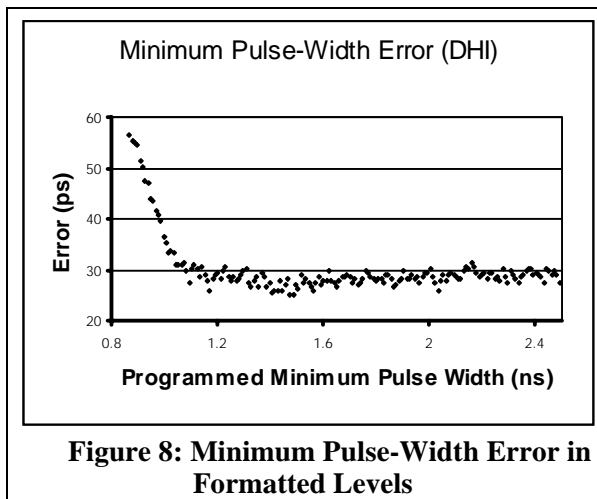
Apart from measuring the loop delay during the calibration of TDLEs, the gate/frequency counter arrangement can also be used to provide either an frequency or time count for an arbitrary input signal. In diagnostic/calibration mode, register CNTRCONFIG is used to select either the external signal or the ring oscillator output for measurement purposes. The table in figure 9a shows the usage of the gate/event counter for various bit settings of the register CNTRCONFIG. For a RIC/DICMOS with 8 independent ACH/BCL input pairs (which can be alternatively used as pads for accepting signals from external sources during calibration), up to 8 independent external signals can be routed to each of the eight gate/frequency counter circuits (4 for drive side and 4 for compare side) inside RIC/DICMOS. Depending upon CNTRCONFIG bit settings, either a frequency or a time count value can be transferred to the off-chip capture memory or stored in register EVENTCOUNT for read back.

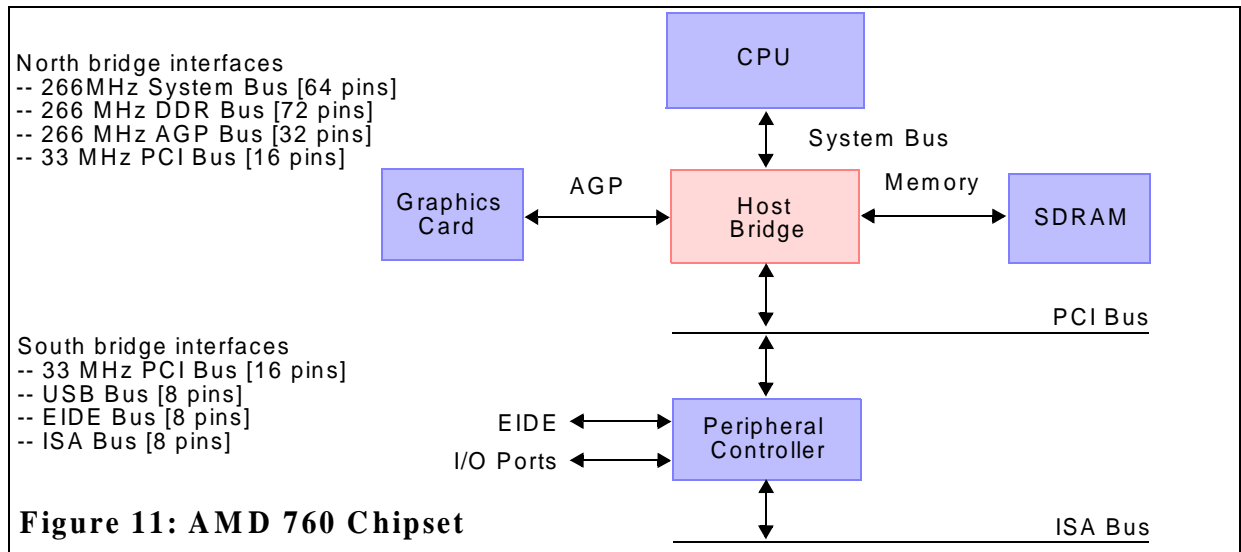
## 4 Simulation Results

Currently, RIC/DICMOS is in layout phase, with critical SPICE simulation results (figures 8-10) showing worst-case DHI EPA (Edge Placement Accuracy) of  $\pm 40\text{ps}$ . Also, the uncalibrated delay step-size has a monotonicity of  $\pm 1/2\text{ LSB}$ . TDLE linearity shows a repetitive error of  $\sim 15\text{ps}$ , due to the type of circuit architecture deployed.

## 5 Applications and benefits of high fanout formatter

Many chipsets such as Advanced Micro Device's AMD760 [5,6] require that different pins be tested at different frequencies (see figure 11). The North bridge interfaces that include the system bus and the PCI bus, require tests to be run at 266 MHz, and South bridge interface has drive and strobe requirements at 33 MHz. Thus, for testing 168 high speed (266 MHz) and 56 low





speed (33 MHz) pins, just 28 RIC/DICMOS pairs are required.

Another typical example is of nVidia's NV2A graphics processor used in the Microsoft XBox Video Game System. This is a logic device with 418 signal pins. Functional test vectors need to be run at 245 MHz, with some very large scan patterns at 5 MHz, as well. In order to accommodate the testing requirements of the moderate pin-count of the device, toggling at moderate frequencies, RIC/DICMOS provides unparalleled integration, with an associated reduction in test hardware cost, and at an edge placement accuracy of below +/- 81ps.

It is cost effective for test systems manufacturers to design their custom ICs with foresight such that the ICs support a wide array of architectures, both present and near-future, than develop ASICs (that have, at least, a two year design time frame, and carry millions of dollars in NRE and engineering costs) that are utilized specifically for a targeted application, and are then rendered useless soon afterwards due to incompatibilities with evolving architectures. RIC/DICMOS formatter was designed to meet the present and future needs of both low cost functional and structural test market segments, where the system level edge placement accuracy is of the order of +/-150ps.

## 6 Conclusion

RIC/DICMOS is a 800 Mbps drive and response circuit implemented in 0.18 micron CMOS, contained within NPTest new timing generator IC. Its eight independent drive and strobe channels provide high fanout on testhead PCB, yielding dense hardware integration and an overall cost savings, without compromising the +/- 150 ps system EPA required of low to moderate cost test

systems. RIC/DICMOS auto-calibration scheme is an innovation which allows the linearity of new formatter's delay elements to be determined at least 500 times faster than its predecessors'.

## 7 Acknowledgments

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## 8 References

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