Testing High Frequency ADCs and DACs with a Low Frequency Analog Bus

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Abstract

As the sampling frequency of new ADCs and DACs increases, it gets more difficult to accurately convey the analog stimulus or response to or from the converter under test – there is a bandwidth bottleneck. This paper describes a technique that uses a <100 kHz analog bus, such as the standard 1149.4 bus, to convey an arbitrary analog signal, and converts the signal to or from a high frequency at the converter, on-chip. This permits existing low-frequency distortion tests, both ATE-based and embedded, to be used for high frequency converters. High frequency noise is easily filtered out, permitting a more repeatable test and the use of low cost testers. A hypothetical 100 MHz, 14-bit ADC and DAC are used as examples. The technique has reduced sensitivity to sampling jitter, and 16~18 bit linearity appears feasible.

1. Introduction

The testing of low frequency (LF) analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) for differential non-linearity (DNL), integral non-linearity (INL), and total harmonic distortion (THD) is a standard procedure in integrated circuit (IC) testing. Some automatic test equipment (ATE) has standard software routines for these tests – an analog or digital-equivalent linear ramp or sine wave stimulus is generated and the voltage increment associated with each least significant bit (LSB) change is measured, or the level of harmonic frequencies is calculated. However, as the speed of IC converters increases above 50 MHz, and as their resolution simultaneously increases above 10 bits, these standard tests are more difficult to implement accurately. In addition, converters may be embedded in the middle of a system-on-chip (SOC) so that high quality, low-impact access is difficult and expensive.

A number of built-in self-test (BIST) techniques have been proposed. Early approaches, such as HBIST [1] and adcBIST [2], propose a complementary ADC and DAC, and do not measure DNL and INL. Oscillation BIST [3] uses analog feedback to measure DNL and INL, requires active analog test circuitry on-chip, and is not suitable for sigma-delta converters. MADBIST [4] and its more recent versions [5][6] require a large number of shift register elements (>8K bits) for sigma-delta stimulus generation, and a digital signal processor (DSP) for response analysis. Sigma-delta signal generation methods are limited to a few tens of megahertz for >10 bit resolution and reasonable clock rates, unless 4th-order or higher band-pass filtering is used (which adds area and diagnosis issues).

High frequency (HF), high resolution ADCs typically have relatively low, process-sensitive, input impedance, <5 kΩ [7], so passive filtering of digitally-generated waveforms is not suitable – a high speed analog buffer is needed, which introduces distortion, area, and diagnosis issues. High speed DACs often require low impedance loads, <100 Ω tied to a ground, and their voltage range sometimes has minimal overlap with a sigma-delta ADC's mid-rail-centered input voltage range. These issues are significant problems for BIST that uses constant-current driven capacitors for ramp generation [8][9], or feedback-based DAC tests [10].

While THD tests of high-speed converters may be more representative of functional performance in the intended application, it may not be very diagnostic – it does not indicate what part of the converter circuitry is defective. DNL/INL tests are more diagnostic but are less representative of at-speed functional performance if a simple linear ramp or DC-servo method is used, because the ramp increments are necessarily small. A high speed, highly linear, analog ramp would be more representative but is difficult to generate accurately and is more difficult to convey to/from the converter-under-test because a limited bandwidth path degrades a ramp's linearity – in effect, there is a bandwidth bottleneck.

The notorious high cost of mixed-signal ATE is a contributor to IC test costs, however, analysis of this cost is useful for learning how to reduce it. The cost of industrial-grade sub-100 kHz, 16~24 bit converters can be less than \$50, and DSP chips costing less than \$20 are available. Therefore, the expense of mixed-signal ATE must be attributable to *other* factors:

- a high signal-to-noise ratio (SNR) must be achieved in the presence of many high-speed digital signals;
- analog stimulus frequencies must be a precise fraction of the digital clock frequencies;
- ATE analog circuitry must be faster and more accurate than the (latest technology) circuits to be tested;
- a controlled-impedance (50 Ω) switch matrix is required to deliver the waveform to an arbitrary pin for high frequencies, and separate force/sense channels are needed for low frequencies;
- adjustable bandwidth low pass filters are needed;
- the tester may also have many high-speed digital channels.

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Reduced pin-count (RPC) testing has been proposed [11][12] to facilitate low-cost testing of high pin-count ICs – especially because it can facilitate multi-site testing. These techniques contact between 10 and 64 digital pins. Access to the analog pins associated with ADC inputs and DAC outputs usually requires dedicated access pins and mixed-signal ATE channels, which can prevent or significantly reduce the cost advantages of multi-site testing.

This paper describes a way to test high speed, high accuracy ADCs and DACs via a single, LF analog bus. Minimal digital circuitry is added on-chip, and no on-chip active analog circuitry is added. The techniques permit existing LF converter tests to be re-used for HF converters, for IC or board-level testing.

2. Overview of the new ADC test

Multiplexing is a well known way to combine two signals to produce a single higher frequency signal, and many testers use this technique to produce digital output rates higher than the data rate of a single ATE channel. Analog multiplexing is possible, of course, by combining multiple DAC outputs, but this does not solve the bandwidth bottleneck problem mentioned earlier, nor does it reduce multi-site loadboard complexity.

The block diagram of Figure 1 shows how multiplexing can be used to produce a high frequency analog test signal on-chip: a low frequency signal, such as a ramp or sine wave, is supplied by a tester via a low frequency analog bus, and a DC voltage is supplied from an on-chip analog ground. The on-chip analog multiplexer can be a simple pair of relatively low-impedance CMOS transmission gates. The multiplexing is performed synchronously to the ADC's sampling clock, at half the Nyquist sample rate of the ADC, so that every second output sample from the ADC will correspond to the low frequency ramp or sine wave. Digital samples can be shifted off-chip via scan access, at a relatively low, under-sampled rate, for conventional off-chip analysis.

For example, consider testing a 100 MHz, 14-bit ADC. From the tester's perspective, the ADC can appear as a low frequency ADC: the ATE applies a rail-to-rail linear ramp or cycles of a 1 kHz sine wave, and monitors a serialized digital output at 14 bits per microsecond (14 Mb/s) – test time for 64K samples is 65 ms plus DSP time to perform a fast Fourier transform and calculate THD, SNR, etc.. Coherent sampling is discussed later.

From the ADC's perspective, it is receiving an at-speed analog waveform that changes by as much as half (or more) of its full range between samples. Every 100th 14-bit output sample of the sine wave is latched and shifted out serially to the tester as a digitally-encoded 1 kHz sine wave, or every 2nd sample of a linear ramp is latched and accumulated on-chip for 50 samples (100 clock cycles), and the average is shifted out each microsecond.

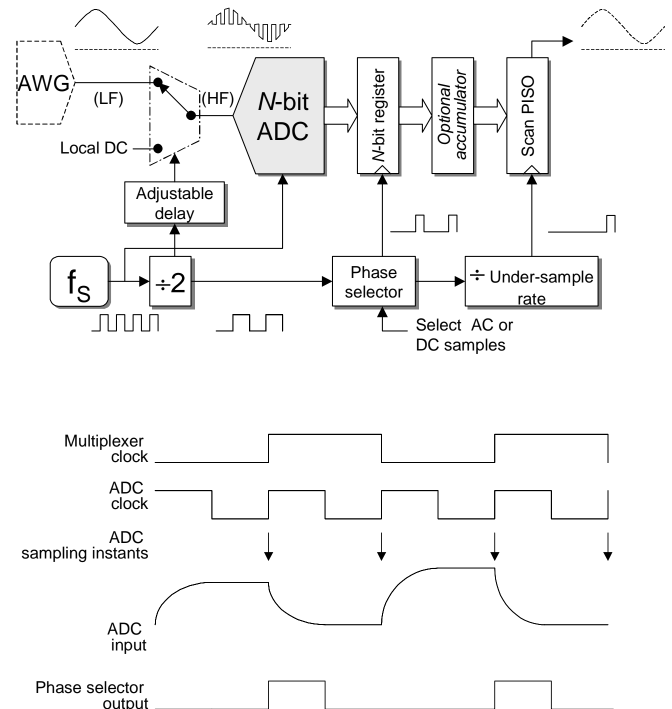


Fig. 1 ADC test access block diagram, and waveforms

For ADCs that have an input impedance less than 500 kΩ (i.e., <1000 times that of the CMOS transmission gates used for the multiplexer), a sampled force/sense scheme must be used, as will be discussed later.

2.1 Details of the ADC test

The tester supplies a high quality, low frequency signal. Because it can be less than 10 kHz, 16-bit test accuracy is inexpensive and available on many low cost testers. The generator could also be an on-chip sigma-delta signal generator, or an on-chip pulse-width modulator. The analog signal is then conveyed to the converter under test via a single-ended or differential analog bus – many converters can be tested via the same bus, though not simultaneously. When parallelism is essential (when test time per converter is deemed too long), then multiple buses and stimulus generators are necessary.

The analog multiplexer is located as close as possible to the input of each converter under test, to minimize the parasitic load capacitance. If the converter's functional input is a pad, the pad can be driven by the bus, and no off-chip connection (and tester channel) is needed for that pad. The DC input signal can be an analog ground voltage mid-way between V_{DD} and V_{SS}, any other convenient DC voltage, or an on-chip programmable DC voltage (which does not need to be accurate, but should be stable).

The selector input to the multiplexer is driven by a digital clock with approximately 50% duty-cycle and a frequency of one half the ADC's Nyquist sample clock frequency. For converters with high input resistance (R_{ADC} =1 MΩ), and low input capacitance (C_{ADC} = 1 pF), a multiplexer with R_{MUX} = 500 Ω on-resistance will introduce a time constant of 500 ps, or 5 ns for 10 time constants. This is theoretically sufficient for testing converters with F = 100 MHz and N = 12 bits accuracy. Generally,

$$F_{MAX} = 1/(10 \times R_{MUX} \times C_{ADC})$$
$$N_{MAX} = \log_2(R_{ADC} / R_{MUX}) - 3$$

The achievable accuracy at a chosen ADC sampling frequency is limited by the ratio of the multiplexer transmission gate's series resistance to the ADC's input impedance.

For lower input resistances, higher frequencies, or more bits of accuracy, a sampled force/sense scheme is necessary in which the conventional force/sense access provided in ATE is extended into the IC-under-test using the analog buses, as shown in the schematic of Figure 2. A capacitor (and possibly a high value resistance) is connected between the force and sense lines to provide a closed-loop (negative feedback) when the multiplexer is selecting its other (DC) input – a typical PMU already has this feedback capacitance for stability. In addition, the multiplexer is designed so that the selector signal is actually two non-overlapping clocks, and the force path switch is enabled before the sense path switch (but both are disabled at the same time), as shown in the waveforms of Figure 2.

The simulation performed to obtain the waveforms of Figure 2 was performed using publicly available 0.5 um CMOS Spice parameters [13], and an ideal op-amp with an open loop gain (A_{OL}) of 80 dB, unity gain frequency of 160 MHz, zero offset, 10 MΩ input impedance, and 10Ω open loop output impedance. The multiplexer's n-channel transistors were 8/0.6 µm/µm, and p-channel transistors were 24/0.6, to give approximately 1 kΩ small-signal resistance (V_{DD} = 3V). The feedback capacitor was 100 pF, and the analog bus capacitance to ground was 100 pF. None of these parameters are "high" performance. The ADC input is modeled as 1 pF in parallel with 5 kΩ to $V_{DD}/2$. The output waveform, as seen in the 1000X magnified view of Figure 2, settles to 0.12 mV above the input voltage – this source of error is discussed later.

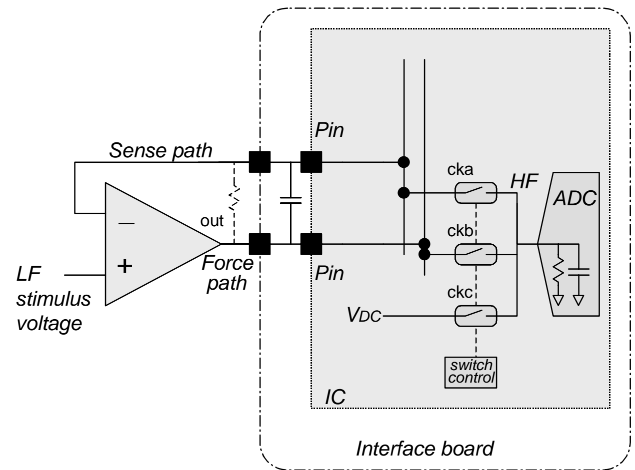
The LF bandwidth of this circuit is dependent upon the multiplexer switch's on-resistance (force path + sense path: $R_{MUX} = R_{SWa} + R_{SWb}$), the force/sense feedback capacitance (C_{FB}), and the duty cycle of the feedback clock pulse.

$$f_{LF-3dB} = 1/(2\pi RC) = 1/ (2\pi R_{MUX} (T_S/\tau)\, C_{FB}) = \tau /(2\pi R_{MUX}\, T_S\, C_{FB})$$

where T_S is the sampling period (twice the ADC's sampling period), and τ is the feedback path's clock pulse width. For example,

if f_{SAMPLE}= 100 MHz, T_S=20 ns, τ = 7 ns, C_{FB} = 100 pF, and $R_{MUX} = 2 \times 1k\Omega$,
then $f_{LF-3dB} \approx 280$ kHz.

This frequency corresponds to one RC time constant, but it takes 11 RC time constants to settle to 16-bit accuracy, so the usable frequency range is much lower than the –3dB bandwidth.



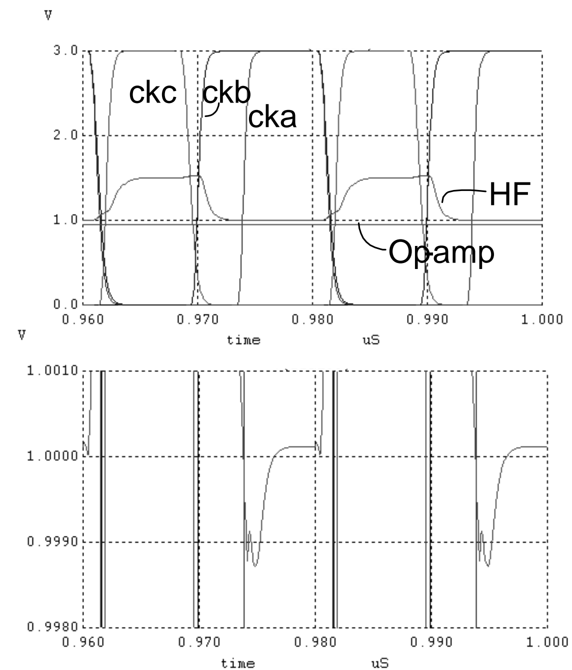


Fig. 2 Example ADC test access, and simulation voltage waveforms, for 1V stimulus and 1.5V DC (bottom waveform is HF signal with vertical-axis magnified 1000X)

The waveforms of Figure 2 are for a feedback capacitance of 100 pF. The waveform for 500 pF is very similar. The gain error is approximately equal to $(V_{IN} - V_{DC})/A_{OL}$, where A_{OL} is the open loop gain of the op-amp at the low frequency. If an off-chip op-amp is used, then its gain and unity gain frequency can be very high. In any case, finite open loop gain only introduces a closed loop gain error which can be accounted for.

When a ramp stimulus is used, the accumulated average of samples (50 in the above example) can be analyzed on-chip to calculate the DNL and INL. A variety of algorithms are possible, including those that are noise sensitive, because of the large amount of averaging that can be performed at each step before calculating the non-linearity error. For example, the DC servo loop method can be used [26].

The achievable accuracy at a chosen ADC sampling frequency, when the sampled force/sense scheme is used, is limited by:

- clock-coupling effects from the transmission gates, which can be minimized by using smaller, matched n-channel and p-channel capacitances, and by using fast clock edges (so that the op-amp has no time to react);
- the series impedance of the force-path transmission gate, which, for a given gate-to-channel capacitance, can be decreased with each technology shrink;
- the op-amp's open loop gain at the low frequency, which can be maximized by using an off-chip op-amp.

Figure 3 shows the uncompensated full-range linearity, summarized from Spice simulations, for two different resistive loads (in parallel with 1 pF): the 5 kΩ case is more representative of a mostly capacitive input, and 1 kΩ is more representative of a resistive input. A larger feedback capacitance and smaller transmission gate resistance provide better linearity; for the 5 kΩ example 100 pF and 500 Ω were used, respectively. Figure 3 shows 15 bits linearity (within 90 μV of a best-fit straight line, over a 3 volt range) for both the 1 and 5 kΩ examples. Reducing the signal range improves the linearity – in this case, in excess of the V_{DD}~V_{SS} range was used, assuming an off-chip op-amp. The central 75% of the range achieves 16 bits linearity.

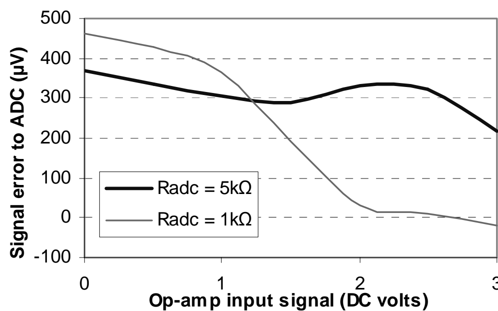


Fig. 3 Linearity of ADC input force/sense circuitry

The applied DC voltage, V_{DC} in figure 2, can also be applied with a force/sense scheme to ensure that it has higher accuracy and minimizes inter-sample interference. For ADCs with differential inputs (the typical case), the inverted version of the low frequency analog signals can be substituted for the DC voltage.

3. Overview of the new DAC test

The multiplexing principle described for the ADC can also be applied to testing a DAC.

As shown in Figure 4, on-chip digital multiplexing can be used to produce a high frequency digital test signal: one multiplexer input is a digitally-encoded low frequency signal (a ramp or sine wave) supplied serially by a tester, and the other input is a constant digital value. The output of the DAC is sampled by a simple, relatively low-impedance CMOS transmission gate. Again, multiplexing is performed synchronously to the converter's Nyquist sampling clock rate, at half the sample rate of the DAC, and the analog output from the DAC is sampled for one half clock cycle (or less), every second clock cycle, so that the output will correspond to the original low frequency ramp or sine wave. The output of the sampling transmission gate is connected to the on-chip (and off-chip) analog buses for conveying to the ATE for conventional DSP analysis.

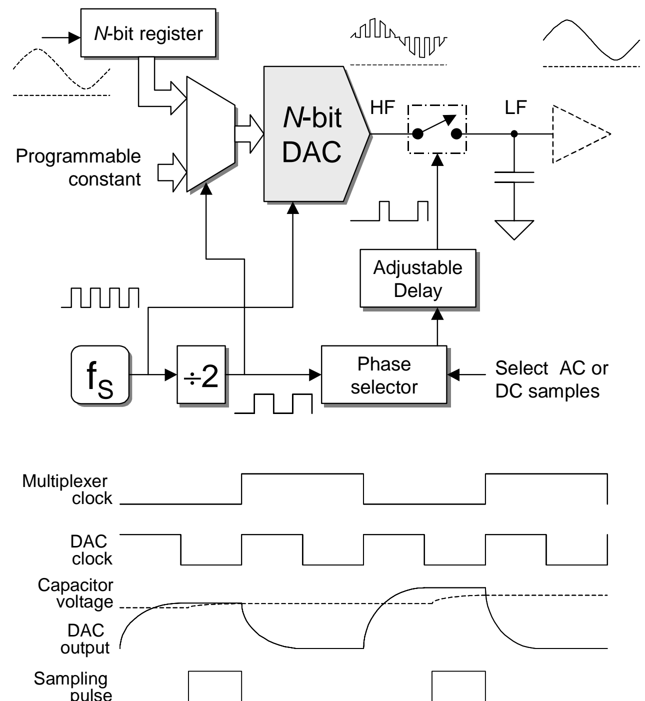


Fig. 4 DAC test access block diagram and waveforms

From the DAC's perspective, it is receiving digital words that change by as much as half (or more) of the full range between samples, at-speed. The analog output is sampled every 2nd cycle of the 100 MHz clock, by the

transmission gate and storage capacitance of the analog bus. High frequency noise is filtered out by the bus capacitance (>50 pF when connected to off-chip bus) and by the tester's anti-alias low pass filter.

Similar to the ADC test example, consider testing a 100 MHz, 14-bit DAC. From the tester's perspective, the DAC can appear as a low frequency, 14-bit converter: the ATE applies a bit stream corresponding to a digitized rail-to-rail linear ramp or cycles of a 1 kHz sine wave, via a scan chain, and the ATE samples a low frequency analog bus signal output.

3.1 Details of the DAC test

The tester shifts in digitally-encoded samples of a sine wave or ramp. In the case of a ramp, the stimulus is generated entirely on-chip using a binary counter whose parallel outputs are connected directly to the multiplexer at the input to the DAC. The other data input to the multiplexer is a register containing a constant value (that is programmable via scan), or the constant value could be pre-determined and implemented by combinational logic gates, thus saving a shift register and eliminating the digital multiplexer. The selector input to the multiplexer is an approximately 50% duty-cycle clock that has a frequency of one half the DAC's Nyquist sample clock frequency.

The output of the DAC is sampled by a CMOS transmission gate, whose n- and p-channel transistors are designed for equal capacitance to minimize charge injection into the channel. The technique of sampling a high speed signal using an analog switch and capacitor was first described in [14] and extended to use off-chip capacitance in [15].

As stated in [15], the maximum bandwidth for the low frequency signal (and its harmonics) is limited by the sampling switch's impedance, the bus capacitance, and the sampling pulse width:

$$f_{BUS_3dB} = 1/(2\pi RC)$$
$$= 1/\left(2\pi R_{SW} \left(T_S/\tau\right) C_{BUS}\right)$$
$$= \tau /(2\pi R_{SW}\, T_S\, C_{BUS})$$

where R_{SW} is the switch resistance (incl. R_{SOURCE}),
T_S is the sampling period,
τ is the pulse width, and
C_{BUS} is the bus capacitance.

For example,
if f_{SAMPLE}= 50 MHz, T_S=20 ns, τ = 5 ns, (25% duty cycle), C_{BUS} = 100 pF, R_{SW} = 1kΩ,
then $f_{BUS_3dB} \approx$ 400 kHz.

Again, it takes 11 RC time constants to settle to 16-bit accuracy, so the usable frequency range is much lower than the –3dB bandwidth. The maximum sample frequency is primarily limited by the CMOS process technology, and is almost always higher than the DAC under test.

An important limitation is the accuracy at high speed: the accuracy is limited by the transmission gate's charge injection and non-linear series resistance, and by the current leakage in the storage capacitance (the analog bus) between sampling instants, but these appear to mostly cause a gain error.

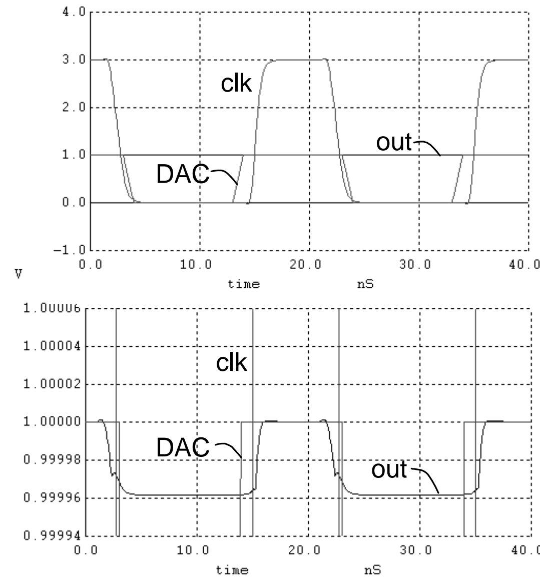


Fig. 5 Example DAC test access, and simulation voltage waveforms, for 1V stimulus and 1.5V DC (bottom waveforms have vertical-axis magnified 10,000X)

Figure 6 shows the uncompensated full-range linearity, summarized from Spice simulations – note that the vertical scale is in microvolts, and that the average of the "out" waveform of Figure 5 is used. The switch resistance was approximately 1.3 kΩ, using equal sized n- and p-channel devices and 100 pF bus capacitance. The sample rate was 50 MHz, with 50% duty cycle, corresponding to a 100 MHz DAC. Figure 6 shows 18 bits linearity (within 10 µV of a best-fit straight line, over a 3 volt range).

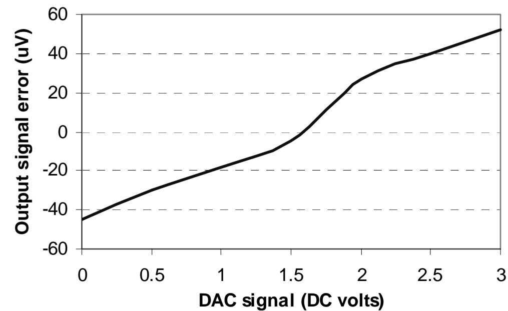


Fig. 6 Linearity of DAC output sampling circuitry

4 Using the 1149.4 analog test bus

The IEEE 1149.4 Standard for a Mixed Signal Test Bus [18] specifies an analog extension to 1149.1 digital boundary scan [19]. Briefly, 1149.4 simply adds two analog buses to an IC that has 1149.1 (JTAG) boundary scan, and routes them to some or all of the IC's pins, as shown in Figure 7, so that an analog stimulus signal can be applied to each pin, and an analog response signal can be measured at a pin, possibly the same pin.

The two analog buses facilitate the use of force/sense access. For testing with differential signals, four analog buses can be used.

Although the ADC/DAC test technique presented in this paper can use any analog bus, the IC area to implement analog access is minimized if the same analog bus is used to perform other tests, including those that 1149.4 was originally intended for. Multiple analog buses and access pins can be used if more parallelism is needed in the test (e.g., testing multiple converters simultaneously).

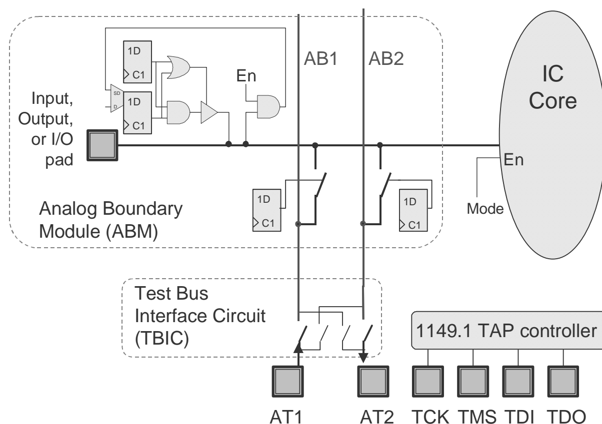


Fig. 7 1149.4 circuitry: ABM, analog buses, TBIC, TAP

5. Hardware verification

A demonstration board was constructed, containing a 24-bit ADC with maximum sampling rate of 40 kHz, a 16-bit DAC with maximum sampling rate of 100 kHz, an 1149.4 chip (available from National Semiconductor in sample quantities [15]), and an FPGA.

The clock and data to the 1149.4 device, ADC, and DAC are supplied by the FPGA which is clocked by a 25 MHz crystal oscillator and PLL.

The sampling switches are in the 1149.4 device. There is only one sampling clock input to the switches in the device, so the staggered timing of the force/sense access is not possible.

Hardware test results are not yet available.

6. Discussion

Coherent sampling is always necessary when analyzing sine wave characteristics with DSP [20]. Briefly stated, the ratio of analog stimulus frequency to the sampling frequency must be equal to the ratio of the number of analog stimulus cycles to the number of samples collected, and the numerators and denominators must be relatively prime. Typically, a sine wave is applied to a converter-under-test at a frequency approximately equal to one eighth of the sampling frequency, to represent an at-speed stimulus and to capture the 2nd and 3rd harmonics in-band. However, with the LF scheme described in this paper, any small prime number of sine wave cycles can be used – this simplifies achieving coherency.

Coherent sampling is also required when analyzing a ramp's linearity [20]. The scheme presented in this paper permits any small prime number of low speed ramps to be used instead of many high frequency ramps.

Distortion and noise that is caused by each input sample's value being affected by the preceding sample value can be measured by measuring the 'crosstalk' between samples. Instead of collecting the output samples that correspond to the ramp or sine wave, the samples that correspond to the constant DC value can be monitored, by changing the sampling clock phase by 180º. Excessive presence of the sine wave in the DC result indicates imperfect function, and very low levels are easily measured because the frequency is very low, the output amplitude of the fundamental frequency is very small, and all noise and interference is filtered out. Sampled force/sense may be required to ensure the DC value is delivered accurately to the ADC, as mentioned earlier.

For high speed, high resolution converters, jitter is a primary source of noise [16]. For example, when sampling a sine wave having an amplitude of 1 volt, the signal changes by $2\pi f$ volts/second. This is equal to 300 μV/ps at the zero-crossing for a 50 MHz signal, which corresponds to almost 2 LSB for a 14 bit, 3 volt converter. Typical sampling jitter for a high speed converter is between 0.2 and 1 ps RMS [7]. For the test technique described in this paper, a sampled sine wave is applied, not a continuous sine wave, and therefore the result is less sensitive to sampling jitter and may not correlate well with the jitter-induced noise results for a high frequency continuous sine wave. On the other hand, this facilitates diagnosis of the converter's noise sources and permits repeatable test results when the jitter is difficult to minimize (such as in wafer-level testing). It is very difficult to deliver or measure sub-picosecond jitter in production testing. The jitter for an ADC could be tested by moving its sampling point to the transition part of the waveform (of figure 2) instead of the plateau.

Adjustments in the phase of the sampling instant and pulse width can be made using an on-chip, self-calibrated digital delay line, for example, to permit measurement of the signal transition characteristics, however its jitter must be accounted for.

The non-linearity that is evident in the graphs of figures 3 and 6 could be cancelled using various techniques. For example, it can be compensated by pre-characterizing (once per chip) the linearity using a known input signal, as done in [17], or the non-linearity canceling technique of [24] could be used.

The bandwidth of the ADC test is limited by the non-zero width of the output sampling pulse – a larger bandwidth is possible using a clocked comparator, but that approach is more sensitive to noise, and requires active analog circuitry which must be tested.

The new technique is suitable for testing embedded converters in the middle of an SOC because only a low frequency analog bus conveys the signal, and the result is low pass filtered, so bus routing is non-critical. For a converter whose analog signal is a pad signal, the analog multiplexer can be placed between the converter and the pad, or the (possibly un-probed) pad can be connected to the on-chip low frequency analog bus. At the board-level, a converter on one chip can be tested via an analog bus that connects it to an embedded tester on another chip (especially with the 1149.4 analog bus).

If we re-visit the reasons for the high cost of mixed-signal testers, we can see that the solution presented in this paper addresses them.

- a high signal-to-noise ratio (SNR) must be achieved in the presence of many high-speed digital signals – the new approach uses a low pass filter whose corner frequency can be <10 kHz and thus filters out most digital noise;
- analog stimulus frequencies must be a precise fraction of the digital clock frequencies – the stimulus frequency can now be the master clock divided by an integer power of 2 because only a single sine wave cycle needs to be sampled;
- ATE analog circuitry must be faster and more accurate than the (latest technology) circuits to be tested – the ATE can now use 10 kHz converters and hence much higher resolution is cheaply available;
- a controlled impedance switch matrix is needed – for sub-10 kHz signals, controlled impedance is unnecessary;
- adjustable bandwidth filters are needed – the low frequency stimulus can usually be the same frequency, regardless of the converter under test, so fewer filters are needed;
- many high-speed digital channels – the RPC techniques described in previous papers regain their cost-effectiveness when the analog test capabilities can be implemented using a single, low frequency access bus instead of dedicated access to all high frequency analog pins.

This method is complementary to various BIST schemes. It allows low-cost delivery of high frequency buffered analog stimulus to various points on an IC, and expects that the input resistance (not to be confused with impedance, which includes capacitance) will be a significant factor. Most BIST schemes assume input resistance is >10 MΩ, and thus require additional buffering. As mentioned in the introduction, when a sigma-delta bit-stream is used to distribute digitally-encoded analog signals [6], low-pass or band-pass filtering is needed at the input to the ADC, and so the input resistance of the ADC becomes part of the filter – therefore highly linear, high speed buffering must be added. The force/sense scheme described in this paper can avoid per-converter buffering. Other published embedded stimulus generation techniques that generate a relatively low frequency analog stimulus [8] [21] can be combined with the technique of this paper to generate a high frequency stimulus.

Some ICs that contain an ADC or DAC also provide multiplexed analog access to the converter so that multiple analog channels can be converted, though this is rare for the high performance converters that are the subject of this paper (because such multiplexing adds series impedance and requires additional testing). For medium performance converters that already have these multiplexers, implementation of this new test scheme is simplified. Note that the force/sense multiplexer described in this paper permits a multiplexed ADC to also achieve higher speed and accuracy in function mode.

The 1149.4 standard for a mixed-signal test bus is primarily intended for accessing pin signals, but is also intended for test access to mixed-signal functions on-chip. The typically low-frequency bandwidth of this analog bus, and most analog buses, and the use of medium-impedance (1 kΩ) switches, are not well suited for the low impedances and high frequencies associated with high speed converters. The new force/sense scheme largely overcomes the switch impedance issue. The economic justification for using 1149.4 is difficult if the analog bus is only used for analog boundary scan [22], however, when the benefits of lower cost testing of high speed ADCs and DACs, and minimum pin-count access test of digital pin DC parameters are added, then the benefits can easily exceed the area cost. In fact, *any* analog bus access can derive many of these benefits, and analog buses are used on many ICs [23].

The maximum converter frequency that can be tested is limited by the clock pulse width, edge rate, and gate-to-channel capacitance, all of which improve with smaller geometry processes.

An ADC's sampling noise will be included in the under-sampled output, and can be measured while performing the fast Fourier transform (and accounting for the under-sampling). Noise due to clock jitter can be detected by using an independent clock to perform the analog multiplexing at the input to the ADC under test. By using a narrow sampling pulse to sample a DAC's output, as mentioned earlier, the characteristics of the signal slewing between samples can be measured.

However, a DAC's output noise will be filtered by the analog bus capacitance – this appears to be a fundamental limitation. A more detailed analysis of noise and jitter will be the objective of future work.

8. Acknowledgement

The author is indebted to Aubin Roy for many stimulating discussions and constructive feedback.

9. Conclusions

This paper presents a simple, very low cost method [25] for testing high speed ADCs and DACs. A single low frequency analog bus conveys the analog signals, and high-speed multiplexing and de-multiplexing is performed on-chip as close as possible to the converter-under-test. In essence, the multiplexing/ demultiplexing or modulation/demodulation that is normally performed within a tester is moved from the tester into the chip, and the stimulus force/sense paths are extended through the multiplexer to the ADC input

Detailed simulations in a 0.5 μm process show that 100 MHz converters can be tested with 14~16 bit accuracy using lower cost, mixed-signal testers that only have 10 kHz analog capability, and using very little on-chip DFT circuitry. The maximum frequency increases with each new process technology.

The new test is not directly equivalent to conventional sine wave testing because of the new test's reduced sensitivity to sampling jitter, however the new test is more structural and diagnostic.

Many existing low frequency tests, such as ramp-based histograms, sine wave-based FFT, and the DC servo loop method can be reused with almost no modification (noise under-sampling must be accounted for). The test scheme is also suitable for allowing many previously published, *embedded* LF analog stimulus generators or response analyzers to be used for high frequency converters. When this approach is combined with minimum pin-count access techniques for testing digital I/O pins, the costs of multi-site testing and diagnosis can be further reduced.

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