

Constructive Pattern Generation Heuristic for Meeting SSO Limits

Kendrick Baker, Raytheon Company, McKinney, TX, USA

k-baker@raytheon.com

Abstract

This paper discusses a heuristic for generating a minimal number of true/complement patterns while still meeting Simultaneous Switching Output (SSO) requirements. The algorithm presented herein generates the patterns by construction, as opposed to selecting the patterns from a larger superset of possible patterns. This potentially offers advantages in time and memory, since no information about the superset needs to be stored or analyzed. In addition, the algorithm appears to produce good results, which in this case means small pattern sets.

This paper was submitted under the Board and System Test Workshop Call-for-Papers that had an extended due-date. As such, the full text of the paper was not available in time for inclusion in the general volume of the 2003 ITC Proceedings. The full text is available in *2003 ITC Proceedings—Board and System Test Track*.