Automatic Diagnostic Program Generation for Mixed Signal Load Board

Kranthi K. Pinjala, Bruce C. Kim, Pramod Variyam*

Department of Electrical Engineering
Arizona State University
Tempe, AZ 85287-5706

* Texas Instruments, Inc.

Abstract

This paper describes a method for automatically generating diagnostic programs for mixed-signal load boards. This procedure employs a statistical method of computing Mahalanobis Distance to find defects in load board traces and components

1. Introduction

Test throughput is a key factor that affects the manufacturing cost of a mixed-signal product. Throughput is affected by (1) test time of the device (2) handling time of the handler and (3) test hardware down time. Maintaining trouble-free test hardware is important for ensuring minimum test hardware down time and hence high through put.. Test hardware mentioned here includes the automatic test equipment (ATE), handler/prober, and the device load board. Diagnostic programs supplied by the ATE and handler/prober vendor can be used to isolate and fix the problems of these equipments. A diagnostic program for device load boards is a very desirable tool that can quickly isolate and fix the problems and faults of the load boards. Typically test engineer hand-codes load board diagnostic programs. This effort is labor intensive and could take up to one month of test engineer's time. Quite often load board diagnostic program drops down in the engineers priority list and eventually disappears from his task list due to time-to-market pressures. The purpose of this research is to automate the diagnostic program generation for device load boards.

There are three key factors that make today's mixed-signal load boards complicated.

1. There are several mixed-signal system-on-chip (SOC) devices with wide range of functionalities in the market today. Testing all the functionalities and performance parameters of such SOC devices in a single insertion test flow is very challenging. Load boards for a single insertion testing of SOCs have several active and passive components on them and are very complex.
2. Simpler mixed-signal devices are quite often tested in a multi-site environment where more than one device under test (DUT) are loaded on to the load board and are tested in parallel. Multi-site testing with 16 devices in parallel is quite common these days. Complexity of load boards increases tremendously in a multi-site testing environment.
3. Device performance is continuously breaking barriers and load boards are becoming a bottleneck in evaluating true device performance. Signal integrity in load boards is a key part of achieving a high quality and low noise test environment. At speed testing places severe requirements on the quality of the DUT boards, demanding minimal signal distortion at speeds of several hundred megahertz and sub nanosecond rise time.

As the complexity of load boards increase with the above-mentioned reasons, it becomes very difficult to isolate and fix problems of the load boards. Therefore, it is imperative to develop new methodology and tools to automate and speed up the test development for load boards. Traditional in-circuit testing can be used for testing the DUT board circuitry. However, this testing is an expensive investment. The amount of time spent by a test engineer trying to code test programs for testing the boards is large and the task is difficult. The existing test methods for DUT board include continuity checks for opens or shorts in the traces, TDR (Time Domain Reflectometry) to verify the acceptable range of delays on the interconnect paths and component verifications for faulty parts. Other techniques include using SPICE or IBIS model for the DUT board interconnects for validation of DUT boards.

After the assembly of the board, assembly testing and application testing is performed on the board. The application testing is the initial testing and maybe performed at the design house. The aspects tested during the assembly testing are continuity, opens and shorts in the connected pads, signal traces, lands and load board components; acceptable component values and good impedance values for transmission lines; good component, fit and assembly of mechanical components. The application testing of the load board determines if the load board works correctly with the DUT and the ATE. The test results may include time constant measurements, shmoo plots and any other required frequency measurements as applicable. At various times during the application phase of the board, the testing of the board needs to be done. This ensures the signal integrity when the DUT is being tested.

To be able to test the board during its life cycle, a tool that provides all of the tests related to both assembly and application testing would be the most desirable solution to validate the goodness of a board. This paper proposes creation of a virtual reusable test environment that would accomplish this task. The tool developed performs the tests based on the test programs developed by the test engineer. The tool saves the testing time and makes the testing process more convenient and less complex. During the entire life cycle of the board, the same test program could be run several times on the board. In order to increase the test results computation within the tool, a statistical test technique has been proposed. The use of statistical technique would increase the speed of the testing tool developed. The test engineer captures the test information for the board based on the assembly configuration of the board as well as the test information of the IC to be tested using the load board.

2. Limited access testing approaches and the proposed test approach

The typical load board topologies depict that the tester resources such as sources or measure probes that are available to be able to test the load board are very limited. The problem of testing the load board compares to that of limited access testing problem. The conventional in-circuit testing has the limitation of probe location accuracy. The addition of test pads for probe access greatly increases the time-to-market pressures. The need to do functional testing arises to improve the loss of coverage in the in-circuit testing due to limited access. The IEEE 1149.4 standard provides an integrated test pad location at each device pin and maybe used for testing limited access mixed signal devices. Hence a test methodology may be combined with the IEEE 1149.4 architecture and automatic test programs maybe generated based on the topology of the circuit. Various test approaches for analog fault detection and diagnosis have been proposed [1-4]. Most of these approaches rely on the node voltage and current measurements to automatically generate pass /fail tests and component diagnostics. Apart from generating results from voltage –current stimulations of the circuit at all the accessible nodes, the other approaches developed look for the particular test pads that would give the best diagnostic results [5,6] .The IEEE 1149.4 standard also provides for the stimulus and measurement capability. In [7], the IEEE 1149.4 instrumentation and its application to testing active circuits have been outlined. The combination of IEEE 1149.4 standard with the voltage-current measurements methods compensates the bottlenecks encountered due to limited access to the nodes of the circuit.

This paper proposes the testing methodology of voltage-current measurement that does not require fault modeling for analog circuits. It also does not require complete nodal access to automatically generate a test that can provide diagnosis. Therefore, this approach is suitable in testing load boards that have limited access to nodes on the board. However, the use of IEEE 1149.4 architecture in the load boards would be an expensive proposition. The voltage–current measurement techniques and the frequency measurements would suffice for the board test requirements along with the use of techniques for optimal selection of test nodes for improving testability. The tool proposed in this paper implements this methodology. Various algorithms have been proposed for analyzing a circuits node voltages [8-10]. The algorithms proposed have high computational complexity. The algorithm proposed in this paper is a statistical technique that reduces the computational complexity and time involved in declaring pass/fail results.

3. Approach

This paper presents a new tool that implements statistical method for generating diagnostic programs based on the board topology, the availability of tester resources and components on the board. The tool is based on an algorithm used for gaining access to the various DUT board components, determining the testability, which also includes issues of fault detection and diagnosis [11]. The algorithm used for component verification is based on the divide and conquer technique in separating various DUT board components into sub-circuit modules [12]. The sub-circuits are individually tested for the defects in components by the application of the appropriate tests on the available test access points [13]. A fault dictionary is built based on the response of the sub-circuits on the board for various tests. The statistical methods of Mahalanobis Distance and I-Optimality are used for fault detection and diagnosis. The *netlist* file of the load board is the main input to the algorithm and the second input is the *pinmap* file, which gives details of tester resources associated with the board. From the netlist and pinmap files, the library of the tester resources and board components is developed.

The components and tester resources found in the netlist are identified from the inputs to the algorithm. The other information to the algorithm is a *relay configuration* file that identifies various relay types on the board. The following section describes the algorithm in detail.

3.1 Tree Algorithm

Consider the sub-circuit shown in Figure 1 for testing a DUT on the load board. The circuit contains two resistors, two capacitors and a relay.

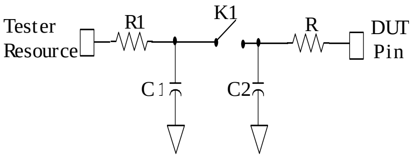


Figure 1. Sub-circuit used for testing the Device Under Test on the load board.

The sub-circuit shown in Figure 1 can be transformed into a tree structure as shown in Figure 2. The tree structure starts from the tester resource to the DUT pin. A node has two or more branches and a branch contains a single component. If the component is connected to ground, the branch ends. A branch can continue with more branches with components.

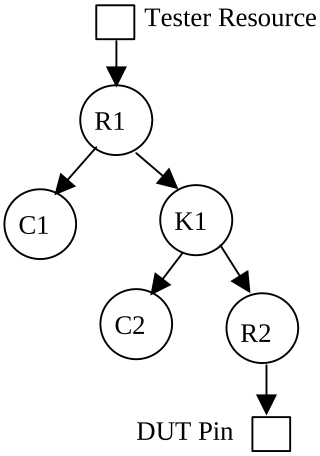


Figure 2 . Tree Structure of Circuit in Figure 1.

The algorithm is summarized as follows:

Step1: From the netlist, construct sub-circuits for testing.

Step2: Identify testable components using the tree structure.

Step3: Apply stimulus to testable sub-circuits.

Step4: Compare responses with data in fault dictionary.

3.2 Construction of Fault dictionary

Once a testable sub-circuit is identified on the load board, SPICE simulation is performed for open and short faults of all components including resistors, capacitors and relays. We use statistical method to identify the faults. The outcome of the statistical method is stored in the fault dictionary database for identifying faults on DUT board under test [14].

4. Statistical Method

On the load board, there are many components with varying tolerances. It is extremely difficult to identify faulty responses for circuits with varying tolerances. Monte Carlo simulations cannot accurately identify the faulty response due to many different combinations of component tolerances. We used Mahalanobis distance [15] to overcome this problem.

Mahalanobis distance (MD) is used to find the “nearness” of an unknown point from the mean point of a group. The observation is classified into a group whose center has a minimum distance. It is superior over other simple distance measures. For instance the Euclidian distance does not capture correlation between variables and needs to be scaled to reflect differences in variances. Therefore, MD is suitable in fault detection where it can provide a good measure of similarity between the observed response and the fault dictionary. In fault detection, only two classes are needed, while in fault isolation many classes may be used depending on how many typical faults need to be isolated. Faulty patterns may be generated by injecting physical failures into the circuit models and performing simulation to determine circuit responses. In the simulation before test process, physical failures are grouped according to their MD measures. In the simulation after test process, the measured waveforms are compared with these groups and their MDs are found to determine whether the circuit is faulty and the physical failures are identified. The Mahalanobis distance is given by

$$D=\sqrt{(x-m_x)^T C_x^{-1}(x-m_x)} \quad (1)$$

where D is the Mahalanobis distance between an n-dimensional feature vector x and its mean vector m_x. C_x is the covariance matrix for the vector x.

Frequency domain tests study the circuit behavior at a number of test frequencies. A rule of thumb is to select test frequencies by picking one below the lowest non-zero break point, one above the highest finite break frequency, and one in between. Several test frequencies are needed near break points.

The test frequencies are picked by any available method. The voltage levels at each test frequency are considered as the feature vector to compute MD measures. Then, the calculated MD in the nominal case and in fault cases is compared to each other to establish the threshold for a decision.

The feature vector is the voltage level vector obtained by recording the voltage response of the circuit at the various test frequencies. Steps involved in the computation of MD distances for circuit diagnostics are shown below:

Step1: The feature vectors for the fault-free circuit for varying tolerances (within the tolerance range) of the components is recorded. The mean of those vectors gives the mean feature vector for the fault-free circuit.
Step2: Single faults are introduced into the circuit .For each fault, the feature vectors are recorded for varying tolerances (within the tolerance range) of the components in the circuit.
Step3: The feature vectors for a single fault are compared to the mean feature vector computed in Step 1.
Step4: The comparisons yield the maximum and minimum MD distances for a given fault (distances are computed as in Equation 1).

4.1 Test Results using Mahalanobis distance

Three circuits are built to test the concept of using Mahalanobis distance to identify faulty components.

Figures 3(a), (b) and (c) illustrate the circuits.

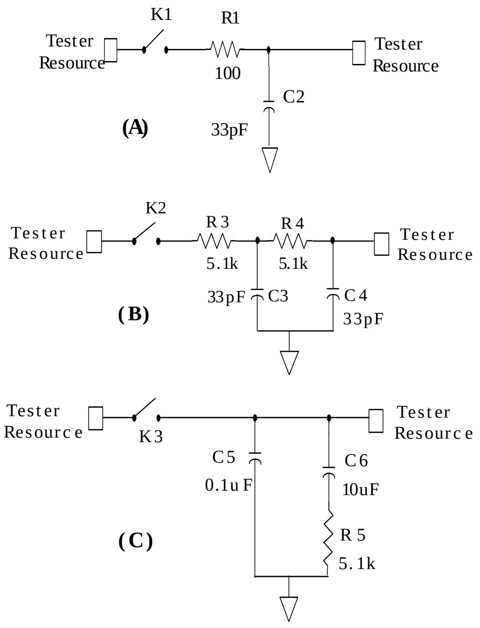


Figure 3 (a) Sub-circuit with relay, two resistors and a capacitor, (b) sub-circuit with relay, two resistors and two capacitors and (c) sub-circuit with relay, one resistor and two capacitors.

We have two test access points available in the circuits of Figure 3. The circuits under test have resistors and capacitors with 5% and 10% tolerances, respectively. A sine wave input of 1.0 Vrms is applied to the circuits. Short and open faults are introduced to each component to simulate faulty conditions. The resistor faults are simulated by complete open or short. Varying the capacitor value to one tenth of original value and ten times the original value simulates the capacitor faults. The input is applied and the voltage is measured at the output of the following test frequencies: 100Hz, 500Hz, 1KHz, 20KHz, 50KHz, 80KHz, 100kHz, 200kHz, 300kHz, 400kHz, 500kHz, 600kHz, 700kHz, 800kHz, 900kHz, 1MHz, 1.5MHz and 2MHz. Using the MD equation, we calculate the Mahalanobis distance of the faulty response from the nominal response. For example, the Mahalanobis distance of R_1 open (Figure 3a) is between 8.12 and 27.74. For all measurements in Figure 3, we activated the relays to closed position.

Table 1. Fault Measurements for Figure 3(a).

Fault	MD Min.	MD Max.
R_1 short	0.0259	0.0387
R_1 open	8.12	27.74
C_2 open	0.0332	0.04
C_2 short	0.0458	0.1345

Table 2. Fault Measurements for Figure 3(b).

Fault	MD Min.	MD Max.
R_3 short	1.5089	3.535
R_3 open	3.8369	12.665
C_3 open	.3908	.4084
C_3 short	2.1066	21.277
R_4 short	.579	.5835
R_4 open	3.2875	8.972
C_4 open	1.3165	1.1468
C_4 short	3.1655	40.296

Table 3. Fault Measurements for Figure 3(c).

Fault	MD Min.	MD Max.
R_5short	0.9235	0.9976
C_5 short	5.984	32.797
C_5 open	1.038	5.462

4.2 Test Results of Mahalanobis Distance for load board Circuitry

Two typical load board circuit topologies have been used to test the Mahalanobis distance concept to identify faulty components. Figures 4(a) and 4(b) illustrate testable sub-circuits on the load board.

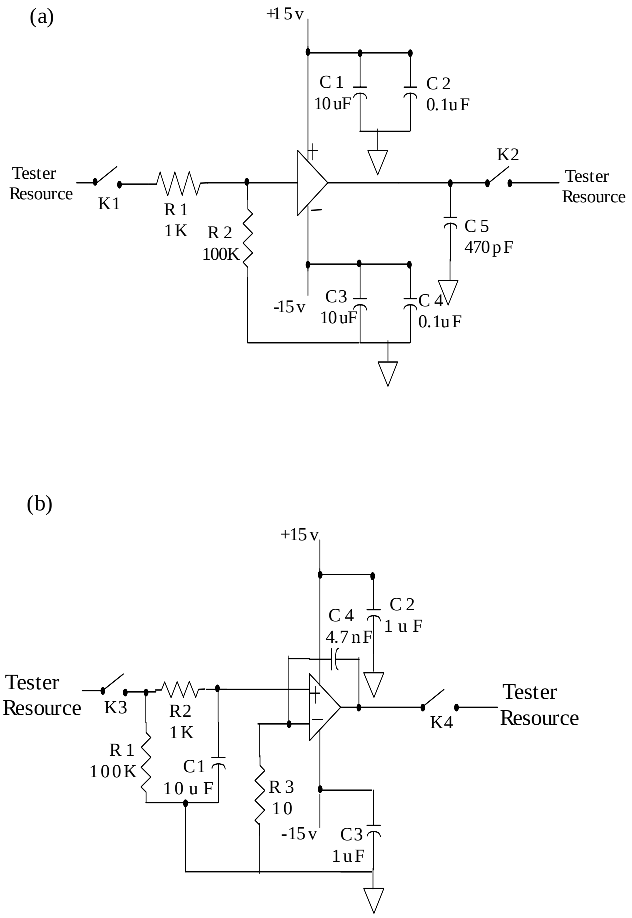


Figure 4 (a) Sub-circuit with relays, resistors, capacitors and a buffer (b) Sub-circuit with relays, resistors, capacitors and an opamp.

Table 4. Fault Measurements for Figure 4(a).

Fault	MD Min.	MD Max.
R_2 short	1.3832	1.3845
R_2 open	0.0125	0.0127
C_1 open	0.0002	0.0011

Table 5. Fault Measurements for Figure 4(b).

Fault	MD Min.	MD Max.
R_2 short	2.9461	2.95
C_1 open	2.541	2.5675
C_1 short	24.9124	28.6521
C_2 open	0.0728	0.1786

We have two test access points available in the circuits of Figure 4. The circuits under test have resistors and capacitors with 5% and 10% tolerances, respectively. A sine wave input of 1.0 Vrms is applied to the circuits. Short and open faults are introduced to each component to simulate faulty conditions. The resistor faults are simulated by complete open or short. Varying the capacitor value to one tenth of original value and ten times the original value simulates the capacitor faults. The input is applied and the voltage is measured at the output of the following test frequencies: 100Hz, 300Hz, 500Hz, 700Hz, 900Hz, 1kHz, 2kHz, 3kHz and 4kHz. Using the MD equation, we calculate the Mahalanobis distance of the faulty response from the nominal response (Table 4 and Table 5). For all measurements in Figure 4, we activated the relays to closed position.

5. Complementary Single Fault Diagnosis

The MD measurements for the single fault detection of circuits in Figure 3 have the limitation of creating solution spaces where two or more single faults overlap in the MD distance. This aliasing effect decreases the confidence level of the total testing strategy. Therefore, we performed a complementary test for fault diagnosis based on computing the predictable variance component of the system output using the I-Optimality criterion.

To derive the best test vector solution for testing an analog system, the I-Optimal approach [16] is used. The test frequencies are selected from I-Optimal solution for estimating the output response of the analog system. The optimal test vectors are applied to the nominal circuit with single fault and the responses are recorded. Let $S_{1,\ldots\ldots,}$ S_n denote the n test frequencies chosen by the I-Optimality criterion. Let X denote the binary coded predictor variable of the form [0 0 0,…,1 1 1 1], having n zeroes and n ones. Let Y = [Y_0 Y_1] where Y_0 denote the output response for nominal system and Y_1 denote the output response of the faulty system, obtained by the optimal test vectors chosen. The predicted values of Y are given by

$$\overline{Y} = r_{xy}\frac{\sigma_y}{\sigma_x}(X - M_x) + M_y$$

where M_x and M_y denote the means and σ_x , σ_y denote the standard deviations of X and Y, respectively and r_{xy} denotes the coefficient of correlation between X and Y. The predicted variance component is thus computed for $\overline{Y}$. Using Monte Carlo Analysis for the analog system under test, the worst-case variations of the components are simulated and the output is recorded. Then the maximum and minimum limits of the predicted variance of the system for each type of single fault are calculated. These upper and lower limits of variance are calculated for all the single faults that can occur in the system and these values are stored as the fault signatures, which are then used for comparison with variances of an observed output.

6. Test Automation

To perform testing of the load board automatically, we developed a simple graphic user interface. The inputs to the GUI are netlist, pinmap and relay configuration files. From this information, a testable sub-circuit is identified. A tree structure is formed based on the testable sub-circuit and MD distance is calculated. The output of the GUI is a file that provides information on testable relays. A Matlab program is developed to automate the computation of Mahalanobis Distances and declare the pass /fail results for the board components. Figures 5 and 6 illustrate the GUI inputs and outputs, respectively.

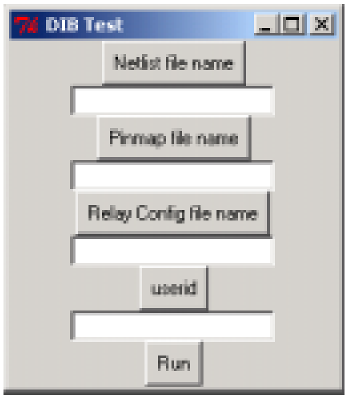
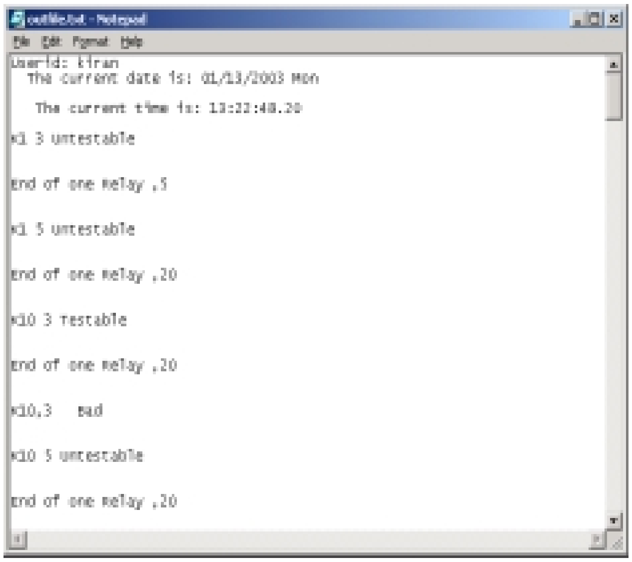


Figure 5. Inputs for the GUI.



```
Userid: kiran
  The current date is: 01/13/2003 Mon

   The current time is: 13:22:48.20

K1 3 untestable

End of one Relay ,5

K1 5 untestable

End of one Relay ,20

K10 3 Testable

End of one Relay ,20

K10,3    Bad

K10 5 untestable

End of one Relay ,20
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Figure 6. Outputs of the GUI for testable relays.

The following is the detailed explanation of the GUI output. The line 4 of Figure 5 shows that the relay K1 with a fixed contact at pin 3 is diagnosed as untestable. Line 5 is an indication that a relay simulation has ended. The lines from 8 to 10 indicate that the relay K10 is testable and it is bad.

7. Conclusions

This paper described a new test technique for the load board using a statistical method. The Mahalanobis distance can be calculated to identify faulty components on the load board. At the same time, interconnect checks can be made by the Mahalanobis distance measurements for complete load board testing. The statistical method is verified by building real circuits in the laboratory and comparison with the simulated data in fault dictionary. The effective fault detection and diagnosis were highly successful. Since the testing method involves node-voltage measurements, it does not need access to all the nodes of the circuit to generate the diagnostic results. The testing method proposed using the voltage-measurement techniques at selective test pads could greatly simplify the test results computation procedures. However, lack of a supporting standard such as IEEE 1149.4 increases the complexity involved in deriving the algorithm for diagnostics of the load board. The graphic user interface was developed to automate the algorithm and further work is being continued to design a testable load board using statistical method.

8. References

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