A High Precision I_{DDQ} Measurement System
With Improved Dynamic Load Regulation

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Abstract

This paper describes a system for performing high precision IDDQ measurement of CMOS ICs having a large peak current during operation. Although the measurement rate is at a low speed of 200uS, the average current of up to 1A during operation may be accepted by improving the dynamic load regulation. This system is also applicable to conventional testing apparatus. This paper covers problems in IDDQ testing, solution for the problems, embodiment of each circuit, verification of the results, conclusion and future issues.

1. Introduction

IDDQ measurement is used as a means of failure detection for CMOS semiconductors.[1] As leakage current has increased due to high integration and reduced minimum feature size, deciding what current value to judge as abnormal has become a problem. Therefore, the conventional IDDQ testing method is inadequate and Delta-IDDQ, IDDT, current signatures, etc. were released as the next-generation test methods. The practical effectiveness of these techniques was unknown and there have been no new proposals from ATE manufacturers. This topic was discussed at ITC in 1999.[2]

A typical SoC multifunctional device carries many IP cores and various standby modes are added to improve power-saving during mobile operation. Many electronic parts can be mounted in one package. This requires an increase in he conditions under which the power supply current must be measured, causing an increase in examination time.

Improvements in productivity due to process yield and early launch of quality products are required due to high-mix low-volume production and reduced time from development to production. Therefore, testing in high or low-temperature environments, where leakage current changes greatly, is also needed.

The demand of detecting abnormalities under such conditions requires the expansion of the dynamic range needed for IDDQ measurements. While the large-scale integration of circuits became possible due to the miniaturization process and the reduced withstanding voltage of the transistor, there is a trend toward lower supply voltage to reduce power consumption. Since the peak current during operation is increasing, improvement of the dynamic load regulation is also required.

Improvement in the speed and precision of measurement of very small currents and improvement of the dynamic load regulation are opposite trends. In order to improve the Dynamic-Load-Regulation property, a large bypass capacitor near the device is required. On the other hand, since voltage noise from the power supply flows to the bypass capacitor and becomes a large noise current in a very small current measurement, improvement in precision and speed are difficult. Therefore, means are taken to reduce the value of the bypass capacitor and make late pattern impression rate at the time of a setup.

In test-program development, BIST and DFT can reduce the manpower required for increasing test patterns and debugging. For device engineers, a design that considers the setup conditions at low speed for IDDQ testing leads to an increase in the workload. The real peak current of the device can be as large as several amperes and then there is an idle period until the next peak current. The average power supply current will become small if the peak current is supplied by the bypass capacitor closest to the device.

For this paper, examinations were performed by simulations, and test results were obtained using prototypes. The prototypes were systems in which an average current of up to 1A during operation is acceptable and measuring a very small current with high precision is possible.

1-1 Target specification

Current ratings	
Maximum output current	1A
Total Load regulation	50mV
(for 500mA change in load current)	
Static-current measurement	
Maximum output current	500mA
Measurement range	10mA
Measurement resolution	0.01% (estimate)
Measurement accuracy	0.05% (estimate)
Measuring time	100uS (estimate)

2. Problems in I_{DDQ} testing

This section reviews two problems in IDDQ testing and introduces a solution for these problems.

2-1 Dynamic Load Regulation

When actually using a device, a power supply is arranged near the device, and many bypass capacitors are used. Features, such as high accuracy, variable voltage, current measurement, and current limiting, are required for a DPS (Device Power Supply) used in a testing apparatus. Moreover, since numerous DPSs are required, the size of the testing apparatus becomes large. Therefore, DPSs are placed at a distance from a DUT and wiring must be used to connect the DPS to the DUT over this physical distance.

The inductive component and the resistive component of the wiring cause problems in realizing a high-speed response. A general power supply detects voltage change of an output caused by a change of the load current using an operational amplifier, and realizes a steady and highly precise constant-voltage property by negative feedback. Since a power supply of the negative feedback type has limitations on how fast it can respond to a change, a rapid supply of current is not available. For this reason, adding large capacitors near the DUT compensates the response delay.

2-2 Noise Current in measuring a very small current

When a capacitor is connected to the source of voltage, a noise current flows due to a voltage noise generated from the source of voltage. If a current measurement is performed under such conditions, the noise current is measured together with the desired current.

Fig.1 shows a typical circuit of a high precision voltage source. Fig.2 shows an example of the voltage waveform (Vm) across the current detection resistance (Rm).

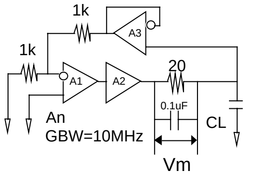


Fig.1 Circuit of a typical high precision voltage source

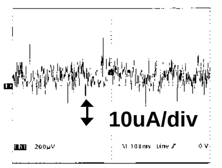


Fig.2 Voltage across the current detection resistance

In a real DPS circuit, the noise becomes still larger because of the noise between the reference voltage, the circuit power supply and ground, and the noise induced on the connection lines, etc. Moreover, the load capacitor with high dielectric constant materials poses a problem with dielectric absorption. Dielectric absorption appears as a series circuit of large resistance and small capacitor in parallel with the main capacitance, making a large time constant and requiring a long time for charging and discharging.

Because of the problems described above, it is necessary to make the value of the capacitor small to supply very small current at high speed.

3. Solution for the problems

If the inductive and resistive components of the connection between the DPS and the DUT can be made small, the dynamic load regulation performance of the DPS will be improved.[3]

At this time, it is also a requirement for the system to be applicable to conventional testing apparatus. Therefore, the solution must use a minimum amount of circuitry and require a minimum number of wires between the testing apparatus and the DUT to be mounted on the user-interface unit, which is called a performance board.

The following conditions were determined considering the conditions described above.

1) Improve the dynamic load regulation.

Adopt a system in which high-speed current supply is possible even if it is placed at a distance from the DUT.

2) Realize both a high-speed current supply and a low current measurement.

At the time of the low current measurement, the path of the high-speed current supply is cut off with a MOSFET.

By putting a resistance into the output of the low current-measurement circuit, this makes the characteristics steady even when a large capacitive load is present.

3) Improve the precision of the current measurement.

To efficiently equalize the noise and realize high precision with a wide dynamic range an integrating type A/D converter is used.

4. Embodiment of each circuit

The circuit configuration is divided into 4 blocks: a high-speed current supply block, a switch block, an IDDQ measurement block, and an A/D conversion block. The configuration is shown in Fig.3.

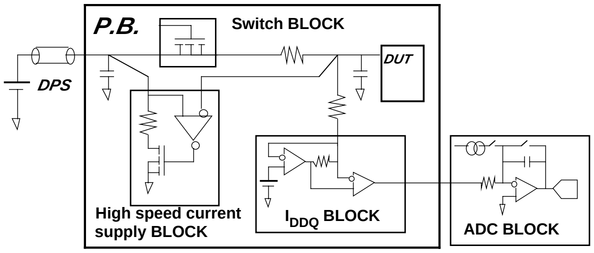


Fig.3 Configuration of the I_{DDQ} test circuit

4-1 Method of IDDQ Measurement

Fig.4 shows the IDDQ measurement timing chart for this system.

The DUT is set up in T0. After the setup is completed, a series of operations for the IDDQ measurement starts with a start signal from the outside.

T1 is the wait time until the voltage fluctuation caused by the setup is recovered. T2 is the wait time from turning off switch S1 until the characteristics become steady. T3 is the wait time until the IDDQ measurement system becomes steady. T4 is the measurement time of an integrating type A/D converter. T5 is the wait time from turning on switch S1 until the characteristics become steady.

The total IDDQ measurement time from T1 to T5 is 180uS. If the frequency of the pattern is 10MHz in the setup of T0, 200 pattern steps correspond to 20uS. As a result, it is possible to measure from T0 to T5 continuously every 200uS.

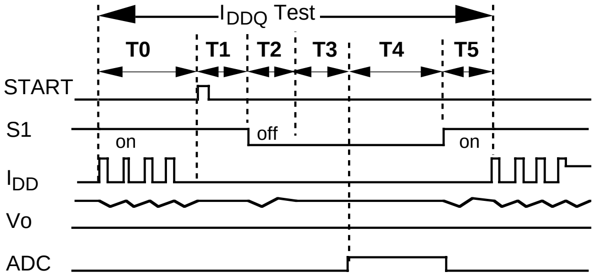


Fig.4 Timing chart of I_{DDQ} measurement

4-2 High-speed current supply block

Although improving the response speed of the DPS will produce a reasonable merit when designed in consideration of the conditions, it will make the size of the apparatus larger. A dynamic load was added to improve the dynamic regulation, leaving the DPS of the testing apparatus as it is. Since the performance and function of the DPS are unchanged, only the transient response can be improved in this system.

Fig.5 shows the configuration.

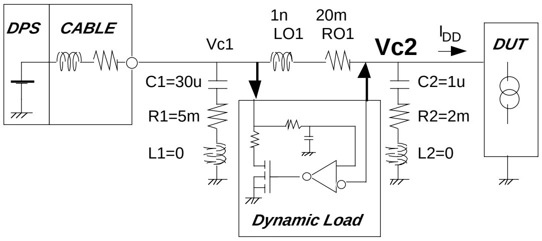


Fig.5 Connection of the Dynamic Load

The principle of operation is simple. A fixed current is applied from the DPS to the DPS side of the dynamic load in advance. If the voltage at the power supply terminal of the DUT falls due to a change in the power supply current drawn by the DUT, the current that has been applied to the dynamic load will be supplied to the DUT. If the voltage is recovered, the current that has been supplied to the DUT will be applied to the dynamic load. The output of the DPS is used as a reference voltage for detecting voltage change. It is low pass filtered in the dynamic load block so that even if there is a change in the output of the DPS, a steady reference voltage can be obtained.

Fig.6 shows simulation results comparing the dynamic load regulation with and without the dynamic load circuit block. The voltage variation is reduced by a factor of 20, from 200mV to 10mV. The variation when the current is changed (20mV) is caused by the inductance from the bypass capacitor to DUT. The recovery characteristics of the voltage are determined by the value of the bypass capacitor, the difference between the current that passes through the dynamic load, and the current that the DUT consumes.

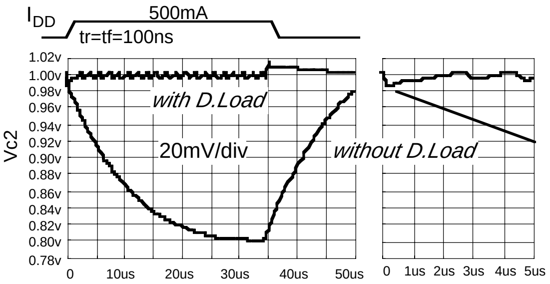
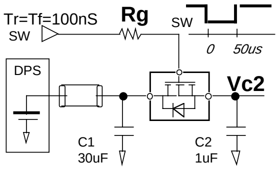


Fig.6 Simulation results comparing the dynamic load regulation with and without the Dynamic Load

4-3 Switch block

A MOSFET is used for the switch. Characteristics, such as small size, low on-resistance, and low leakage-current, are required. A MOSFET switch with low on-resistance has a large gate capacitance and it has a high gate voltage for turning it on/off. Therefore, at the time of switching, spikes to the drain or the source become a problem. The amplitude of the spike is reduced by slowing down the rate of charge and discharge of the gate capacitance by enlarging the resistance driving the gate.

Fig.7 shows the equivalent circuit, and Fig.8 shows the results of simulation. While the spike becomes smaller if the gate resistance is large, the influence of the bypass capacitor is larger and results in a small spike value of 5mV or less.



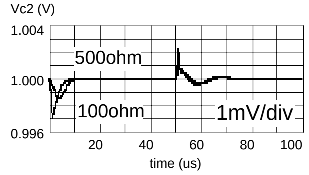


Fig.7 Equivalent circuit of the Switch block

Fig.8 Spike voltage when switching on and switching off

4-4 IDDQ measurement block

A general voltage source current measurement circuit is used for the IDDQ measurement.

Fig.9 shows the connection of the circuit to the DUT. If line-3 is a common cable of 50 ohm, the inductance is 250nH/m, while the capacitance is 100pF/m and the resistance is 100mohm/m. A simple model of the T type with a single step, in which the inductance and the resistance are divided in half, is adopted.

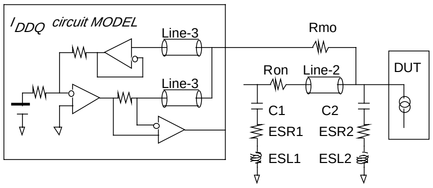


Fig.9 Connection circuit of I_{DDQ} measurement system

Fig.10 shows the equivalent circuit of the IDDQ measurement circuit. In order to improve response, the GBW of the operational amplifier was set to 10MHz.

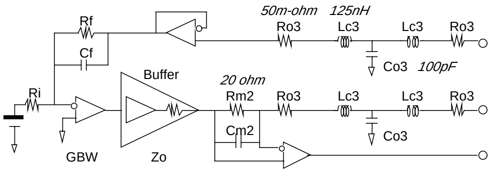


Fig.10 Equivalent circuit of I_{DDQ} measurement circuit

Fig.11 shows the simulation results when the output impedance (Zo) of the buffer amplifier of the IDDQ circuit is changed. From the upper side, 0.1ohm, 1ohm, 10ohm, and

100ohm are shown. It can be seen that values less than 1ohm do not have any significant effect. Therefore, 1 ohm was adopted for the output impedance, as this is commercially available.

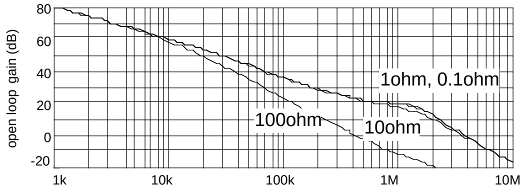


Fig.11 Frequency characteristics when the output impedance(Zo) of buffer amplifier was changed

4-5 Dynamic load regulation and Settling time

Fig.12 shows an equivalent circuit for analysis considering also the influence of the wiring to the DUT.

The connection shown from the output of the switch to the bypass capacitor (C2) right beside the DUT represents the copper pattern wiring in the printed circuit board. A 1-ohm transmission line with 50 parallel 50-ohm transmission lines of 0.13mm width and 35um thickness was adopted and the length was set to be 10cm.

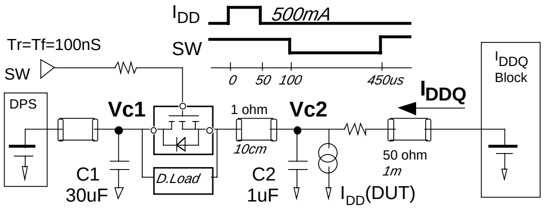


Fig.12 Equivalent circuit for analysis also considering the influence of wiring to the DUT

In order to make the characteristics of each part intelligible, the peak current of the DUT was set to 500mA, the period was set to 50uS, and the quiescent current was set to 1uA. The settling time of the switching was set to 50uS and the settling time of the current measurement was set to 350uS.

Fig.13 shows a comparison of the load regulation in the 1st bypass capacitor (C1) located before the switch. As compared to the conventional power supply, both the falling time and the settling time to the final value are improved greatly; the falling time becoming 1/50, from 25uS to 0.5uS, and the settling time becoming 1/30, from 450uS to 15uS. Moreover, the load-regulation value is also improved as 1/5, from 160 mV to 30 mV.

Fig.14 shows a comparison of the load regulation in the 2nd bypass capacitor (C2) after the switch. As compared with Fig.13, the 20mV voltage drop has occurred due to the resistance of the switch and the 1-ohm transmission line during the period of large current. After the switch was opened, the voltage immediately became steady with almost no influences from the spike, etc., caused by switching on and switching off.

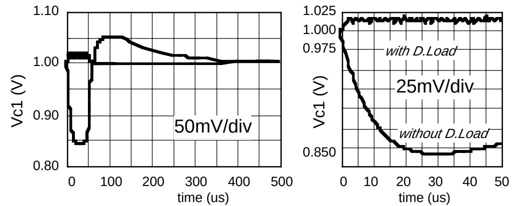


Fig.13 Comparison of the load regulation in the first bypass capacitor (C1)

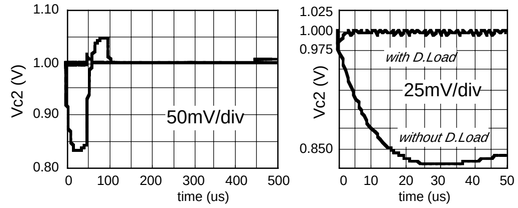


Fig.14 Comparison of the load regulation in the second bypass capacitor (C2)

Fig.15 shows a waveform of the current that flows in the IDDQ measurement circuit. Although there is a difference arising from the current supply block seen while the switch is on, it turns out that there is almost no difference in the settling time for the current to reach the final value after the switch is turned off.

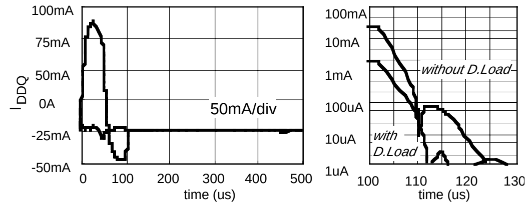


Fig.15 Waveform of the current which flows in the I_{DDQ} measurement circuit

4-6 A/D conversion block

Based on a full-scale current measurement of 10mA, and a resolution of 1uA, the resolution required is 0.01%. Considering that 10mA is converted into 10V, the maximum current of the integrating circuit is set to 1mA, and current measurement time is set to 50uS. The integrating capacitor in this case has a relatively small value as C=1mAx50uS/10V=5000pF.

When the resolution is 0.01%, the voltage produced by the integrating-circuit in this case is V= 0.1uAx50uS/5000pF=1mV. The control time accuracy of the integrating circuit is T=50uSx0.01%=5nS, which is within a technically feasible control range.

In a general integrating type A/D converter, integration is further performed from the voltage that remains in the integral period in order to calculate the final value. This makes the measuring time long. It is possible to shorten the measuring time by measuring the remaining voltage with A/D converters of a serial comparison type. By using a multi-slope type for the type of integration, expansion of the dynamic range and a reduction of the number of bits of A/D converter are also possible.

5. Verification Results

This section provides a summary of the results

5-1 Frequency characteristics

Fig.16 and Fig.17 show the frequency characteristic when a load capacitance is added to the IDDQ measurement circuit. Specifically, Fig.16 shows the simulation results and Fig.17 shows the actual measurements of a prototype circuit. The change in frequency response, which arises due to the value of the load capacitance, match.

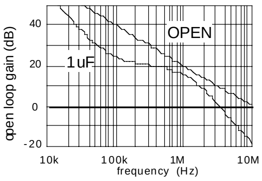


Fig.16 Simulation value of the frequency characteristics

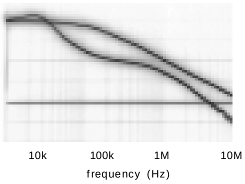


Fig.17 Actual values of the frequency characteristics

5-2 Dynamic load regulation

Fig.18 and Fig.19 show the test results of the prototype circuits when IDD(peak) is equal to 500mA.

Fig.18 shows the voltage waveforms at the first bypass capacitor (C1). The dynamic load reduces the voltage variation from 280mV to less than 20 mV.

Fig.19 shows the voltage waveforms at the second bypass capacitor (C2), having an initial fluctuation of 80mV. This fluctuation is caused by the inductance between the first bypass capacitor and the DUT, and has no dependence on the presence of the dynamic load.

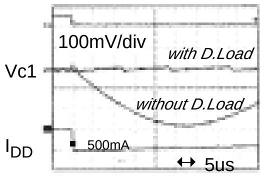


Fig.18 The load regulation value at the first bypass capacitor (I_{DDP}=500mA)

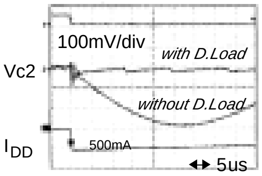


Fig.19 The load regulation value at the second bypass capacitor (I_{DDP}=500mA)

5-3 Settling Time

Fig.20 shows the current measurement waveforms when IDDQ is 0A, and Fig.21 shows the current measurement waveforms when IDDQ is 0.75mA. The value of IDDQ does not affect the settling time. Since a prototype of the integrating type A/D converter is not completed, the settling time for 0.01% including the noise has not been confirmed.

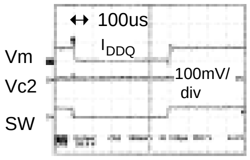


Fig.20 Waveforms of current measurement when I_{DDQ} is 0A

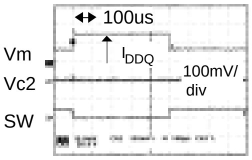


Fig.21 Waveforms of current measurement when I_{DDQ} is 0.75mA

Fig.22 shows a picture of modules made as prototypes.

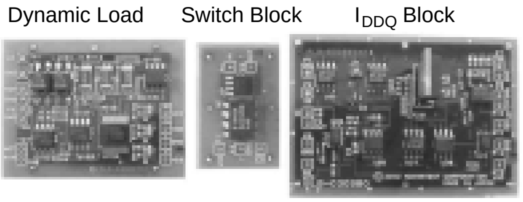


Fig.22 Modules made as prototypes

6. Conclusion and Future issues

Except for the verification of the settling time of the IDDQ measurement, almost identical results for the response characteristics and spikes were obtained for the simulation and for the prototypes.

For further improvement in performance, the placement of the IDDQ circuit right beside the DUT is critical, and miniaturization of the circuit and accepting large current are required. Moreover, it is necessary to examine the integrating type A/D converter and confirm its effectiveness for abnormal detection when used for the actual device.

The improvement in reliability of an electric device is important in a highly information-oriented society. As an ATE manufacturer, it is important to strengthen joint development with engineers, parts manufacturers, EDA manufacturers, and researchers for the improvement in productivity of semiconductors and reliability.

References

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