A New Approach for Low Power Scan Testing

Takaki Yoshida,   Masafumi Watati

Matsushita Electric Industrial Co., Ltd.
1, Kotari-Yakemachi, Nagaokakyo, Kyoto, 617-8520, Japan
E-mail:yoshida.takaki@jp.panasonic.com

Abstract

As semiconductor manufacturing technology advances, power dissipation and noise in scan testing has become a critical problem. In our studies on practical LSI manufacturing, we have found that power supply voltage drops cause testing problems during shift operations in scan testing and we have analyzed this phenomenon and its causes. In this paper, we present a new testing method named MD-SCAN (Multi Duty-Scan) which solves power supply voltage drop problems in scan testing, as well as offering an efficient method of application.

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1. Introduction

In order to guarantee a desired quality and yield of LSI, testing plays an important role in an LSI's development cycle. However, in accordance with the rising transistor count and density of devices, testing is becoming more and more complex while test costs are steadily increasing. In such circumstances, in spite of its strict circuit design rules and area and its performance overhead, scan design has become an indispensable method in order to achieve efficient testing and to obtain the desired fault coverage. Scan design is also the base technology of the new logic BIST.

During scan test application, because clock signals are distributed simultaneously to numerous scan flip-flops, a large amount of power is consumed. As the density of LSI increases, this tendency is becoming more acute, and concerns regarding malfunctions due to power supply voltage drops are growing. Our previous studies show the occurrence of such malfunctions caused by power dissipation and noise in practical LSI testing [1].

In order to reduce power dissipation during scan testing, we can slow down the clock frequency of scan testing. But this method leads to an increased testing time and testing cost. Various methods to reduce power dissipation during scan testing by using dedicated circuits to control the scan clocks have been introduced. For example, methods to reduce power dissipation by means of test partitioning and scheduling have been published[2, 3]. Furthermore, various methods adopt the use of gated clocks to reduce the number of scan clocks operating simultaneously [4-9].

Some methods suggest reducing power dissipation through scan ordering [10, 11].

The problem of power dissipation is also particularly serious for the increasingly popular scan base BIST, and new research is now taking this aspect in consideration [12, 13].

However, even though power dissipation and noise could be reduced, these methods result in an increase in testing time in certain cases. We presented a new scan testing approach aimed at the reduction of power dissipation and noise without an increase in testing time. In our method, test vectors are modified so that power dissipation during scan testing is reduced without increased testing time or a complex clock control circuitry [1].

2. Previous work

In this section, we describe a case of operation malfunction caused by power dissipation and noise during scan testing that we encountered in a practical LSI development project [1].

Figure 1 illustrates an example circuit which causes such a problem. In this example, we used an EB tester and SPICE simulation to observe the state of the signals from BufferA, which is the source providing the scan clock signals to the scan flip-flops, as well as the variation in the power supply voltage supplied to this buffer.

The top part of Figure 2 shows a transition waveform of BufferA obtained with a EB (electron beam) tester in normal mode.

The measured slew rate (the time period required to transit from 10% to 90% of the high or low peak level of a signal) was equal to 1.3ns, a value significantly larger than the slew rate of 0.85ns obtained through SPICE simulation on the same buffer alone. We then stopped the clock of the peripheral scan chain circuit for the scan chain under investigation and observed the resulting transition waveform. As shown in the bottom part of Figure 2, when the clock of the peripheral scan chain circuit is stopped, the slew rate of the buffer improves

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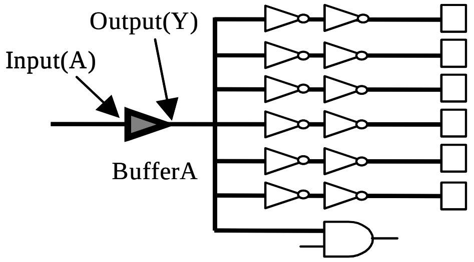

Figure 1. Circuit causing power supply voltage drop

Transistor count	8M
Process	0.18um 4 layers AL
Supply voltage	1.8V

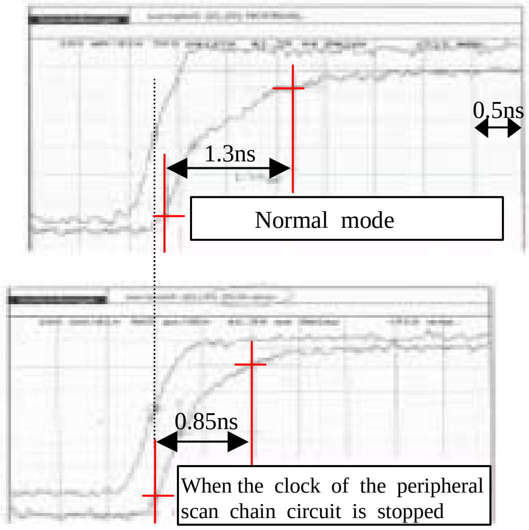

Figure 2. Comparison of the buffer slew rate and delay

greatly, from 1.3ns to 0.85ns, and coincides with the design rate from SPICE.

Figure 3 shows the waveforms of the clock signal sent in scan mode and the internal power supply obtained through EB testing. We can observe that a power supply voltage drop of approximately 300mV occurred upon receipt of the clock edges produced by the scan flip-flops. We can conclude that the malfunction occurred because the simultaneous switching of the circuitry, including scan flip-flops, in scan mode causes a drop in the power supply voltage supplied to the malfunctioning buffer resulting in an increased slew rate in the operation of the buffer.

In a previous work, we presented a new method to reduce the power supply voltage drop named MD-SCAN (multi duty-scan).

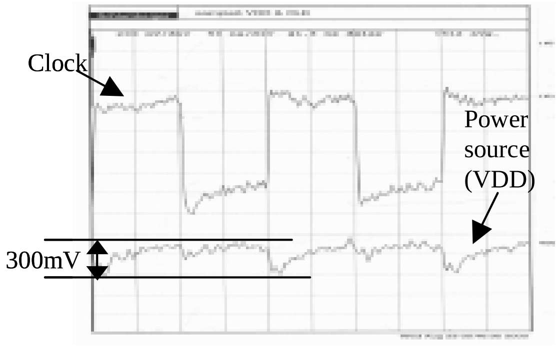

Figure 3. Waveform of power supply voltage observed by EB testing

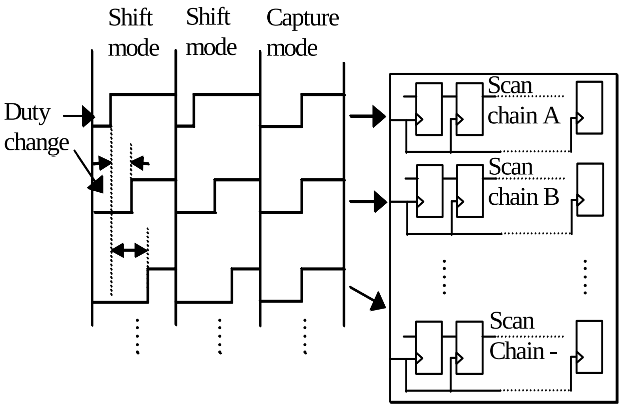

Figure 4. Mechanism of the MD-SCAN method

In the case of multiple scan chains, scan clocks are usually designed to minimize clock skews over all flip-flops so that clock signals can be distributed to destination flip-flops simultaneously. In order to avoid simultaneous operations which thus cause a power supply voltage drop, we changed the duty of the clock signals for each scan chain. In the example of an operation where clock signals are rising, illustrated in Figure 4, clock signals having different duties are applied to scan chains A and B in order to avoid simultaneous shift operations between the scan chains. Clock signals for capture operations are generated so that they can be distributed to all flip-flops simultaneously by switching modes. The fall of the clock signals, when flip-flops do not function, occurs simultaneously. Since the operation cycle stays the same, there is no need to drop the operating frequency during shift time and therefore there is no increase in the testing time. There is also no need of a complex clock control to avoid the overlapping of the clock signals sent to different scan chains. The application of our method is thus relatively easy.

To analyze the power supply voltage drop and observe the results obtained with the MD-SCAN method, we used RailMill from Synopsys. Figure 5 shows the results obtained for the power supply drop in the buffer supplying the clock signals to the scan flip-flops when the clocks are simultaneously sent to all scan chains on a test circuit of several tens of thousands of transistors. Figure 6 illustrates the results obtained for the power supply drop of the same buffer when the MD-SCAN method is applied. We ultimately proved that the power supply drop could be contained by changing the clock duty for an extremely short time.

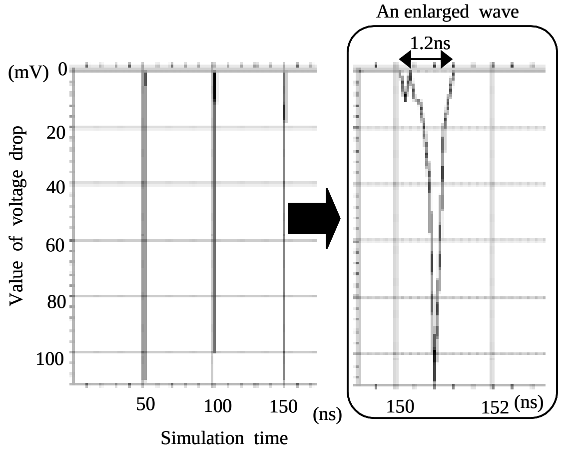

Figure 5. Results of the power supply voltage drop (all simultaneous changes)

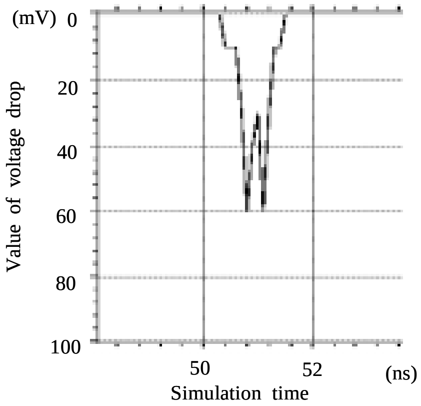

Figure 6. Results of the power supply voltage drop (with MD-SCAN, 0.3ns shift example)

3. Power supply voltage drop problems

We have continued our study of the phenomenon of and causes that produce a power supply voltage drop and of an efficient way of applying the MD-SCAN method.

Figure 7 (shmoo plot) illustrates the relationship between the power supply voltage and the operation cycle using a tester of the same type as the one that produced malfunctions due to a power supply voltage drop during scan testing in our development project. This was accomplished on an LSI of approximately 8 million transistors using a process of 4-layer AL wiring of 0.18um. The power supply voltage is 1.8V.

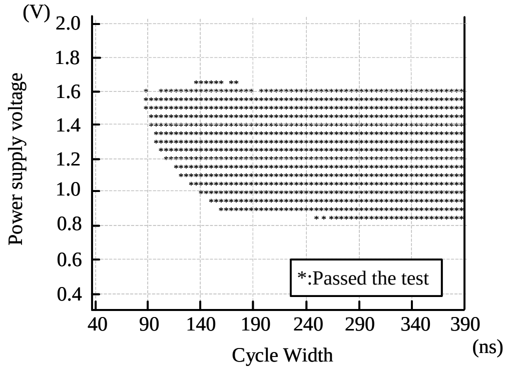

Figure 7. Relationship between the cycle width and the power supply voltage in testing of the malfunctioning LSI

Transistor count	8M
Process	0.18um 4 layers AL
Supply voltage	1.8V

Figure 7 shows that the higher the voltage increases the more difficult it is for the device to function correctly (it does not pass the test).

Having specified the scan flip-flop that causes malfunction at the terminal, where errors were often detected, we observed the data and clock signals for it.

Figure 8 shows the circuitry in the periphery of the scan flip-flop under investigation (FF2 in the figure). Figure 9 shows the power supply voltage used to study the clock signal and the data hold margin of FF2, as well as the variation in the delay from the buffer of origin to FF2.

Concretely, we calculated the delay by analyzing the signal levels by EB tester at the four points indicated by

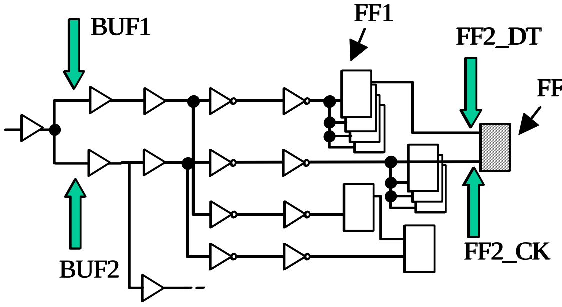

Figure 8. Circuitry in the periphery of the scan flip-flop that caused the malfunction

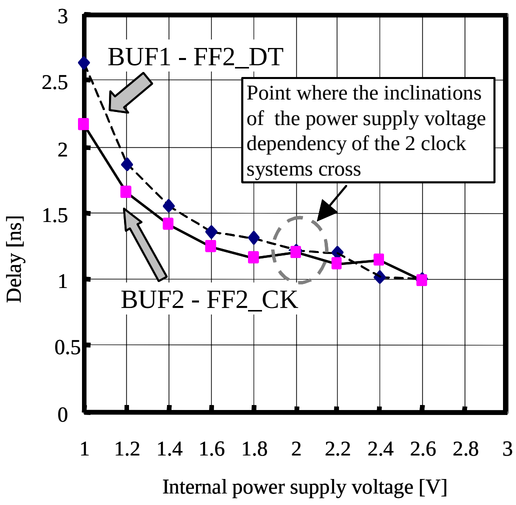

Figure 9. Characteristics of the power supply voltage of FF2 hold margin (Power supply voltage and variation in the delay from buffer of the origin to FF2)

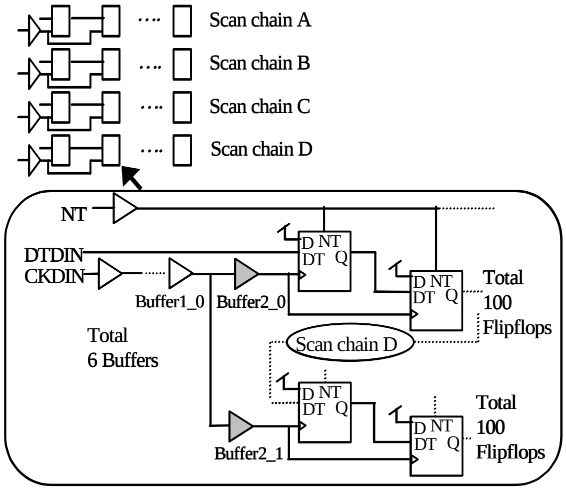

Figure 10. Test circuit (The bottom diagram is an enlargement of a section of scan chain D)

Table 1. Dependence of power supply voltage drop on the power supply voltage

Power Supply Voltage (V)	Scan chain A		Scan chain B		Scan chain C		Scan chain D	
	Buffer		Buffer		Buffer		Buffer	
	2_0	2_1	2_0	2_1	2_0	2_1	2_0	2_1
1.52	170mv	170mv	180mv	180mv	170mv	150mv	200mv	180mv
1.8	240mv	240mv	250mv	250mv	240mv	200mv	280mv	250mv
2.15	290mv	290mv	300mv	300mv	290mv	240mv	330mv	300mv

arrows in Figure 8. We can notice that, according to the figure, when the voltage is low, the signal delay of the data is larger than that of the clock. They gradually get closer as the power supply voltage is increased and eventually are inverted. In other words, even if we manage to guarantee the hold margin of the scan flip-flop, this margin will presumably disappear gradually as the power supply voltage increases, eventually giving rise to a malfunction.

We have assumed that, as in the case described in our previous work, the cause of this phenomenon lies in the delay caused by a power supply voltage drop when clock signals change simultaneously, and we thus deepened our study.

4. Experimental results

4.1 Variance of the clock delay and drop of the power supply voltage

To analyze the problems occurring on practical devices, we studied the relation between the power supply voltage and power supply voltage drop with the clock delay.

We used the same RailMill from Synopsys as we did in our previous work to estimate the power supply voltage drop. As RailMill can not be used on a practical LSI scale, we tested by designing and verifying with a small scan circuit that was close to reality. The configuration of the sample circuit is illustrated in Figure 10. The process is 0.18um, a three-layer AL wiring is used and the power supply voltage is 1.8V. It has four independent scan chains, A, B, C and D, each of the scan chains consisting of 200 scan flip-flops. Each scan chain is separated by clock tree synthesis into 2 columns of 100 flip-flops. The power supply line is laid out so as to be shared by the four scan chains. As we are performing a check related to the shift operation, the data input of the scan flip-flops is fixed at H.

The objective of the RailMill verification is the power source supplied to Buffer2_0 and Buffer2_1 (in gray in the figure), that are the sources supplying clocks to the scan flip-flops of each scan chain.

Table 1 shows the power supply voltage drop of each buffer for three different power-supply voltages, 1.52V, 1.8V and 2.15V. This table shows that the higher the power supply voltage is, the more it drops. We also notice that the power supply voltage drop is not constant within the same circuit. If, for example, we compare Buffer2_1 of scan chain C and Buffer2_0 of scan chain D, we can observe a tendency for the discrepancy in the values of the power supply drop to widen with a difference of 50mV, 80mV and 90mV when the power supply voltage is 1.52V, 1.8V and 2.15V, respectively.

Next, we examined the extent of the simultaneous operation of the scan flip-flops. The concrete method of verification is to examine statistically the values of the path delay of clock signal inputs for the scan flip-flops, when clock signals are simultaneously sent from external CKAIN, CKBIN, CKCIN and CKDIN. Figure 11 illustrates the distribution of the delay from the external input to the clocks of all scan flip-flops for the three different power supply voltages. Table 2 shows the average delay and the standard deviation for each power supply voltage. We can notice that the higher the power supply voltage is, the smaller the variance of the delay becomes, thereby increasing the probability for the scan flip-flops to operate simultaneously and eventually leading to a power supply voltage drop.

With regard to the malfunctions described in section 3 and the data and clock signals of the scan flip-flop at the source of the problem, the higher the power supply voltage becomes, the larger the value of the power supply voltage drop on the clock side becomes in comparison with the data side. At the same time, the delay caused by

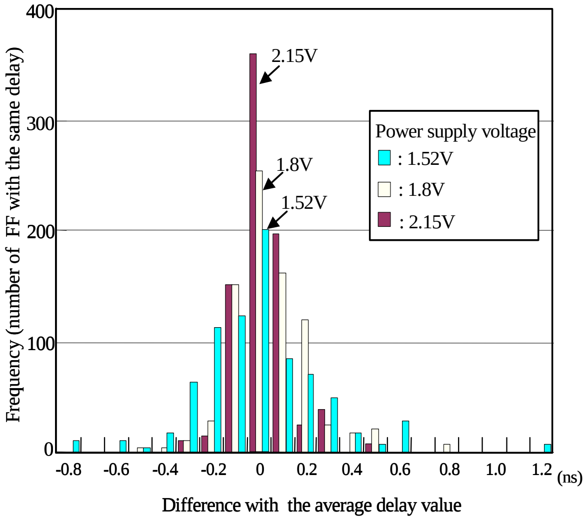

Figure 11. Delay distribution from external input to clocks of all scan flip-flops

Table 2. Dependence of the average delay and standard deviation of all scan flip-flops on the power supply voltage from external input to clock input

Power Supply Voltage (V)	Average Value (ns)	Standard Deviation
1.52	1.47	0.056
1.8	0.82	0.033
2.15	0.51	0.020

With regard to the malfunctions described in section 3 and the data and clock signals of the scan flip-flop at the source of the problem, the higher the power supply voltage becomes, the larger the value of the power supply voltage drop on the clock side becomes in comparison with the data side. At the same time, the delay caused by the power supply voltage drop increases resulting in an insufficient hold margin.

As we mentioned before, the value of the power supply voltage drop is not constant but varies within the circuit. We therefore decided to perform a more detailed study including the physical place and route positions of the scan flip-flops and of the buffers that were used for the analysis of the power supply voltage drop in the test circuit. Figure 12 is a diagram that illustrates the physical place and route of the test circuit.

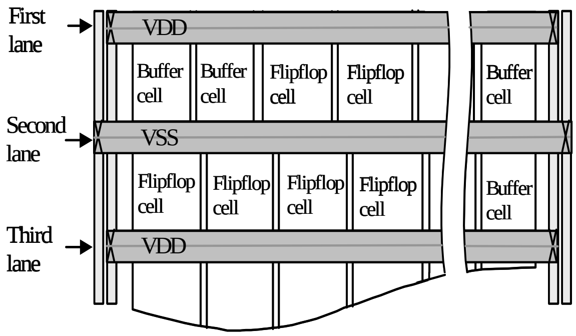

Figure 12. Physical place and route diagram

Table 3 shows the physical place and route position of the buffers under investigation and indicates on which lane they are placed. It also indicates the number of flip-flops placed on the lane of the buffers. When studying this table in conjunction with Table 1, we find out that, although it may be due to the small size of the test circuit, buffers that are positioned on the same lane show the same value for the power supply voltage drop.

Table 3. Physical place and route position (lane number) of each buffer and number of scan flip-flops on each lane

	Scan chain A		Scan chain B		Scan chain C		Scan chain D	
	Buffer		Buffer		Buffer		Buffer	
	2_0	2_1	2_0	2_1	2_0	2_1	2_0	2_1
Lane number	29	29	12	12	29	9	23	12
Number of FF on each lane	20	20	23	23	20	20	22	23

Table 4 shows the variance of the delay at the scan flip-flops positioned on the lanes that include the buffers under investigation. Because only a small number of scan flip-flops, up to a maximum of 23, are positioned on each lane, and because the number of flip-flops itself is determinant, it is difficult to hold a discussion based on simple sums. However, when comparing each lane, we can notice a general tendency such that the greater the number of flip-flops with a small delay variance there is on the same lane, the larger the power supply voltage drop is. We can therefore conclude that the delay variance is linked to the value of power supply voltage drop.

Table 4. Dependence of the standard deviation from the average delay from scan flip-flop external input starting on the power supply voltage from each buffer to clock input

Power Supply Voltage (V)	Scan chain A		Scan chain B		Scan chain C		Scan chain D	
	Buffer		Buffer		Buffer		Buffer	
	2_0	2_1	2_0	2_1	2_0	2_1	2_0	2_1
1.52	0.028	0.028	0.023	0.023	0.028	0.033	0.020	0.023
1.8	0.018	0.018	0.015	0.015	0.018	0.022	0.012	0.015
2.15	0.011	0.011	0.010	0.010	0.011	0.014	0.008	0.010

4.2 Optimal way to apply the MD-SCAN method on a practical device

As was mentioned in section 2, the MD-SCAN method that we disclosed in a previous work is effective against power supply voltage drops.

This method consists of shifting the clock duties of the clock system so that the scan flip-flops do not function simultaneously.

Figure 13 illustrates the variation in the power supply voltage drop of the buffer under investigation when the MD-SCAN method is applied. This example shows the case when clock signals of different duties are sent to scan chains A, B, C and D.

We can see that the use of this method produces a decrease in the various values for the power supply voltage drop of the buffers under investigation in all cases (the difference for lane 9 and lane 23 for instance is approximately 80mV). The value of the power supply voltage drop eventually remains almost the same after the duty was changed about 0.3ns~0.4ns (the difference for lane 9 and lane 23 for instance is approximately 10mV), or in other words, becomes the value of the power supply voltage drop which is the least affected by any simultaneous change.

Figure 14 shows an example when the clock duties are changed for the A and B, and C and D pairs. In this case as well, we can notice a decrease in the power supply

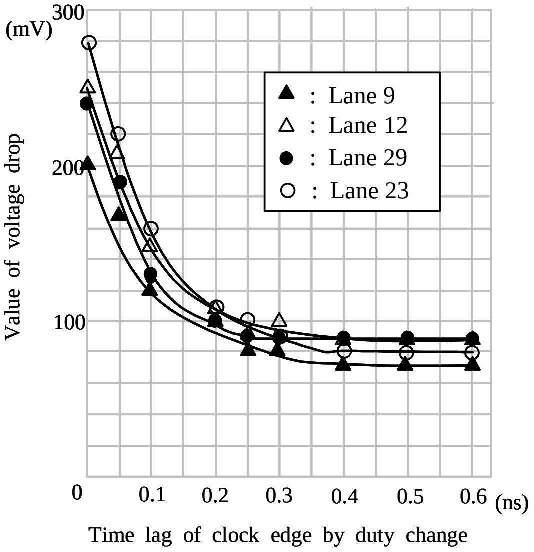

Figure 13. Relationship between the range of the clock duty change and the power supply voltage drop with the MD-SCAN method (Duty change for all scan chains)

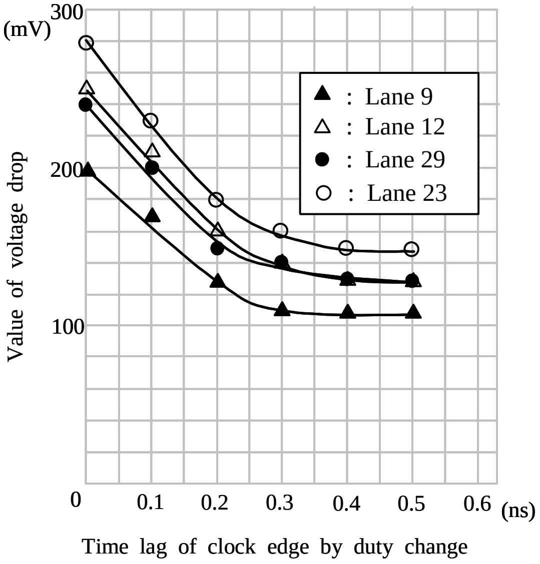

Figure 14. Relationship between the range of the clock duty change and the power supply voltage drop with the MD-SCAN method (Paired duty changes for scan chains A and B, and C and D)

voltage drop that eventually remains almost the same after the duty was changed about 0.3ns~0.4ns. The value at which the power supply voltage drop remains almost the same is smaller when the duty is changed individually for scan chains A, B, C and D than when the duty change is performed by pairs A,B and C,D.

Table 5 shows the delay variance when the MD-SCAN method is used. The delay variance is naturally larger in comparison to when clock signals are sent simultaneously to all scan chains, as in the case of Table 2. We can say that, by increasing the delay variance, our method enables us to avoid simultaneous change.

Table 5. Dependence of the average delay and standard deviation of all scan flip-flops on the power supply voltage from external input to clock input (With MD-SCAN, duties of scan chains A and B, and C and D are shifted by 0.1ns)

Power Supply Voltage (V)	Average Value (ns)	Standard Deviation
1.52	1.62	0.115
1.8	0.96	0.113
2.15	0.65	0.112

In order to apply the MD-SAN method most efficiently, it is ultimately best to split the scan flip-flops placed on the different lanes of the place and route so that the clocking can be accomplished as much as possible with a delay variance. For example, it is better that the duty is changed individually for scan chains A, B, C and D, than that it is changed by pairs A,B and C,D. This is because, in the former case, the delay variance of the scan flip-flops placed on each lane of the place and route is larger, and thus, the value is smaller at which the power supply voltage drop remains almost the same.

Accordingly, the dispersion of the clock delay for the scan flip-flops on the place and route ultimately produces a decrease in the power supply voltage drop. Or, conversely, the most efficient scan clock shift can be to some extent gathered from information regarding the number of scan flip-flops and the lanes on which they are laid out on the scan chain.

There might be a high probability that a detailed change of clock duty for each scan chain would produce a dispersion of the clock delay for the scan flip-flops on the place and route.

However, while there is no problem when the design is such that the clock system is set for each scan chain, one must be careful when scan chains are changed with multiple clock systems like FF1 and FF2 of Figure 8. In this case, care must be taken in the design stage to set a change of clock duty that does not cause skew.

In other words, if the design, including the place and route, is not planned beforehand on the premise of the use of the MD-SCAN method, there is a possibility that a complex change of duty will make the design more difficult.

Nevertheless, by simply dividing the overall clock signals into two without making detailed duty changes for each scan chain, like for the example shown in Figure 14, although there is a variance in the extent of the decrease of the power supply voltage drop, the drop on the whole is improved and one can obtain a reasonable effect. Looking at it on a macro scale, a power source is supplied to the whole circuit so that splitting the operating scan flip-flops into two has an overall effect and makes sense.

In brief, if in practice it is possible to make sufficient arrangements in the design, including place and route, detailed duty changes for each scan chain could also be possible and would probably produce a greater effect. Conversely, if it is difficult to accommodate the circuit, it might be easier, in terms of design, to split all scan chains into large groups for the duty change. This also will produce a satisfactory effect.

5. Conclusions and Future Work

Up to now, scan design, including place and route, has been planned so that the clocks of the scan flip-flops move simultaneously as much as possible. There was no question in that regard. But we would like to issue a warning regarding this accepted content.

After place and route, practical scan flip-flops function with a slight variance in delay. The more one tries to correct the clock delay, the more it leads to a drop of the power supply voltage. This may not have been a problem to this point, but recently it has reached the point where the delay becomes the cause of malfunction. This phenomenon becomes particularly striking when the delay variance is small and the power supply voltage is high.

Therefore, in terms of design, it is wise not to correct those parts that do not require a correction of the clock delay. We have presented the MD-SCAN method as a way of producing variance in the delay and proved its efficiency.

The amount of power supply voltage drop varies within a single circuit. While it is feasible to guess, based on place and route data, to a certain extent the parts where the power supply voltage is likely to drop, this specification might not be easy. By adapting beforehand the design for the use of the MD-SCAN method, we should be able to contain the delay that caused the power supply voltage drop more efficiently and thus eventually make the design itself easier.

Following the recent increase in LSI speeds, cases of malfunctions caused by phenomena unseen up to now and tied to signal integrity, such as the power supply voltage drop described in this paper, are emerging. In the future, we will study how the MD-SCAN method that we have presented here can be useful in practice in order to improve signal integrity phenomena, including power supply voltage drops.

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