Challenges in Low Cost Test Approach for ARM9™ Core Based Mixed-Signal SoC DragonBall™-MX1

George Bao
Motorola Semiconductors Hong Kong Limited
George.Bao@motorola.com

Abstract

This paper discussed the challenges that we faced when we developed the low cost test strategies for the new generation ARM9™ Core based mixed-signal System-on-a-Chip (SoC), DragonBall™-MX1 (DBMX1). First of all, we presented a tailored cost model to select our Automatic Test Equipment (ATE). With this low cost tester, we developed a method for at-speed digital tests with slower tester clock, a new embedded PLL jitter test approach with sliding delta cycle and fixed strobe, and a loop-back self-test proposal for embedded ADC and DAC. Our final target is to achieve all the mixed-signal tests on a very low cost pure digital ATE.

1. Introduction

Motorola's DragonBall™ product family is the leading microprocessor in the portable handheld market. MC68000 core based DragonBall™, DragonBall™-EZ and DragonBall™-VZ dominate the Palm OS based controller market of Personal Data Assistant (PDA). DragonBall™-MX1 (Media Extensions) [1], a 200MHz ARM9™ Microprocessor Core based mixed-signal System-on-a-Chip (SoC) with latest Motorola 0.18um HiP6W CMOS dual-gate-oxidation and five-metal-layer technology is the fourth generation DragonBall™ series. It integrated 128KB embedded SRAM and over 30 digital modules, such as, LCD Controller, SDRAM Controller, USB Support, Multimedia Card and Secure Digital Host Controller, Memory Stick Host Controller, Smart Card Interface, Image Sensor Interface, Bluetooth Accelerator and etc. Besides, there are two major embedded mixed signal modules integrated. One is the clock generation module containing one 192MHz MCUPLL and one 96MHz USBPLL from either a 32KHz oscillator or a 16MHz oscillator. The other is called Analog Signal Processor, which consists of one 16-bit Sigma-Delta touch panel input ADC and one 16-bit Sigma-Delta voice CODEC containing ADC and DAC. Figure 1 is a simplified DBMX1 block diagram and its floor plan.

The silicon test of DBMX1 is not only driven by the time-to-market schedule, but also by the competitive cost requirements. According to SIA 2001Edition of International Technology Roadmap (ITR) for Semiconductors [2], for microprocessor, the manufacturing cost per transistor dropped ten times while the cost of Automatic Test Equipment (ATE) depreciation just increased slightly. Figure 2 showed the trends to the next decade for Microprocessor [2]. We mapped the estimated data for our DragonBall™ (DB) products into this chart and found that we had much room for the improvement of our test cost.

In the ATE market, high speed digital channels (over 100MHz) with sophisticated Edge Placement Accuracy (EPA) were very expensive. To test a Mixed-Signal SoC requires even more expensive mixed-signal ATE. By balancing these requirements, we developed a test cost model for ATE selection. This model assisted us in making the decision to target our silicon test on the ATE with very low Cost Per Pin (CPP). But, how to minimize the trade-off in test coverage became our big challenges. This paper went through these challenges, including at-speed digital test with slower test clock, embedded PLL test, and embedded ADC and DAC test. With the methods we adopted to settle all the test challenges, we proved our approaches to achieve the maximized test coverage and tester utilization with the minimized test cost. Furthermore, by applying the loop back test for ADC and DAC, we will be able to achieve all the mixed-signal tests on pure digital low cost ATE. But, many studies are on going to avoid the noise cancellation issue for this self-test proposal.

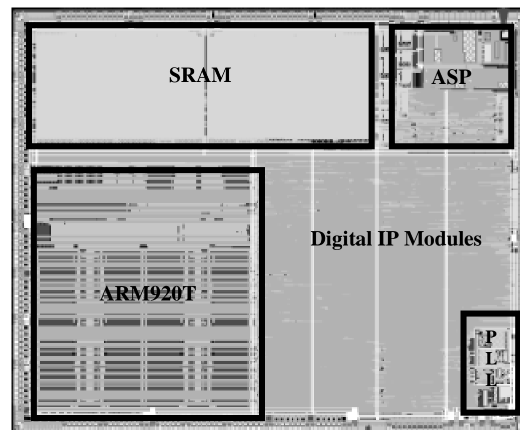


Figure 1. DBMX1 block diagram and layout floor plan.

0-7803-8106-8/03 $17.00 Copyright 2003 IEEE

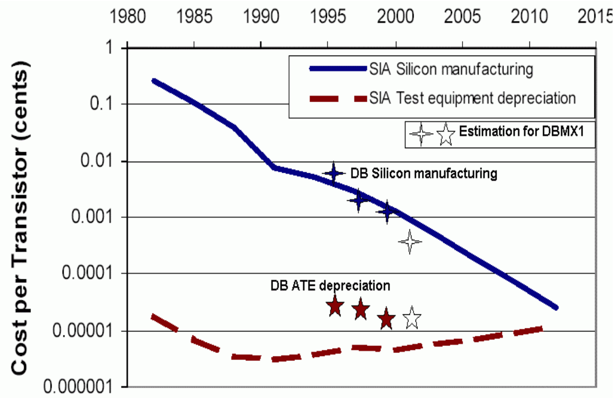


Figure 2. Microprocessor cost of test trend model.

2. Test Strategies and ATE Selection

First of all, the challenge came from the selection of the ATE. When defining the test strategy for DBMX1, we studied several useful test economics models. But, these models mainly focused on the decisions about whether to do DFT and covered the relatively bigger scopes. Some modeled the test cost to the combination of the front-end NRE and back-end Volume related [20], while some covered all the aspects from test preparation cost, execution cost, silicon related cost to quality related cost [19]. In the research and development area of silicon test, there were several popular cost reduction methods published, such as Multi-site Test [3], Reduced Pin Count Test [4], Bandwidth matching [5] and Low channel cost tester [6] (i.e. $400 vs.$4k).

In our case, DBMX1 was a high speed SoC with full scan methodology already implemented in all the digital and memory modules as shown in Table 1. About 26% of the die area was contributed by the golden ARM920T core test patterns. There were 76 patterns accessed via Test Interface Controller (TIC) with 99.5% coverage from 630K vectors [7]. Another 64% of the die area was covered by the full Automatic Test Pattern Generation (ATPG) scan and built-in-self-test (BIST). Full stuck-at ATPG scan was designed with 97.6% fault coverage. There were two scan groups from two IP modules. One was called AHB_IP1, covering the following modules:

ETM and ARM DFT wrapper, BROM, DSPA, AHBC, AIPI1, AIPI2, AITC, DMA, LCDC, MEMC, PWM, RTC, TIC, TIMER1, TIMER2, UART1, UART2, WDT, AIPI2 wrapper, AITC wrapper and DMA wrapper.

The other was called AHB_IP2, covering the reset of the modules as below:

ASP digital, ASP analog wrapper, BTA, CRM, CSPI, GPIO, OSC16M wrapper, OSC32K wrapper, RAM1_64K wrapper, RAM2_64K wrapper, MSHC, SIM, SSI, USBD, AIPI2 wrapper, AITC wrapper and DMA wrapper.

AHB_IP1 covered 97.22% of total 1799538 faults and AHB_IP2 covered 97.35% of total 2354780 faults based on the simulation. As transition delay faults and path delay faults were not simulated in this iteration, we had to implement at-speed normal mode assembly code tests for key modules in addition. For embedded 128KB SRAM and other caches, we adopted BIST to minimize the test time and vector memory. For the bitmapping analysis, a marching algorithm with embedded DMA is simulated and tested so as to avoid the expensive memory test option on ATE.

Based on these features, in evaluating several proposed test platforms, we set our target on how to lower the manufacturing equipment related test execution cost. This required us to balance the cons and pros between an expensive high speed VLSI ATE or a low cost digital ATE with additional clock module built on Device-Interface-Board (DIB). In the other hand, DBMX1 is also integrated with a mixed signal ASP module with 16bit base band ADC and DAC, which asked us to make another choice between a mixed signal ATE and a digital ATE with mixed signal test option. Therefore, we tailored our cost model into a simpler one with the concerns of the test equipment cost in assisting our decision for the ATE selection. We defined the test equipment related cost per test insertion (C_{test}) to be the sum of manufacturing related ATE cost (C_{ate}), ATE option related cost (C_{opt}), on-DIB add-on circuit module related cost (C_{dib}) and other miscellaneous cost (C_o) in Equation (1).

$$C_{test} = C_{ate} + C_{opt} + C_{dib} + C_o \qquad (1)$$

In our model, we defined C_{ate} by the terms of cost per digital pin (C_{perpin}), the number of configured pins (N_{pin}), the ATE utilization (U_{ate}), the depreciation ratio (R_{dep}) during the depreciation period (T_{dep}) and the unit silicon test time (T_0). We adopted Equation (2) because any selected ATE could be shared by the manufacturing of the other products. Although the cost of ATE was determined by the depreciation, the cost of the special option in ATE was mainly absorbed by the test of this specific product. Therefore, we modeled C_{opt} by dividing the full depreciation of the option (C_{dopt}) by the test insertion volume (V). As there was still so-called opportunity utilization for other product to share the option, we defined this factional multiplier (M_{opt}) in Equation (3) for C_{opt}. However, the cost of add-on circuit modules on DIB (C_{addon}) was 100% charged to this product and its estimation was simplified in Equation (4). We considered other cost, including that of handling (C_{handle}) and of quality ($C_{quality}$), to be minor and consistent in Equation (5).

$$C_{ate} = \frac{C_{perpin} \times N_{pin}}{U_{ate}} \times \frac{R_{dep}}{T_{dep}} \times T_0 \quad (2)$$

$$C_{opt} = \frac{C_{dopt} \times M_{opt}}{V} \quad (3)$$

$$C_{dib} = \frac{C_{addon}}{V} \quad (4)$$

$$C_o = C_{handle} + C_{quality} + ... \quad (5)$$

Then, we applied the following assumptions to our test cost model for DBMX1: N_{pin}=512 for a dual-DUT test; U_{ate} =50%; R_{dep}/T_{dep} =20%/365(days) for a five year straight-line depreciation; T_0=10 seconds per insertion; C_{dopt}=USD200K for a mixed signal option; M_{opt}=70%; C_{addon}=10K for 5 DIBs; C_o=USD0.05. We plotted the relation between the test equipment related cost and test insertion volume in Figure 3 by further assuming USD1.3K per pin for low cost digital ATE, USD2K per pin for high speed VLSI ATE and USD3K per pin for relevant mixed signal ATE. In this chart, as the test insertion volume increased, the cost of the low cost digital ATE dropped significantly. When the insertion volume was over 1.4 million, the test cost of the low cost digital ATE with mixed signal test option would be lower than that of the mixed signal ATE. Then, the breakeven point between VLSI ATE with the option and the mixed signal ATE was 2.2 million. It was interesting that after 3.1 million insertions, the cost of the low cost digital ATE with the option would drop even below those of the VLSI ATE without the option. Therefore, the justification came from the test insertion volume.

Throughout the above analyses, we made our decision to select the low speed ATE with a mixed signal test option for the pilot production test. The pure digital ATE could be used as the opportunity for the future mass production. But during the implementation there came the test challenges to tackle with this selected low cost test solution.

First is the at-speed test for the speed that is over the ATE clock limit. The embedded ARM920T CPU core can be speeded up to 200MHz while the other modules and I/Os are working under 100MHz in asynchronous clock mode. The solution is to generate this 200MHz input clock for ARM920T core by an on-DIB add-on clock doubling module [8]. The second challenge is to test the PLL jitter of the embedded MCUPLL (up to 192MHz) and USBPLL (up to 96MHz) using the maximum 100MHz digital channels. The input oscillator clock (32KHz) for these PLLs are too low to make the output phase aligned steadily. In order to minimize the impact from the ATE EPA and ATE clock jitter, we devised an under-sampling method called sliding delta clock with fixed edge strobe. This method is also effective to test the jitter for the free running clock with undetermined frequency and phase. The third challenge is the test of ASP with a touch panel ADC and a voice band CODEC containing ADC and DAC. At the early stage, we used the Mixed-Signal Option (MSO) in the ATE for characterization and pilot production test. As the production volume goes up, we will not be able to afford to invest more of such expensive option. Therefore, a loop back self-test approach to test embedded DAC by embedded ADC is proposed and under development. The rest of this paper will present the methods to deal with these challenges, at-speed digital test, embedded DPLL test and embedded ASP test. The potential improvement to lower the silicon test cost will be discussed as well.

Modules to Test	Area Ratio	Test Methodology
ARM920T	26%	Golden Functional Vectors with 99.5% claimed Coverage
SRAM & FIFO	24%	DFT (BIST) with full coverage
AHB_IP1	20%	DFT (SCAN) with 97.22% Fault Coverage
AHB_IP2	20%	DFT (SCAN) with 97.35% Fault Coverage
At- Speed Digital	N/A	At-Speed Functional Test
PLL	3%	Frequency Counter and Jitter Test
ASP	7%	ADC & DAC Mixed Signal Test

Table 1. DBMX1 DFT strategy.

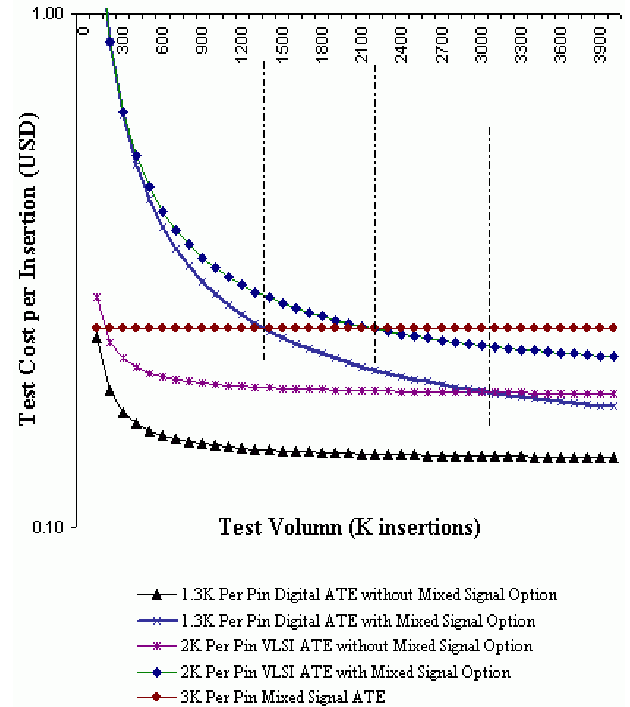


Figure 3. Relation between test equipment related cost and test insertion volume for DBMX1 ATE selection.

3. At-Speed Digital Test

Digital circuits covered over 90% of the DBMX1 die area. There are two clock domains inside DBMX1 generated from internal MCUPLL and USBPLL. One is called FCLK for ARM920T CPU, which can run up to 200MHz and the other named BCLK servers all the rest circuits. In silicon test, we partition the clock domain into four parts as shown in Table 2.

Test Clock Domain	Modules to Test
External 32KHz & 16MHz OSC clock	PLL frequency and jitter
External slower clock bypassing USBPLL (BCLK) & MCUPLL (FCLK)	I/O Leakage and Drive Static and dynamic IDD ARM920T TIC Stuck-at ATPG SCAN IEEE1149.1 JTAG ESRAM bitmapping
External 100MHz clock (BCLK)	At-speed assembly code At-speed eSRAM BIST At-speed ASP test
External 200MHz clock (FCLK)	At-speed ARM920T CPU (Asynchronous Mode)

Table 2. Test clock domain arrangement for DBMX1.

Internal clocks are only used when we need to test embedded PLL itself. Most of the defective oriented tests, such as those of I/O, IDDQ, TIC, stuck-at SCAN, JTAG and eSRAM bitmap, use a single external slow clock (less than 100MHz) bypassing the embedded oscillators (OSC32K and OSC16M) and PLLs (MCUPLL and USBPLL) in order to maximize the circuit coverage. For the speed coverage, at-speed external 100MHz clock bypassing embedded PLLs is used for testing timing sensitive vectors generated from assembly code simulation, such as those of SDRAMC, WEIM, DMA and ESI. This clock is also adopted for eSRAM BIST and ASP test at speed. In asynchronous mode, ARM920T core can run at the speed up to 200MHz while the other modules are running at 100MHz or lower.

Although the low cost ATE that we selected for DBMX1 is capable of test at 100MHz data rate (CLK) per pin, to test the embedded maximum speed of ARM920T by external 200MHz clock requires a more accurate EPA of the input clock edges and a finer pulse generation (less than 5nS). Therefore, an on-DIB clock doubling module [8] is implemented to multiplex two 100MHz clocks (CLK) with 50% duty cycle each and 90% phase difference. Figure 4 illustrated the block diagram of this on-board clock multiplexing module comprised by five additional channels, two for multiplexing of two 100MHz input clocks (CLKA and CLKB), two for driving level control (VIH and VIL) and one for calibration (CLKC). The advantage of such structure is to control the drive level and edge of the clock output (CLKO) at a ratio of R between 1 and 2 (*R=Fclko:Fclk*). Any ratio can be obtained as long as there are enough edge sets available. But the accuracy is limited by the minimum pulse width which should be no less than 5nS. As shown in Figure 5, the actual waveform output for CLKO will be 200MHz when *R*=2:1 with just one edge set, while it will be 150MHz when *R*=3:2 with four edge sets used.

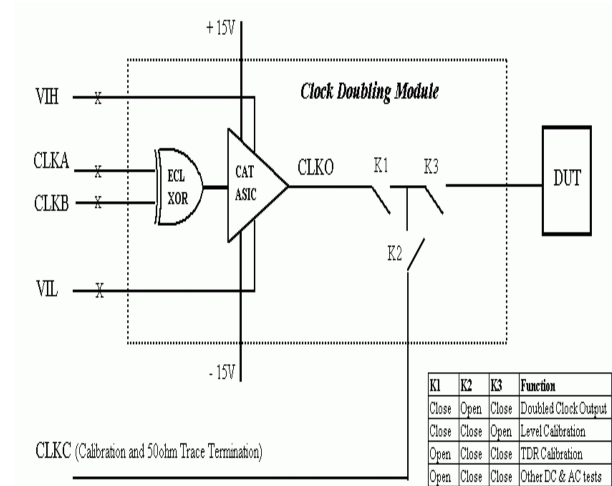
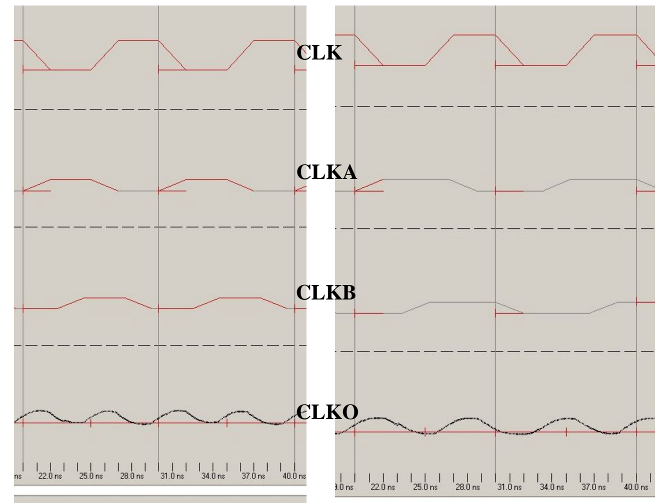


Figure 4. On-DIB clock doubling module by Teradyne.



(a) Fclko:Fclk=2:1 *(b) Fclko:Fclk=3:2*

Figure 5. CLKO output waveforms captured by the built-in digital waveform display tool with low bandwidth.

During the test pattern execution of CLKO, K1 and K3 is closed and K2 is open. Calibration is performed by CLKC when K1 and K2 are closed and K3 is open. TDR calibration is performed when K1 is open and K2 and K3 are closed. This condition can be used for all the other AC and DC tests as well with CLKC. At the beginning, we found some reflection from K2 because the TDR trace is not perfectly matched to the delay inside the

clock doubling module. In order to avoid such reflection, a termination in the CLKC is tried. Figure 6 shows the clock module shmoo plots before and after termination. The symbol “#” stands for that all the test patterns pass at the CLK period (PER – to be doubled at CLKO) and level (VIH) of the input CLKA and CLKB for the clock doubling module while the symbol “.” Means one or certain tests fail at the specific speed and input level for clock module. Before termination, the reflection results that the higher the VIH, the worse the speed performance. After termination, the pass margin can successfully cover the right 10E-8 second PER, which stands for working at 200MHz CLKO frequency.

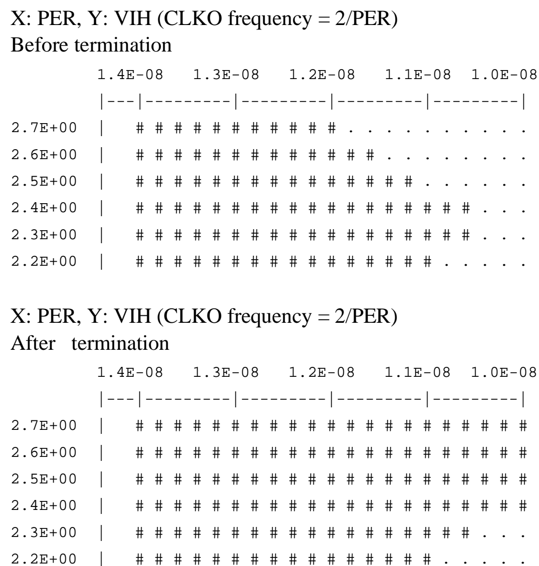


Figure 6. Shmoo plot (PER v.s. VIH) for clock doubling module output before and after termination.

4. Embedded PLL Test

DBMX1 clock module is tested in the following four modes as illustrated in Figure 7.

Path a, Clock bypassing mode:
OSC16M→BCLK (Functional Test Mode 100MHz)

Path b, 32KHz to MCUPLL mode:
OSC32K→PREM→MCUPLL→FCLK (192MHz)

Path c, 32KHz to USBPLL mode:
OSC32K→PREM→USBPLL→BCLK (96MHz)

Path d, 16MHz to USBPLL mode:
OSC16M→USBPLL→BCLK (96MHz)

PLL test is always a challenge for ATE as deep sub-micron technologies keep increasing the complexity of SoC design. It is a tradeoff of test coverage, cost and time. One of the difficulties is the jitter test especially for such highly multiplexed embedded PLL with very low speed input oscillator frequency (32KHz) and very high speed output clock (192MHz). Depending on the purpose of the PLL output clock, the cycle jitter can cause error in CPU data access, misalign bits in data communication, downgrade the speed performance and impact the manufacturing yield. How to effectively test and characterize jitter has been one of the hot topics in the research field in the past decade.

On bench tests, the digital sampling oscilloscope based histogram measurements [9] [15] are normally used to characterize the jitter by shaping the edges against a fixed edge trigger point and analyzing an overlay history of the accumulated signal. Besides, frequency domain based methods with spectrum analyzer and ADC sampling [10] has also been studied. Time domain based over-sampling jitter test methods such as real-time time interval analyzer measurements [11] and repetitive start/stop time measures are too expensive to test the high speed clock because of the strictly required high sampling rate. Therefore, under-sampling jitter test methods are much more popular on ATE application with relaxed requirement of ATE clock rate. These methods include level stamping and time stamping [12] [13]. Level stamping can test jitter in terms of delay and standard deviation statistically by comparing the signal repetitively to a voltage threshold across a defined time interval. Time stamping can mark the time stamp at each defined threshold level and calculate the statistical time interval between stamps. To further reduce the test cost, built-in-self-test (BIST) with build in structure of sampling, counting, calculating and comparing logic has been identified as an effective method recently [14] [16]. But the BIST requires overhead of the extra die area which increases the design complexity and die cost. Therefore, the low cost ATE selected for DBMX1 drove us to develop an under-sampling jitter measurement method for our selected ATE.

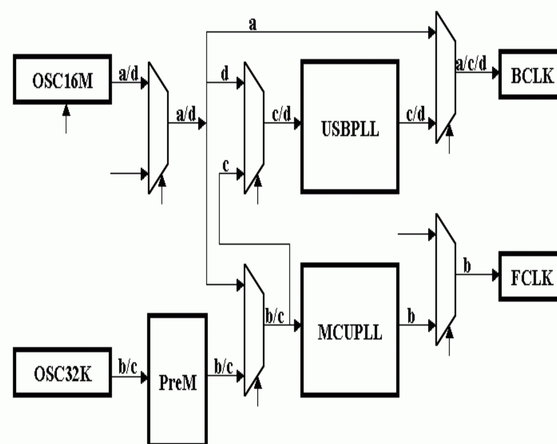


Figure 7. Test modes for DBMX1 clock module.

In the conventional under-sampling test method, the frequency of the targeted output clock must be known and the sampling clock cycle must be exactly the same as or the multiplex of the clock under test (CUT) so that their edges can be aligned. Therefore every time when the strobe edge is placed, the state is predefined pass or fail against the threshold. This state is then used to determine whether the edge of CUT is within the correct region [13]. However, such methods will not work properly in the following situations that normally happened in PLL with very high frequency multiplex ratio between input and output:

- If the frequency of CUT is uncertain, but within certain percentage of variation DUT by DUT;
- If the sample rate can only achieve the best accuracy at certain figure of frequency while the CUT is not able to adjust to that exact frequency;
- If the jitter measurement specification limit is close to the worst edge place accuracy (EPA) of ATE.

In order to test the jitter of such kind of embedded PLL in DBMX1, we developed a method called sliding delta clock with fixed edge strobe. In this method, the sampling clock rate is a best fit to the set of the most accurate ATE clock rates, but with a slight different from that of CUT. The fixed strobe is to avoid one of the variation factors that changing strobes cause more EPA variation. In fact, the cycle difference makes this fixed strobe act as a sliding strobe in the continuous cycles of CUT. Figure 8 illustrates this method. The ATE failure memory is used to record the failure cycle counters against certain threshold voltage. By analyzing the failure sequence, determined by the transition from pass to fail or from fail to pass, we can calculate the period and jitter of CUT.

In our method, if the delta cycle is defined as $\Delta Cyc = Cyc_sample - Cyc_CUT$, $(Cyc_CUT/\Delta Cyc) \times N$ strobes are required for sampling N CUT cycles. The advantage of this method is that the CUT frequency does not have to be predefined in case when the CUT frequency is uncertain. The method only needs to make sure there exists a slight different between the CUT cycle and sampling cycle. The finer the difference, the higher the accuracy, but the longer the test time. If the first pass to fail transition and the first fail to pass transition of CUT cycle number i is defined as PF_i, and FP_i respeciviely as shown in Figure 8, for total N CUT cycles, the *Period_CUT* can be calculated by (6). There are two ways to calculate *Jitter_CUT*, one to analyze the adjacent transition (7) and the other to analyze the difference of duty cycle ratio (8). The first method is relatively inaccurate though simple and stable because it is less impacted by edge skew, while the second method is more accurate in terms of methodology, but relatively unstable in implementation. When N is sufficient big, a histogram of jitter distribution can be plotted. However, there is a limitation of the depth of the ATE fail vector capture memory, i.e. 256K, 512K or 1M. Therefore, segmentation pre-process is used to confine the size of each segment within the limitation of capture memory and a pattern re-start or re-burst is required segment by segment. For the clock with uncertain phase that is generated out of embedded PLL, re-burst can cause the segment alignment issue in the second jitter measurement method. Therefore, a keep live pattern procedure is being implemented to keep the PLL input clock running continuously between two adjacent segments so that the edge information will be aligned among the whole test execution.

$$Period_CUT = \frac{\sum_{i=1}^{N}\left(\frac{(FP_i + PF_i)}{2} - \frac{(FP_{i-1} + PF_{i-1})}{2}\right)}{N} \quad (6)$$

$$Jitter_CUT = \frac{Maximum(FP_i - PF_i)}{Period_CUT} \times 100\% \quad (7)$$

$$Jitter_CUT = \frac{Maximum(FP_i - FP_i) - Minimum(FP_j - FP_j)}{Period_CUT} \times 100\%$$

$$where\ 0<i<N\ and\ 0<j<N \quad (8)$$

Figure 9 shows the DBMX1 experiment result with a 100MHz fixed edge strobe rate to test a 99MHz clock from embedded USBPLL and a 198MHz clock from embedded MCUPLL. The captured datalog showed that the jitter distribution calculated by equation (8) spread wider than that of equation (7) because the first equation contains more edge information and the equation has less skew impact to the measuring stability. Although the ATE that we use can only guarantee 500ps EPA, the fixed strobe method is able to minimize the variation of EPA. But over 1% jitter rate of the ATE pattern execution clock will also limit the accuracy of our measurement result.

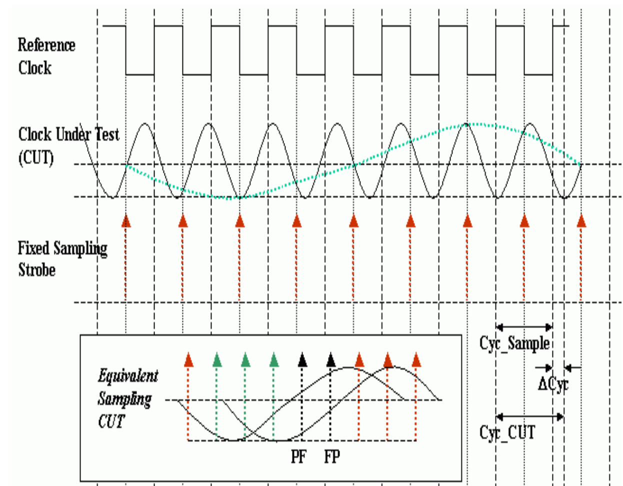


Figure 8. Jitter test using sliding delta clock with fixed edge strobe.

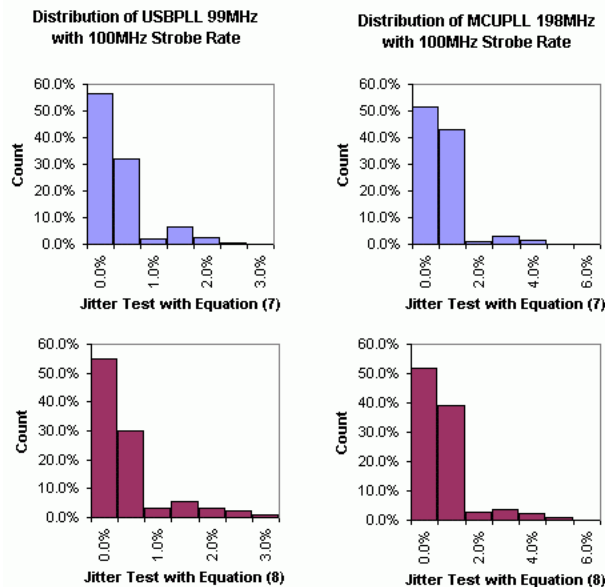


Figure 9. Jitter histogram of a 99MHz USBPLL and a 198MHz MCUPLL measured with 100MHz strobe rate.

5. Embedded ASP Test

Although the mixed signal circuits like embedded PLL can be tested purely on digital ATE channels, the test for embedded ADC and DAC will require a mixed signal option inside ATE. DBMX1 integrates a 16-bit sigma-delta touch panel ADC and a 16-bit sigma-delta voice band CODEC (both ADC and DAC). As a conventional static test method, a linear ramp generated by ATE is input to the analog end of ADC or the digital end of DAC for pen applications. By capturing the response at digital end of ADC or the analog end of DAC, the characteristics, such as offset, gain, differential non-linearity (DNL) and integral non-linearity (INL) can be obtained. For voice application, the linear ramp input is replaced by a pure sinusoidal waveform with which the characteristics, such as signal-to-noise and distortion ratio (SINAD), total harmonic distortion (THD) and spurious free dynamic range (SFDR) can be computed out by ATE [17].

However, just to test this ASP, it takes not only the test time, but also the expensive investment of that MSO, which cost almost one-fourth of that of our selected low cost ATE. Although there are DFT researches for testing ADC and DAC [18], this normally increases the die area overhead. Therefore, we propose a loop-back self-test approach that asks for zero die area overhead.

The first scheme is called the semi-BIST or partial-self-test as shown in Figure 10. In semi-BIST, ATE feeds the vectors of a digitized waveform, i.e. one cycle digitized sinusoidal waveform of 1024 samples to voice DAC. The analog output of the voice DAC is then looped back to the input of either voice ADC or pen ADC via relay or switch. The digital output of these ADCs is received and calculated by ATE with DSP processors or procedures. ATE finally makes a screening decision. Such digital to digital loop avoids any analog signals to or from ATE so that a pure digital ATE can be used. But some low cost ATE has the limitation of calculation speed especially for FFT. Therefore, a full-BIST scheme is proposed as shown in Figure 11. The difference is to do the DSP calculation with the powerful embedded ARM920T processor together with the embedded DSP accelerator module so as to reduce the overhead of ATE furthermore. The test time of BIST method is targeted to be shorter than that of the traditional open loop measurement with mixed signal ATE or options because the ADC and the DAC are to be tested in the mean time with a single launch of sourcing and capturing the same waveform.

However, there exist shorts for such loop-back test with homogenous embedded sigma-delta ADC and DAC. The case when noise or harmonic distortion of ADC and DAC has the same frequency bins but the different phases may cause some cancellation that will result in the better reading of SINAD or THD than what the ADC and DAC actually possess. To select different clock rates of sigma-delta ADC and DAC, to strictly synchronize the input waveform of DAC and ADC, and to correlate to the characterization from the mixed signal ATE can minimize and calibrate this effect. The study is still ongoing.

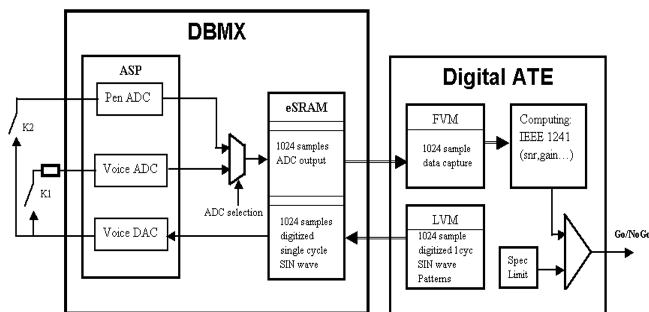


Figure 10. Semi-BIST for DBMX1 ASP.

6. Conclusion

This paper has discussed the challenges that we were facing when we defined the low cost test strategies for DragonBall™-MX1, an ARM920T core based mixed signal SoC. After we evaluated several proposed ATE test solutions by developing and analyzing the model of test equipment related test cost, we selected the very low cost ATE for this complex silicon. We then succeeded in running at-speed 200MHz digital tests with the slower 100MHz digital ATE clock and the on-DIB clock doubling module in test production. To minimize the impact from edge skew, a new under-sampling PLL jitter

test approach with sliding delta cycle and fixed strobe was presented with the satisfied experimental result and implemented in the silicon characterization tests as well. Furthermore, in order to avoid investing mixed signal option in testing voice band ADC and DAC, we proposed the loop-back self-test methods. These approaches will enable us to achieve all the mixed-signal tests on a pure digital low cost ATE. But more researches need to be continued to further enhance the measurement accuracy of PLL jitter test and minimize the cancellation of noise and harmonic distortion in ADC and DAC self-test.

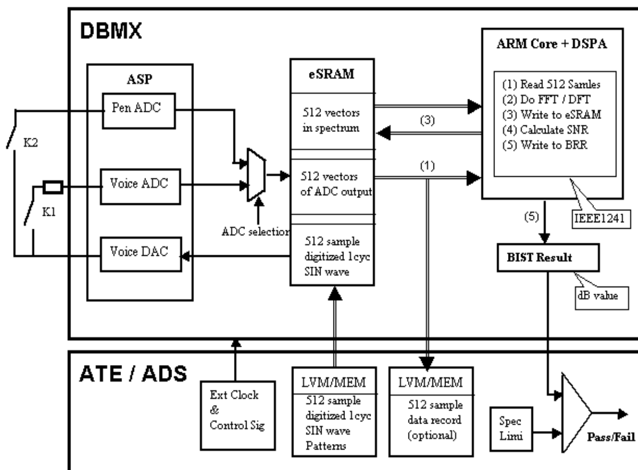


Figure 11. Full-BIST for DBMX1 ASP.

7. Acknowledgements

The author would like to acknowledge Craig Shields and Gladys Tang from Teradyne for providing tester information.

8. References

[1] "MC9328MX1 Integrated Portable System Processor User's Manual", Motorola SPS Asia Pacific, 2002.

[2] Semiconductor Industry Association (SIA), "The International Technology Roadmap for Semiconductors", 2001 edition, International Sematech, Austin, Texas, 2001.

[3] A.C.Evans, "Applications of Semiconductor Test Economics and Multisite Testing to Lower Cost of Test," IEEE International Test Conference, pp.113-123, 1999.

[4] H. Vranken, T. Wayers, H. Fleury and D. Lelouvier, "Enhanced Reduced Pin-Count Test for Full-Scan Designs," Proc.European Test Workshop, 2001.

[5] A. Khoche, R. Kapur, D. Armstrong, T.W. Williams, M. Tegethoff and J. Rivoir, "A New Methodology for Improved Tester Utilization," Proceedings of IEEE International Test Conference, pp.916-923, 2001.

[6] "J750 Hardware Specifications", Teradyne, 2001.

[7] Andrew Burdass, Gary Campbell, Richard Grisenthwaitc , David Gwilt, Peter Harrod and Richard York, "Embedded Test and Debug of Full Custom and Synthesisable Microprocessor Cores", IEEE International Test Conference, 2000.

[8] John Whittaker and Tomohiru Murayama, "High Speed Clock and Data for the J750", Teradyne User Group, Teradyne Inc., 2001.

[9] T.J. Yamaguchi, M. Soma, M. Ishida, T. Watanabe and T. Ohmi, "Extraction of Peak-to-peak and RMS Sinusoidal Jitter Using an Analytic Signal Method", Proc. IEEE VLSI Test Symposium, Montreal, Canada, May, 2000.

[10] Sasikumar Cherubal and Abhijit Chatterjee, "A High-Resolution Jitter Measurement Technique Using ADC Sampling", IEEE International Test Conference, 2001.

[11] T.J. Yamaguchi, M. Soma, D. Halter, J. Nissen, R. Raina, M. Ishida and T. Watanabe, "Jitter Measurements of a PowerPC™ Microprocessor Using an Analytic Signal Method", IEEE International Test Conference, 2000.

[12] Wajih Dalal and Daniel Rosenthal, "Measuring Jitter of High Speed Data Channels Using Undersampling Techniques", IEEE International Test Conference, 1998.

[13] Peter Huber, "PLL Jitter Measurement on J750 Test System", Teradyne Users Group, 2000.

[14] Seongwon Kim and Mani Soma, "Test Evaluation and Data on Defect-Oriented BIST Architecture for High-Speed PLL", IEEE International Test Conference, 2001.

[15] Keith A. Jenkins and James P. Eckhardt, "Measuring Jitter and Phase Error in Microprocessor Phase-Locked Loops", IEEE Design and Test of Computers, 2000.

[16] Benoit R. Veillette and Gordon W. Roberts, "Stimulus Generation for Built-In-Self-Test of Charge-Pump Phase-Looked Loops", IEEE International Test Conference, 1998.

[17] "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters", IEEE, 2001.

[18] V. Zagursk, A. Gertners, "Test Technique for Embedded ADC", Circuits and Systems, 1998.

[19] Nag P.K., Gattiker A., Sichao Wei, Blanton R.D., Maly W., "Modeling the economics of testing: a DFT perspective", Design & Test of Computers, IEEE , Volume: 19 Issue: 1 , Jan.-Feb. 2002 Page(s): 29 –41.

[20] J. Johnson, "Is DFT right for you?", Test Conference, 1999. Proceedings. International , 28-30 Sept. 1999 Page(s): 1090 –1097