

ULTRA LOW COST LINEAR TESTING

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Abstract

The advent of high quality PC based instruments, combined with the normal day to day skills of linear test engineers, eliminates the need for general purpose linear testers in many cases. Linear applications are dominated by custom DUT boards; therefore a few application card tricks and some PC instruments can replace the general purpose linear tester and significantly reduce cost and size without sacrificing performance. This paper explores one example of a simple PC instrument based tester for an industry standard Op Amp, and then examines how one might package the solution into a parallel multi-site test solution.

1. Introduction

For the past 20 years the ATE industry has been using general purpose linear testers for amplifiers, comparators, converters, and other analog devices. However, the general purpose tester has traditionally been supplemented with family boards, specialty instruments, and custom load boards.

In terms of the test development process, most of the time to complete an application was taken up by the custom circuitry and the process of hardening the application for manufacturing: managing repeatability, correlating multiple testers, and correlating to bench measurements and simulation.

The general purpose tester served as a very expensive substrate for custom application solutions. Even when a solution was made general purpose and reusable, each time the manufacturing floor had to increase capacity, a very expensive substrate had to be purchased to support the application solution, thus increasing the cost of test in order to maintain flexibility.

In today's environment, with many ultra low ASP analog devices, an extremely low cost custom solution designed around parallel handling equipment may be the only way to reduce the cost of test.

The question this paper asks is what would an application solution be like if the expensive general purpose substrate were replaced with today's low cost instrumentation?

- Does today's instrument technology make this practical?
- Can the resulting accuracy and repeatability match the "general purpose" tester?
- Would test development time change?
- What would mechanical integration look like?
- Would the solution scale to many sites?

The author took a pragmatic approach to this question rather than a theoretical one: an attempt was made to create an application for an industry standard Op Amp with today's off the shelf instrumentation.

2. The Design of the Tester

2.1 Controlling the application hardware

Almost all Op Amp solutions use a conventional Op Amp Loop circuit on the application board, family board or custom instrument that is close to the DUT. (An Op Amp Loop is a feedback circuit that converts data sheet parameters into measurable voltages, i.e. voltages that are well above the noise floor). The loop is then controlled by relay driver boards and VIs in the general purpose tester backplane.

The first choice that had to be made was whether to put DACs and ADCs on the application board or not. There are many inexpensive instruments available today that contain these functions, so it did not make sense to put them on the application board. A search turned up boards in PXI technology that met the requirements. However, what also turned up were instruments that also contained digital IO and counter circuits.

An instrument with DACs, ADCs, digital IO, and a timer/counter is almost a complete tester if one can test without a general purpose VI. In the case of an Op Amp, only one quadrant is needed for the positive supply pin, and one for the negative supply pin.

Moreover, some of the PXI instruments also come in PC Card packaging. The card that was picked was a National Instruments DAQCard 6036E. This card contains a 16 bit ADC with an analog multiplexer/scanner front end, gain amp, two DACs, a timer/counter, and 8-bit DIO.

This card was a good match for the goal of testing one quad amplifier with off the shelf instruments. Having a single card for one device means multi-site can be organized in slices, where each site has one instrument card to support one application card; a nice scaleable solution, given that there is a PXI version of the same card that plugs in place of the PC Card without any application card changes or software changes.

The overall hardware for a single site version included:

- A laptop computer
- A PC Card instrument
- An application card
- A cable that connects the PC Card to the application card

A dual site would need a second PC Card and cable, and a second application card. The simplicity of an application card per site lends itself to innovative mechanical arrangements. For example, stacking application cards in clusters that can test wafer die in long chains. Because there is no large test head to deal with, the application cards can be small and dense.

2.2 Designing the Application Card

The application card implemented a conventional Op Amp Loop. Relays were used for the bias current tests to keep leakage to a minimum, and analog switches were used everywhere else. The 8-bit bus was broken in to a 4-bit data bus, a 2-bit address bus, and a clock. A simplified version of the loop without power supplies is shown in Figure 1.

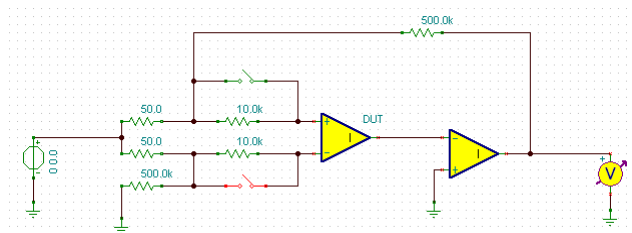


Figure 1

The OP07 Op Amp requires +/- 15 Volt supplies, but the DAQCard DACs have a +/- 10 Volt output. Therefore, a high voltage Op Amp with a gain of 2 was used for each supply. One Op Amp was inverting so that both supplies of the DUT could be controlled by the same DAC.

The second DAC was used for all other reference voltages, which meant using analog multiplexers and switches to route the DAC output to the correct circuit nodes. This required all tests to use only one voltage setting at a time.

The ADC on the DAQCard has 8 differential or 16 single ended inputs, so no multiplexers were needed on the application card. Differential inputs were used wherever noise might be an issue, and the Op Amp loop itself kept most signals well above noise levels.

The design used precision components so that calibration of the application card was not necessary.

2.3 Measurement Control

General purpose linear testers have hardware control over settling times via a general purpose timers and tight IO timing control, or via use of hardware timers and hardware triggering. General purpose multi-tasking desktop operating systems used to control instruments have no precise timing control over IO operations. This can lead to unrepeatable measurements. The solution is the use of instrument triggering.

The DAQCard contains external and internal triggers for the DACs and ADC, and also contains a counter. These timing circuits were used to control instrument timing. Each test followed a common pattern:

- Store power supply values in the DAQCard
- Store the application voltage in the DAQCard
- Setup the relays, analog switches, and multiplexers
- Setup the trigger and timer
- Fire the measurement
- Power down the DUT

The DUT remained powered down until the measurement was fired. Firing the measurement set the supply voltages, waited a fixed time for the DUT to settle, and then made the measurement/s. Power down timing was not controlled.

A side effect of this technique was that tests could be run in any order, because part of a test was powering up and down the device. Furthermore, it also guaranteed that relays were never hot-switched, nor the device supplies taken up/down during setup, e.g. from some auto relay protection system.

Figure 2 shows the schematic representation of the setup and trigger mechanism.

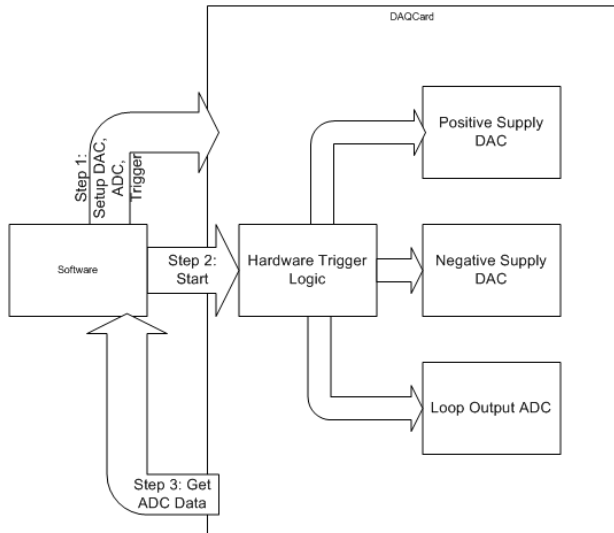


Figure 2

3. Experimental Results

3.1 Practicality of Custom Solutions

Building a custom solution proved to be quite easy. All purchases were done via the internet with a credit card.

Instruments and specifications in the PXI and PC-Card format were easy to find and purchase on-line. Many were also available at on-line auctions.

One reason the NI6036E was used was that it came in PC-Card, PXI, and had a prototyping board available. This allows one to prototype critical circuits and program them on a prototype board and then smoothly move to a layed out board using the same software.

There were two vendors that offered schematic capture and board layout tools that were internet linked to their fab. Once the layout was complete, the software took a credit card and the boards were delivered within 3 days. A printed circuit board vendor with a business model setup for prototyping was perfect for this solution. Application board solutions are usually built in very low quantities, so turn around time is more important than cost.

All the connectors, the power supply, and the parts were ordered on-line and were delivered within 5 days.

Software that ran the hardware was build with off the shelf compilers and GUI builders.

However, the example solution built for this paper did not address mechanical integration, e.g. handlers and probers. Integration with handling equipment would be easy in so far as one already had infrastructure in place that defined connectors, frames, mounting brackets, etc.

3.2 Development Time

The development time for the example solution is broken down in Table 1.

Task	Time (days)
Select and purchase instruments	2
Create schematic	4
Prototype and debug circuit	5
Layout board	5
Order and receive boards and parts	5
Assemble board	1
Write test program	5
Tune program for accuracy, test time, etc	2
Total	29

Table 1

It would be difficult to draw any general conclusions from this example. None the less, the author's experience suggests that building the custom solution was comparable in effort to building a new solution on a general purpose tester. For example, if one had a general purpose analog tester and no previous Op Amp solution board, the time it would take to build one for the general purpose tester would be very similar to building a customer tester, assuming that all the instruments one needed to buy were available.

The author's conclusion is that if one can use standard instruments, and one has an infrastructure for mechanical integration, and one has support from the hosting organization to leverage online purchase mechanisms, then the calendar time it takes to produce an application solution from scratch is about the same whether using instruments or general purpose testers.

In many organizations tester time is hard to get. There is always pressure to maximally utilize the equipment for production because of its huge cost. In that environment, low cost custom solutions are attractive, because low cost instrumentation allows a company to divide the capital investment between engineering and production more dynamically and each part of the organization has better control over its resources.

3.3 Duplication Cost

Table 2 shows the cost breakdown of the example solution.

Item	Amount
NI6536E	\$900.00

Cable	\$100.00
PC Board Fab	\$350.00
Parts	\$150.00
Total	\$1500.00

Table 2

If the solution were scaled to 8 sites, the total cost would be \$12,000.00. A typical general purpose tester that could test 8 sites would run between \$150,000.00 and \$400,000.00 depending on whether it was purchased used or new.

The cost differential is at least 10X. The author admits it is not always possible to build a custom solution, and therefore one will always need some general purpose testers around. But, when it can be done, the capital savings can be huge.

3.4 Measurement Performance Analysis

The specified accuracy of the NI6036E DAQCard is about 1mV when using the 10V range, or about 0.01%. Assuming an ideal loop with no error, the error reflected back to the op-amp input is the measurement error divided by the gain. The low gain setting is X1000, so the measurement accuracy is 1uV or 0.0001%. For the high gain of X10000, the error is 0.1uV or 0.00001%.

Now, taking the loop gain error due to resistor mismatch into consideration will show that it dominates the instrument error. The loop has 0.5% resistors, so the gain error is approximately 1%. Over a 10V range that is 100mV. When reflected back to the input, the result is 100uV, 100 times larger than the error due to the instrument.

3.5 Measurement Repeatability Analysis

Initial repeatability data was created by taking several devices and running them 100 times. A delay of 1 second was used between runs to remove thermal effects. Many amplifier input offset voltage is very sensitive to temperature change, and tests that load the output increase the DUT temperature. The delay allows the DUT to cool off between runs.

The means are calculated and becomes a reference point for comparing differences between fixtures, testers, and between typical values and limits. Standard deviations are calculated and give an indication of repeatability of each measurement. Accuracies are calculated by taking the application circuit accuracy (resistor tolerance, amplifier offset, etc) and instrument accuracy and calculating a worst case value at the limit of a parameter.

Guard bands are calculated by taking 6 sigma, which represents the spread with outliers somewhat discounted statistically (as opposed to using max value minus min value), and adding in the accuracy. The goal is to produce a number that guarantees that devices that pass final test, will never fail quality test. Only one fixture was built, so fixture to fixture differences are not accounted for in this data.

Table 3 (Maxim OP07E - Device 1) and Table 4 (Maxim OP07E - Device 2) show the results for an OP07.

Parameter	Test Results			Quality		
	Mean	Std	Units	6 Std %	Accuracy	Guardband
Input Offset Voltage	49.817	0.0017	uV	0.0102	0.9500	1.28%
Input Offset Current	0.882	0.0200	nA	0.1200	0.2280	9.16%
Input Bias Current (+)	0.072	0.0226	nA	0.1356	0.0800	5.39%
Input Bias Current (-)	0.953	0.0114	nA	0.0684	0.0800	3.71%
Supply Current (Vcc)	2.388	0.0018	mA	0.0108		
Supply Current (Vdd)	2.433	0.0015	mA	0.0090		
Large Signal Voltage Gain	268.372	2.0760	V/mV	12.4560	4.5385	9.71%
Common Mode Rejection Ratio	0.138	0.0010	uV	0.0060	0.2500	5.12%
Supply Voltage Rejection Ratio	119.975	0.4139	dB	2.4834	0.1722	2.83%
Output Swing (+)	13.207	0.0007	V	0.0042		
Output Swing (-)	13.432	0.0007	V	0.0042		

Table 3 (Maxim OP07E - Device 1)

Parameter	Test Results			Quality		
	Mean	Std	Units	6 Std %	Accuracy	Guardband
Input Offset Voltage	51.580	0.0023	uV	0.0138	0.9500	1.29%
Input Offset Current	0.897	0.0236	nA	0.1416	0.2280	9.73%
Input Bias Current (+)	0.057	0.0135	nA	0.0810	0.0800	4.03%
Input Bias Current (-)	0.953	0.0163	nA	0.0978	0.0800	4.45%
Supply Current (Vcc)	2.385	0.0019	mA	0.0114		
Supply Current (Vdd)	2.430	0.0015	mA	0.0090		
Large Signal Voltage Gain	269.016	2.1020	V/mV	12.6120	4.5385	9.80%
Common Mode Rejection Ratio	0.111	0.0092	uV	0.0552	0.2500	6.10%
Supply Voltage Rejection Ratio	137.906	3.7060	dB	22.2360	0.1722	23.84%
Output Swing (+)	13.200	0.0008	V	0.0048		
Output Swing (-)	13.433	0.0006	V	0.0036		

Table 4 (Maxim OP07E - Device 2)

Notice that the PSRR for device 2 has a guard-band of 24%. This is because the standard deviation is very high. This particular device has a very high PSRR, 137 compared to 119 for device 1. The measurement is so small, that it will not be repeatable. Therefore, this number is tossed out. Looking at the other guard-bands, the worst case is about 10%.

3.6 Measurement Correlation Analysis

Correlation data was created by asking a major semiconductor manufacturer to test 5 devices 100 times each using their production tester.

The same 5 devices were then tested 100 times each on the ultra low cost tester, and then the mean and standard deviation were compared.

Figure 3 shows the repeatability for two devices. “ULC Tester” refers to the low cost tester proposed here. “Current Tester” refers to the tester from the semiconductor manufacturer.

Test	Device 1		Device 2		Units
	ULC Tester	Current Tester	ULC Tester	Current Tester	
Input Offset Voltage	0.557790	2.451000	1.525000	1.708000	uV
Input Offset Current	18.246000	17.500000	23.298000	12.000000	pA
Input Bias Current (+)	0.100200	0.032500	0.084884	0.030400	nA
Input Bias Current (-)	0.088400	0.037200	0.073942	0.030100	nA
Supply Current (Vcc)	1.737000	0.258000	1.534000	0.164000	uA
Large Signal Voltage Gain	389.150000	3287.000000	2608.000000	17701.000000	V/mV
Common Mode Rejection Ratio	0.039700	0.162000	0.044320	0.270000	DB
Supply Voltage Rejection Ratio	0.238000	0.576000	0.389200	0.952000	DB
Output Swing (+)	0.000681	0.000627	0.000832	0.000359	V
Output Swing (-)	0.000675	0.000620	0.000673	0.000390	V

Figure 3

Most of the tests have similar repeatability, suggesting that the low cost tester performs well. The exceptions require explaining. The gain test again raises its ugly head. We are still dealing with very small offset changes down in the noise and far away from the limit. Again, what really matters is the repeatability near the limit. Without near bad devices, there is not much we can do but make an estimate near the limit. The limit on this device is 0.7V/uV. With a +/- 10V swing, that represents a 28.5uV change in offset. A gain test requires two offset measurements; therefor using device 2, double the standard deviation is 3uV. A six sigma guard band of 18uV is fairly large compared to the 28.5uV change in offset near the limit.

The means were also compared in Figure 4 and Figure 5.

Test	Device 1			Units
	ULC Tester	Current Tester	Error	
Input Offset Voltage	74.57	60.95	-22.36%	uV
Input Offset Current	97.84	40.70	-140.40%	pA
Input Bias Current (+)	-6.15	-6.20	0.87%	nA
Input Bias Current (-)	-6.25	-6.24	-0.08%	nA
Supply Current (Vcc)	398.31	394.32	-1.01%	uA
Large Signal Voltage Gain	7418.00	17348.00	57.24%	V/mV
Common Mode Rejection Ratio	109.62	109.94	0.29%	DB
Supply Voltage Rejection Ratio	113.93	120.40	5.37%	DB
Output Swing (+)	13.46	14.31	5.94%	V
Output Swing (-)	-13.35	-14.09	5.31%	V

Figure 4

Test	Device 2			Units
	ULC Tester	Current Tester	Error	
Input Offset Voltage	58.76	51.57	-13.94%	uV
Input Offset Current	101.82	6.30	-1516.17%	pA
Input Bias Current (+)	-5.97	-6.05	1.32%	nA
Input Bias Current (-)	-6.07	-6.05	-0.25%	nA
Supply Current (Vcc)	414.50	410.45	-0.98%	uA
Large Signal Voltage Gain	18633.00	5631.00	-230.90%	V/mV
Common Mode Rejection Ratio	111.75	111.89	0.13%	DB
Supply Voltage Rejection Ratio	117.55	124.61	5.67%	DB
Output Swing (+)	13.45	14.31	5.97%	V
Output Swing (-)	-13.33	-14.09	5.42%	V

Figure 5

The offset test, which is a key test because other tests are based on offset measurements, correlated within about 20%. It was difficult to achieve this difference. The first time data was taken, the difference was over 100%. The problem was caused by a 60uV thermal emf difference between the input relays. The software was leaving the relays powered on between runs, and the coil of the relay heated the contacts and caused the emf difference to shift. Turning off the relays between runs, and allowing a long wait time between runs produced the current data.

Emf problems may also account for errors in the offset correlation. However, until the relays are replaced with low emf versions, the author will not know the result.

The gain values do not correlate well at all. Given the problems with repeatability, this is no surprise. My conclusion is that gain tests are difficult for any tester, and anyone building an op-amp tester will have to deal with this problem whether using a general purpose tester or a custom one. All the problems related to making the measurement are in the op-amp loop, not the measurement system.

The swing voltages have a significant error considering that the measurement is easy to make. The author suspects the test conditions used by the semiconductor manufacturer are different than the low cost tester. The author used the setup in the data sheet which calls for a typical value of +/-13.8V; half way between the two values. The most likely source of error is a difference in the load.

Overall, the correlation is encouraging. Getting two 60uV measurements to work on two fixtures with different designs is not easy. Experience with previous correlations of this type suggest that a combination of low emf relays and a more effort at discovering differences between fixtures will result in adequate results.

4. Limitations

The simplicity of the hardware design placed some real limitations on what can be tested. The important limitations were:

- The small address space on the application card prevented building a MUX for continuity testing. An alternative would be to use the IO of the DAQCard as a serial bus and give up some IO performance.
- Setting registers required two writes to the IO port, because one bit on the port acted as a clock bit.
- The positive and negative DUT supply voltages could not be controlled independently
- The application board did not support a wide range of current measurements, offset measurements, or loads; so the solution was not general enough to handle all types of Op Amps.
- Measurements requiring more than two DACs at a time were not possible unless the application card derived another voltage from one of the two DACs.

Basically, the application card was specific to the one device under test. A more general purpose application board is conceivable, but then more instruments would be needed to support it.

The bottom line is that a custom solution can not bail one out of trouble like a general purpose tester can. Therefore, one has to know their requirements well and properly design the custom solution to reduce the risk a late design change.

5. Packaging Solution

The experimental results demonstrated that it is possible to build a test solution with one PC Card instrument and an application board as shown in Figure 6.

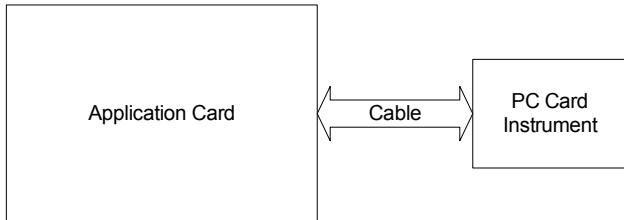


Figure 6

This is great for prototyping or single site applications, but in order to scale the solution to multiple sites, it must be re-packaged. The simplest packaging leverages the simplicity of one card pair per site. In other words, the card pair becomes a test solution slice.

The first step towards this packaging involves replacing the PC Card with a PXI card, because most computers only host 1-2 PC Card slots, but there are 8-16 slot PXI card cages available. The DAQCard-6036E has a PXI equivalent. The PXI version even uses the same cable connector as the PC Card version.

The second step is to create a backplane that can hold both the PXI card and the application card. The simplest organization is a two row backplane shown in Figure 7.

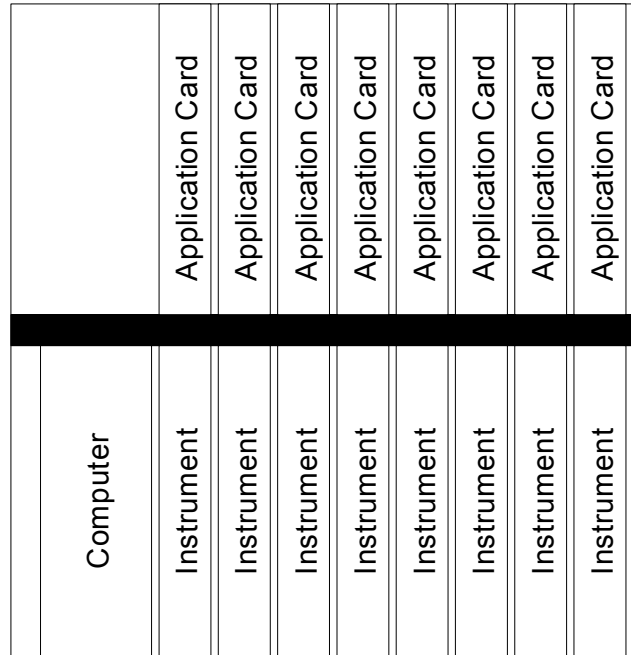


Figure 7

Each instrument in the lower backplane would have a cable connected to the application card just above it. The computer in the lower backplane would control the instruments.

To provide connectivity to each of the devices (site), the upper backplane would act as a routing and connectivity platform for the handling equipment as show in Figure 8.

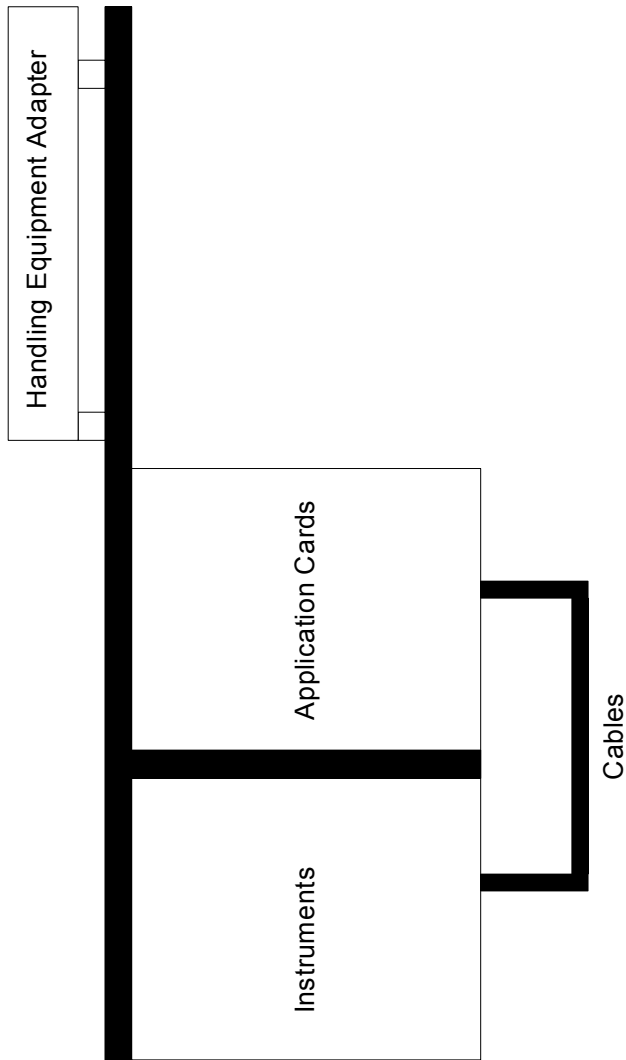


Figure 8

The end result would be a parallel tester. Each application card would test one device. An industrial version of this backplane system is shown in Figure 9. This system has a PXI backplane in the lower half of the box, and an application card backplane in the upper half of the box. This cage can host a CPU, or MXI card with an external computer.

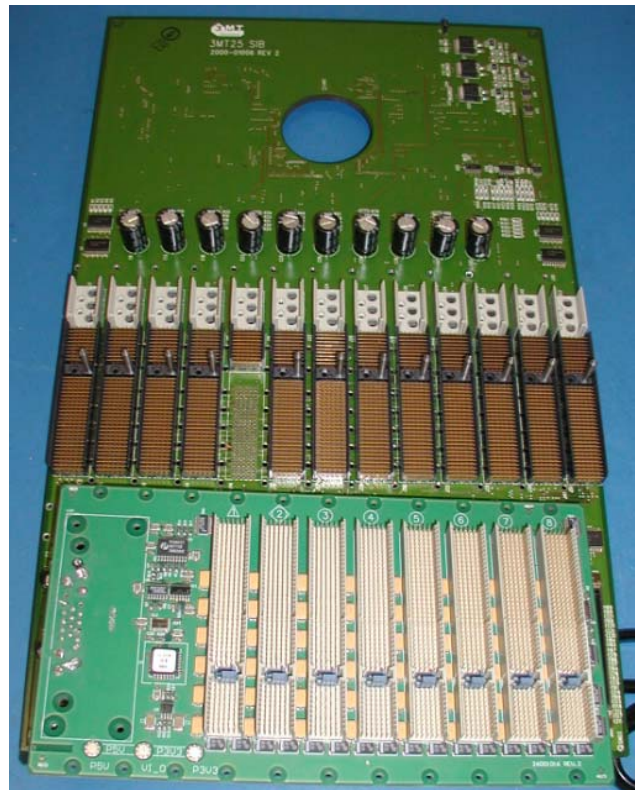


Figure 9

6. Discussion

The “application is the tester” approach requires a test engineer that knows how to design hardware. I have yet to see anyway around this fact when it comes to linear test, or perhaps more accurately analog test.

In many cases, the mechanical aspect of integrating the tester dominates the solution. For example, much of the real magic of RF testing is DUT fixturing and calibration, especially when testing wafers. Many times the application solution reflects the fixturing requirements, for example, an IBM paper [3] describes a handler approach where the DUT is moved from test location to test location and at each location, one test is performed.

For many ultra low ASP analog devices, an extremely low cost custom solution designed around parallel handling equipment may be the only way to reduce the cost of test.

8. Conclusions

Building an “application is the tester” solution was no more difficult than using a general purpose tester. It took no more engineering effort, and cost considerably less.

Since there is no huge mechanical form factor forced on the engineer, there is great latitude and opportunity to integrate parallel solutions into handling equipment. Additionally, some industry standard semiconductor ATE backplane systems for instruments can handle many integration needs.

In reality, linear test engineers have been treating the general purpose tester like a rack of instruments anyway, because so much application circuitry is needed. This paper suggests that a platform that embraces that reality by leveraging commercial off the shelf instruments better serves the needs of the industry.

All that is required are the traditional linear test engineering skills, a mind-set that allows one to let go of the big box.

9. Acknowledgements

I would like to thank Gordon Robinson, whose critical comments keep me intellectually honest.

10. References

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