Mitigating the Effects of The DUT Interface board and Test System Parasitics in Gigabit-Plus Measurements

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Abstract

This paper discusses the issues associated with removing the effects of the measurement path in very high speed measurements. Of critical concern is deterministic jitter caused by the interaction between the measurement path and the device under test. While individual components causing jitter in the measurement path can be well characterized and simulated, simple methods of compensating for measurement path error cannot be applied. This paper explores this issue and suggests two complementary solutions for addressing such jitter.

1.0 Introduction

Much of the focus of the application series in ITC has been on the cost issues associated with the device interface -- especially in terms of yield and quality. Even as the industry moves more and more to "guaranteed by characterization" approaches, at some point a device must be placed on an interface board and a test system. Thus, the need to mitigate the effects of the measurement path is critical.

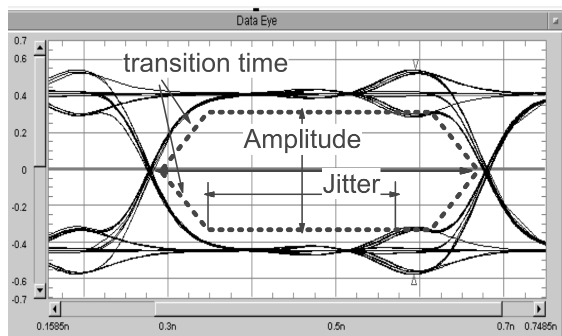

Figure #1 Transmitter Data Eye

Very high speed devices are best described in terms of their data eye. For a transmitter, transition time, amplitude and jitter are the most important data eye parameters. The question for transmitter test is, "How much does the measurement path degrade the device under test?" Likewise for a receiver, sensitivity to jitter, amplitude attenuation, and reduced transition time is critical. The question for the receiver is, "How much does the stimulus path change the data input?" Figure #1 shows the data eye concerns. While compensating for transition time degradation and attenuation is well understood, compensating for jitter is not.

A discontinuity due to an interconnect, relay, bond wire, etc. in the measurement path causes deterministic jitter[1]. The electrical distance (in time) between two discontinuities influences the amplitude of the data eye when the discontinuities are physically close together. However, when they are separated in time by more than 1/2 of the data period, the reflections/ re-reflections from the discontinuities add or subtract from subsequent incident edges, thus causing jitter. In practical test systems this is almost always the case[2]. The discontinuities include:

i. the device output/ input impedance itself,
ii. the DUT interface board -- i.e. vias and launchings,
iii. the test system path -- i.e. relays, bond wires, protection diodes, and terminations.

If a test system is predictable and repeatable, then one often assumes that correction for the measurement system is easy and possible. This, however, is not the case because the jitter

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mechanisms violate important assumptions for standard methods of statistical analysis.

The device being measured *interacts* with the measurement path on three key levels. First, the output impedance (input impedance) of the device under test (DUT) determines the re-reflected energy in the measurement path. In a transmitter, for example, the initial edge travels down the measurement path. As its energy hits discontinuities, a portion of that energy travels back toward the DUT. The DUT output impedance (i.e. reflection coefficient) then determines how much energy reflects back -- the aforementioned re-reflection. There will be variation from device to device. The DUT I/O is a key component of this jitter generation.

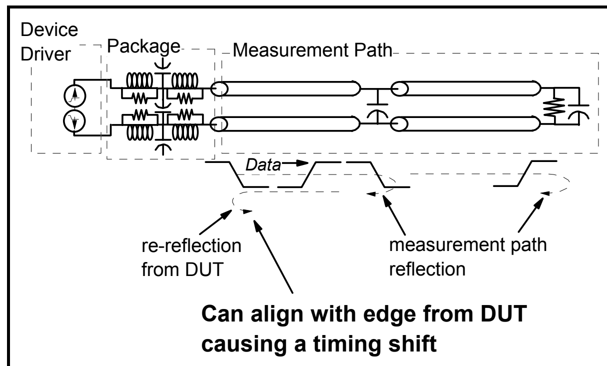

Figure #2a: DUT Interaction (Output Impedance)

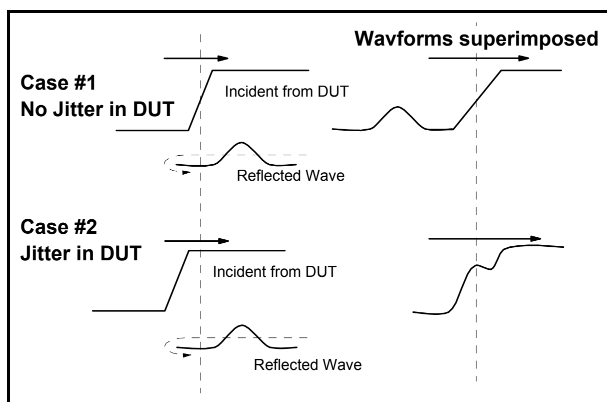

Figure 2b: DUT Interaction (Device Jitter)

The second level of interaction is more subtle. Assume for a moment a jitter-free DUT. That is, every incident edge from the device is fixed relative to the cycle boundary. The incident edge travels down and energy reflects back at a time determined by the electrical length of the path. Thus, the next incident edge may or may not align with the re-reflection of this energy. In a more realistic part, every incident edge moves relative to the cycle boundary. Therefore where this re-reflection may align with subsequent incident edges *changes.* As an example, it is possible for the deterministic jitter of the DUT to interact with the deterministic jitter of the measurement path in such a way that the total measured jitter *is less than* the deterministic jitter of the measurement path stimulated by a jitter-free signal. This property has actually been used as a jitter correction technique[3]. *This violates a basic principle of stationary processes*.

Finally, complicating matters even further is that the output impedance also changes as a function of drive level, and thus the re-reflected energy changes. The internal jitter of the part resulting in the slight movement of an edge could potentially result in very different jitter results if there is a large variation in output (or input) impedance. This is a major issue for single ended, large drive signals in CMOS and TTL but much less of a problem for small swing differential signals.

The simplest method for mitigating the effects of measurement path error is to place matched impedance attenuators at the input or output of the DUT. A high performance 6db matched attenuator, for example, dramatically reduces the effects of a poorly designed measurement path. Attenuators, however, are a very unpopular solution among test engineers for a variety of reasons.

Provided some assumptions can be validated about a particular device technology, the author suggests that a second method for measurement path correction is also possible. These assumptions are:

(1) The causes of jitter in the DUT -- e.g. transistor bandwidth, parasitic reactance, etc. -- cause a contiguously distributed spectrum of jitter performance over several devices. That is, jitter performance tracks process variation in a predictable fashion. For small swing devices

and normal process variations, the author suggests that this is a valid assumption without further discussion.

(2) Analog simulation is possible to determine the dominant causes of deterministic jitter in an I/O device. For an SOC device, for example, the transmitter block must have a solid retiming mechanism, so its jitter performance is mainly dependent of the analog Tx block.

This second method analyzes the measurement path using time domain reflectrometry (TDR) and transmission (TDT) and builds an accurate simulation model for the path. The method then compares the jitter results for a device attached to an ideal measurement path to the same device attached to the real path model. This is done several for devices with different jitter performance. Ultimately some correlation should be found, and thus, a way of predicting the effect of the measurement path degradation can be established.

2.0 Measurement Path Modeling

Several excellent SPICE model Extraction tools on the market are available, and the author strongly recommends the use of such tools. The basic procedure for model extraction from TDR starts by recognizing the pattern of a discontinuity and then iteratively matching a given model to the discontinuity. Figure #3 shows the TDR example of an SMA launching edge mounted to a board. The vendor rates the SMA to 18GHz. The recognized model "pattern" for the SMA connector is that of a segment of transmission line followed by a weak inductive and then a capacitive discontinuity. Thus, the model is shown in Figure #4.

Through a process of iteration, a lumped model can be extracted to reasonably match the TDR.

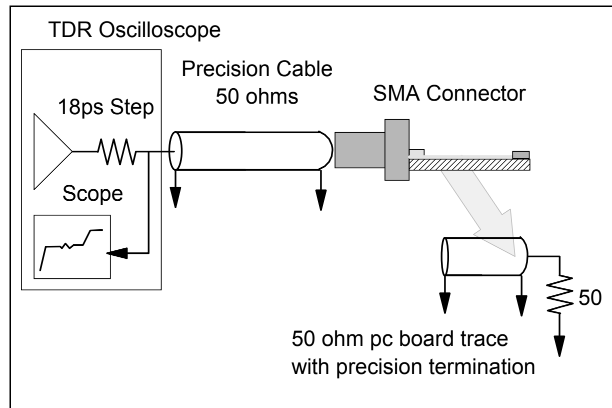

Figure #3a: TDR Setup

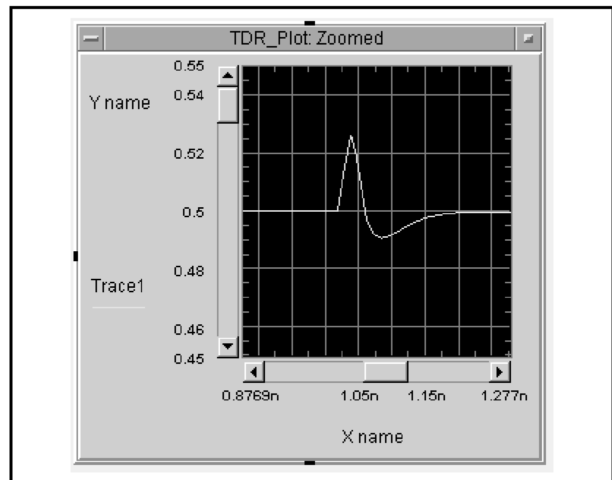

Figure #3b: TDR Plot of SMA Connector

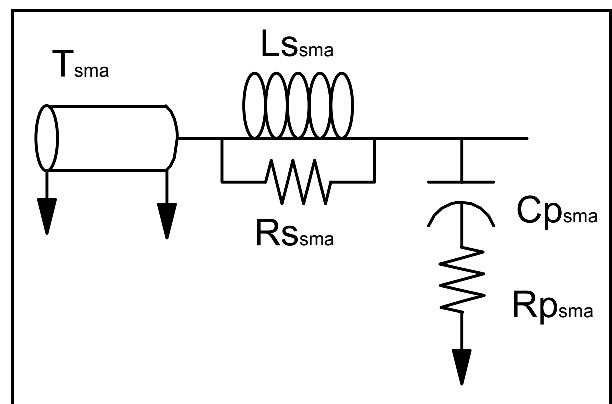

Figure #4: SMA Model

This example uses a Tektronics CSA8000 TDR oscilloscope, and the TDR step is 500mv. Thus the extracted SPICE parameters matching the TDR are:

```
T_sma SMA1 0 SMA2 0 td=25p Z0=50
Ls_sma SMA2 SMA3 .75nh
Rs_sma SMA2 SMA3 40

Cp_sma SMA3 SMA4 .3p
Rp_sma SMA4 0 50
```

(The transmission line distance had to be estimated by knowing the exact distance of the precision cable.)

This process of extracting a model through trial and error iterations can be thus applied to every discontinuity in the measurement path. In the author's experience, the ability to isolate each discontinuity improves results. This can lead to a tremendous investment in time, however. While a more automated tool would generate results much faster, it is important verify results to construct a good model.

3.0 Evaluating Deterministic Jitter in SPICE

The tools for evaluating eye diagrams, bit error rates, and transmission line networks are somewhat incompatible with SPICE and the tools for analog semiconductor design. There are four critical issues:

i. SPICE must generate a pseudo-random bit stream equivalent to the test patterns used for a device.

SPICE does not directly support any random bit patterns. Therefore a script must be used to "wire or" together several pulse generators. The combination of pulses and delays -- combined with scaling-- can thus create an appropriate random bit stream. This is shown in Figure #5. The fore-mentioned script converts a random bit stream output (e.g. 2^7 - 1 PRBS) into several SPICE pulse generators -- one for each low to high transition ("Delay" - previous falling edge = length of low; "Pulse Width" = length of high).

```
.
.
v34 a34 0 pulse(0 1 1.280E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r34 a34 comnode 100
v36 a36 0 pulse(0 1 1.360E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r36 a36 comnode 100
v38 a38 0 pulse(0 1 1.440E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r38 a38 comnode 100
v40 a40 0 pulse(0 1 1.520E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r40 a40 comnode 100
v42 a42 0 pulse(0 1 1.600E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r42 a42 comnode 100
v44 a44 0 pulse(0 1 1.680E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r44 a44 comnode 100
v46 a46 0 pulse(0 1 1.760E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r46 a46 comnode 100
v48 a48 0 pulse(0 1 1.840E-008 6.250E-011 6.250E-011 3.375E-010 1.280E-007 )
r48 a48 comnode 100
.
.
```

Figure #5: Pseudo Random Data in SPICE

A critical limitation of SPICE is that it cannot run some large patterns, such as a 2^{23}-1 PRBS pattern. Therefore critical elements within the pattern, like fast toggles followed by long runs, must be segmented and run individually. Thus, simulation results may tend to underestimate the actual jitter generation within the measurement path and the part -- as a function of the judgment of the simulation engineer.

ii. The output of SPICE, which is aperiodic, must be converted into a periodic format.

Post-processing tools depend on the needs of the user. The post-processing tools used by the author provide an eye diagram, deterministic jitter distribution, and peak-to-peak jitter values.

iii. Tradeoffs must be made between run-time, computer memory, convergence, and the accuracy of the model.

For modeling, very short transmission line pieces tend to dramatically increase run-time or result in non-converging results. A less accurate lumped model (LC, LC, LC,...) dramatically improves run-time. The second concern for modeling is the use of a lossy line. If at all possible, this should be avoided to assist in convergence. (On large boards and systems, it can't be avoided.)

The biggest tradeoff is timing resolution. SPICE allows the specification of both the minimum step

size and the maximum step size. For good results, *both* of these must be set *as small as possible*. The maximum step size directly contributes to simulation error. However, it also can result in memory overflows. (A output typical file will be over 200MB.) Figure #6a and 6b show the jitter results for a near perfect device. In (a) the maximum step size was large, and the simulation ran quickly. In (b) it was very small, and the simulation took more than 100 times longer to run than in (a).

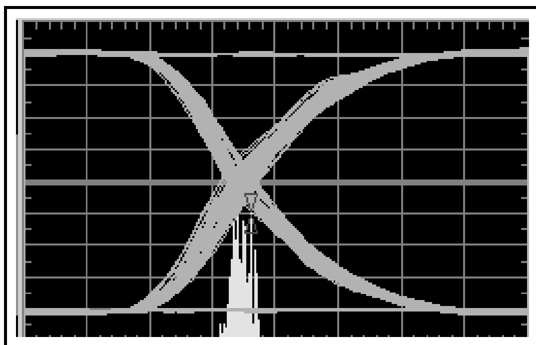

Figure #6(a) Good Part simulated with a large maximum step size (50 ps)

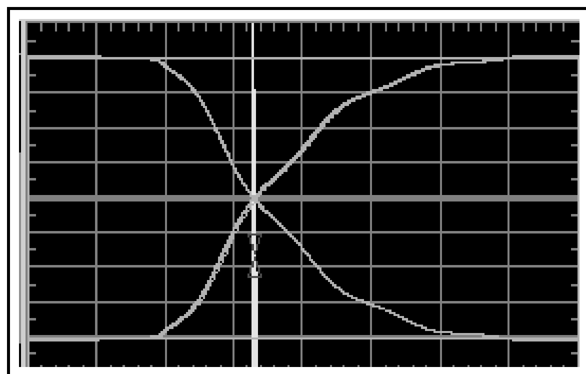

Figure #6(b) Good Part simulated with a small maximum step size (1ps)

iv. The Rise and fall times for measurement path analysis must match the rise and fall times for the device.

Rise and fall time matching is very critical because the actual delay through a discontinuity and amount of energy reflected by the discontinuity depend on both edge rate and edge shape.[4]

In summary, simulation must produce reliable results for both evaluation cases: the device with the measurement path and the device with an ideal path.

4.0 Measurement Path Compensation via Simulation

The experiment to correlate jitter into an ideal path with jitter in a measurement system used 13 data points. Each data point represented a device of a different performance level from slow to fast devices. Each device drove the two signal paths -- an ideal measurement path and the measurement path (test path). In this case the test path had a moderate discontinuity (roughly equivalent to a high performance FET differential probe).

Figure #7a shows a very fast part with very low jitter in the ideal path; 7b show the same part in the test path. Likewise Figure #8a and b show the slowest part in the ideal and test paths respectively.

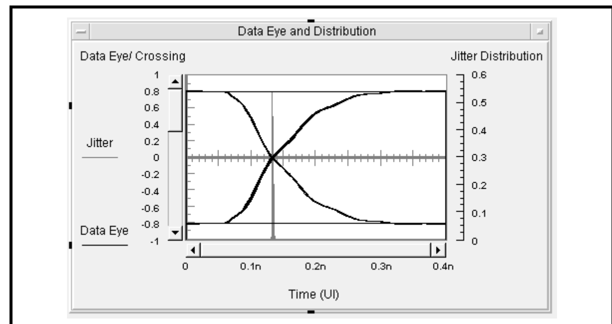

Figure #7a: Best Part, Ideal Path

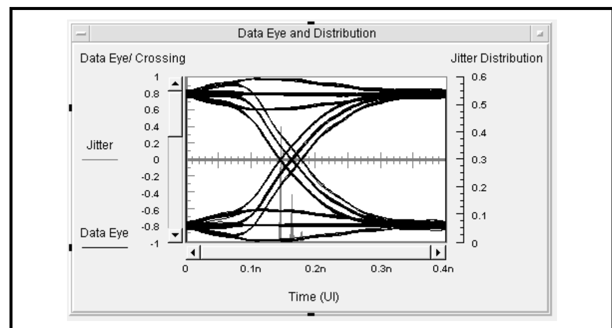

Figure #7b: Best Part, Test Path

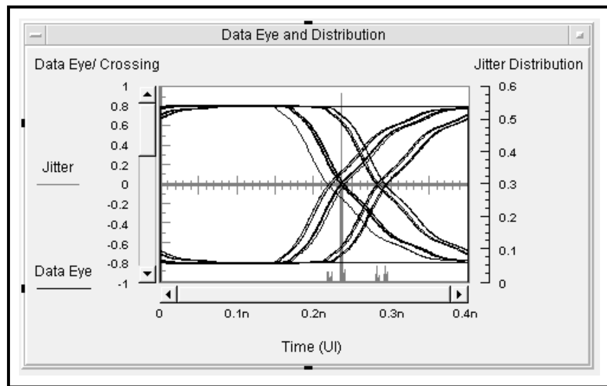

Figure #8a: Worst Part, Ideal Path

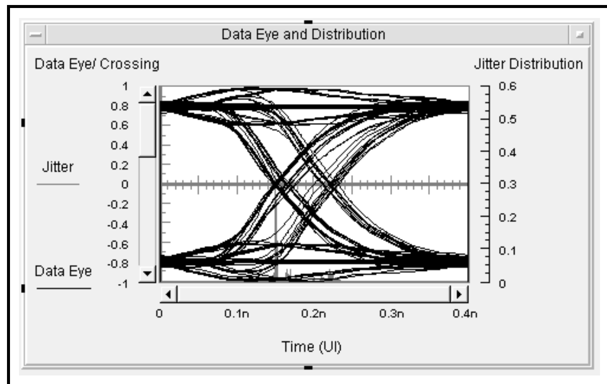

Figure #8b: Worst Part, Test Path

A 2^7-1 PRBS pattern was combined with a series of long runs with a single bit (LL....LHL......LL, HH.....HLH.....HH) and long runs followed by a toggling pattern. The long run patterns are classical stress jitter patterns for IC test, where as the PRBS pattern results in a jitter spread in the measurement path.

Figure #9 shows the results of both the ideal path and the test path for the 13 different test cases. (The x-axis plots the relative speed of the device transistors.) The jitter for the ideal path and the test path tracks, except when the device jitter is very small. Therefore, a correlation is possible, and the very fast devices can be dropped from the correlation calculation (Adj. correlation). This is acceptable because the main concern would be devices performing at or near the specification (e.g. .07-.15UI) versus high performing devices.

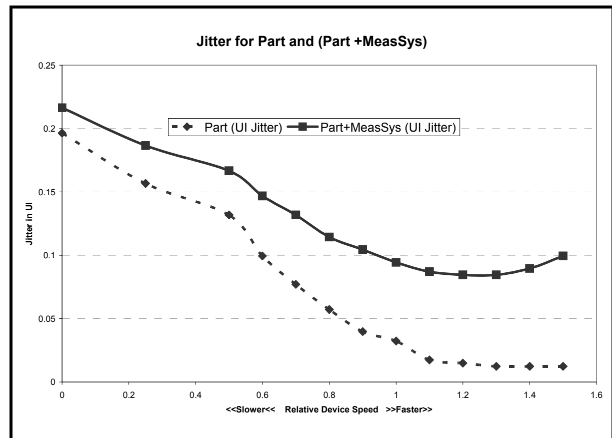

Figure #9
Tracking of Jitter with Device Performance

Linear regression between the two data points results in a very good fit, as shown in Figure #10. The data is as follows:

Correlation Coefficient: .9942
Adj. Corr. Coefficient[5]: .9993
Ip=M(Tp) + B Tracking:
M = 1.385
B = -0.2826
(where Tp =Test Path, Ip = Ideal Path jitter)

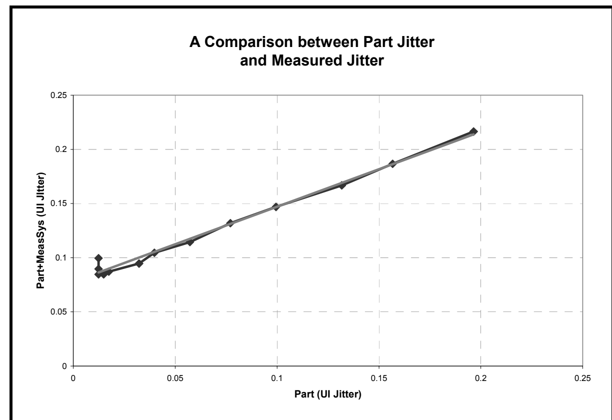

Figure #10, Correlation

The author believes that the poor correlation in the very high performance region is due to simulation error relating to the maximum step size used. This, however, cannot be verified, as the simulator will not converge with smaller step sizes.

The proposed method for compensating for jitter comprises of the following steps:

1. Analyze the measurement path using TDR and TDT techniques. Create a simulation model from the TDR/TDT data.

2. Create a representative SPICE model for the device output. It must include all major sources of jitter -- *especially* I/O impedance.

3. Determine the necessary pattern and create a pseudo-random waveform using SPICE pulse generators that are appropriately sequenced. Care must be taken in creating the pattern. 2^9-1 PRBS patterns are the largest practical patterns -- generating 200MB-500MB files. However, important features of larger patterns (e.g. long runs) may be integrated or pieced.

4. Using Monte-Carlo Analysis or a like tool, determine 4-5 representative speeds for devices from Step 2.

5. Run the jitter simulation for an ideal measurement path and for the path extracted from the TDR/TDT analysis for each of the devices in Step #4.

6. Correlate the two results and determine a least-squares approximation in a Y=MX+B format.

The work done here in simulation can also be done using test equipment. For example, several devices may be tested with precision equipment in a bench setup environment and then tested on ATE with a degraded measurement path. Correlation can thus be established. The pitfall of this approach is that the bench setup environment can also be -- and frequently is -- degraded. The benefit is that an actual 2^{23}-1 PRBS pattern can be used for analysis.

5.0 Use of Attenuation

The part itself is often the single biggest reflection point in the measurement path. Its reflection coefficient falls into three categories:

(1) Current sources (very high impedance)
(2) Follower circuits (low impedance)
(3) Matched impedance. (Usually +/-20%)

In consumer applications, all three have an additional cause for mismatch -- ESD protection.

The attenuator approach provides matching between the device and the measurement path. Because it attenuates the signal, a test engineer must make the tradeoff between "isolation" and signal level passing into the test system. The higher the isolation (and thus, attenuation), the better the impedance match quality and the less effect the measurement path has.

The basic attenuator for differential signals is an "H" attenuator. It is shown below in Figure #11:

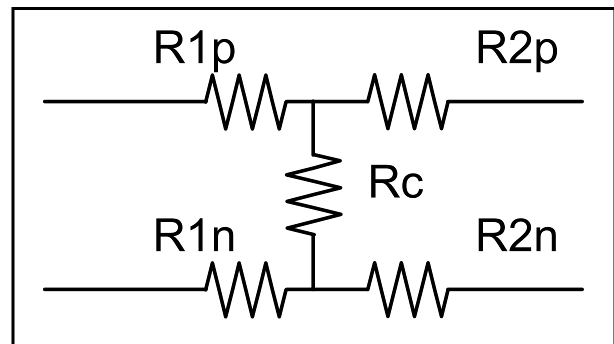

Figure #11: H Attenuator

Generally, R1p=R1n and R2p=R2n. However, R1 is only equal to R2 when the H attenuator is used on an impedance matched device. For 6db attenuation in a 50/100 ohm system, the following are the parameters for R1, R2, and Rc: (R1 is the device side.)

High Impedance Current Output:
R1 = 25, Rc = 100, R2 = 0
Matched Device:
R1 = 16.67, Rc = 133.33, R2 = 16.67
Low Impedance Device (e.g. 8 ohm ECL):
R1 = 50-8 +19.9 = 61.9
Rc= 106, R2=19.9

The author rarely uses attenuation greater than 6db. This allows a reasonable signal to reach the measurement equipment.

The promise of attenuator can be shown by comparing the jitter plots show in Figure #7 to those

shown in Figure #12. The difference in total jitter between the near perfect part in Figure 7a and Figure 12 is .012UI (5 ps @ 2.5Gb) -- roughly five times better than the measurement without the attenuator (Figure 7b). By today's standards of measurement quality, it is "good enough".

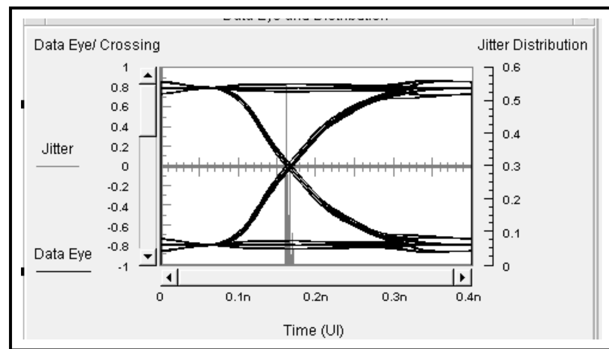

Figure #12: Improved Performance Via An Attenuator (Same Path as Figure 7b)

Attenuators present a handful of implementation problems, which make them unpopular. First, they require use of 0201 components -- needed fit within the desired proximity to the device. 0201 components require special build techniques. Second, care must be implemented in board layout to minimize parasitic reactance. (The plot in Figure 12 includes measured parasitic reactance of an H attenuator.) Third, the components compromise the ability to measure leakage on differential pins. Fourth, high density differential devices present spacing challenges, and the attenuators are not practical. Finally, manufacturing test personnel has a natural reluctance to placing additional components on a device interface board. At a very low cost and minimal engineering effort, however, attenuators make a dramatic improvement, especially for characterization.

6.0 Summary

This paper discussed the issue of correcting for the measurement path in jitter measurements. Correction is difficult because the measurement path interacts with the device in three ways. First, the device output (input) impedance dramatically affects the jitter in the measurement system. Second, the deterministic jitter of the device and the reflection jitter in the measurement path interleave, thus creating a more difficult-to-predict correction. Finally the device output impedance changes, depending on drive level. (A "high" has a different output impedance than a "low".)

Two viable methods exist to compensate for measurement jitter. The first is to use an attenuator. This is, by far, the simplest, but it comes at a cost repugnant to most manufacturing testfloors. The second builds a model of the measurement system and the device. It then predicts jitter performance in both an ideal case and the real case. The end result of the simulation is a least squares approximated correction factor. While this second method is a tremendous amount of work, it has the benefit of being applicable to very high density devices and requires no interface board hardware. As device speeds continue to increase and test capabilities continue to lag behind, this may become the only viable choice for characterization and test of jitter.

7.0 Footnotes

1. Warwick, T. , 2002, p.557.
2. ibid., p558.
3. Warwick, T., 1998, p6-30
4. ibid., p1-3 through 1-10
5. Nonlinear points (near-ideal device) were dropped.

8.0 References

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