

Test Vector Generation Based on Correlation Model for Ratio-Iddq

Xiaoyun Sun*, Larry Kinney and Bapiraju Vinnakota

Department of Electrical and Computer Engineering
University of Minnesota, Minneapolis, MN, 55455

* Tel. No: 612-625-5006, Fax. No: 612-625-4583, e-mail: xsun@ece.umn.edu

Abstract

For ratio-Iddq testing, the test performance is significantly affected by the correlation between two currents of different input patterns as process parameters vary. In this paper we first study the reason for strong correlation between Iddq currents for different test vectors, then build a model to estimate the correlation. Based on this model, we propose three test vector selection methods to improve the fault detection ability of ratio-Iddq testing by selecting test vector pairs with the highest correlation. Hspice simulation showed that the fault detection ability can be improved by as much as an order of magnitude. We also describe a test vector partitioning technique to increase the correlation between Iddq currents of different test vectors.

1. Introduction

Iddq testing has been a very effective test method because it can offer high fault coverage with a small set of test vectors, and can detect defects that escape logic tests [1] - [4]. Traditional Iddq testing detects faults by comparing measured Iddq values against a single pass/fail threshold. As the CMOS technology advances, high leakage current becomes a serious problem to traditional Iddq testing because normal leakage current variation may exceed the leakage current induced by a defect, which makes the defect undetectable. Several advanced Iddq testing methods have been proposed in recent years to address this problem [5] - [11]. Gattiker and Maly [5] used current signatures to detect defects. Thibeault's approach [6] uses the difference in Iddq measurements from two vectors for detecting defects. A multiple-parameter test solution is described in [8] which uses parameters such as maxi-

mum operating frequency and temperature to improve the defect detection sensitivity. An effective variance reduction technique called Nearest Neighbor Residual (NNR) [9] [10] uses the parametric data from neighboring die locations for predicting test outcomes of a die. Maxwell et. al. [11] described a method that sets the dynamic thresholds based on the ratio of maximum Iddq to Minimum Iddq. This method is also known as *ratio* Iddq. A generalized *ratio* Iddq test may use the ratio of any two Iddq currents of different test vectors. Sabade and Walker showed that wafer-level spatial correlation is useful in screening defective chips [12], and proposed a metric called Neighbor Current Ratio (NCR), which is the ratio of leakage current of a chip to the leakage current of a neighboring chip for the same vector [13].

2. Motivation

For a large-size circuit, usually there is a strong correlation between the currents of two test vectors. Fig. 1 shows I_{ddq2} vs. I_{ddq1} for about 300 good devices, where I_{ddq1} and I_{ddq2} are two Iddq currents of different input test vectors. The circuit is a real IC fabricated with $0.25\mu\text{m}$ technology. The regression equation and the correlation coefficient R are also shown in Fig. 1. The correlation coefficient may vary with the test vectors. Fig. 2 shows another two currents I_{ddq4} vs. I_{ddq3} for the same circuit. The correlation coefficient R for I_{ddq3} , I_{ddq4} is smaller than the correlation coefficient for I_{ddq1} , I_{ddq2} . For the circuit mentioned above, 8 Iddq test vectors have been applied and 28 vector pairs (Iddq1, Iddq2 is a pair) have been formed. For the 28 vector pairs, the maximum, minimum and average correlation coefficient are 0.999987, 0.998129 and 0.999386, respectively.

The strong correlation is the basis for ratio-Iddq testing. The regression equation for I_2 vs. I_1 where I_1 and I_2 are two currents of different test vectors V_1 and V_2

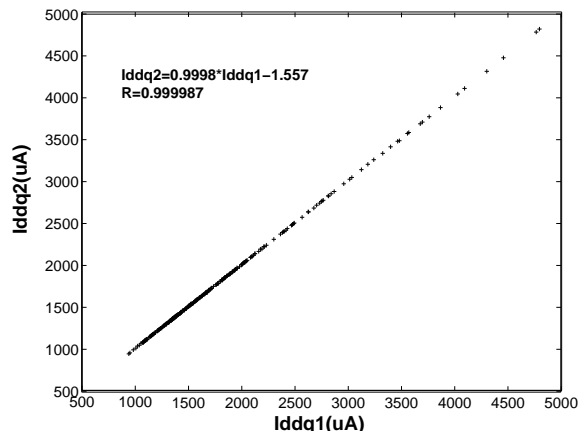


Figure 1. Iddq2 vs. Iddq1

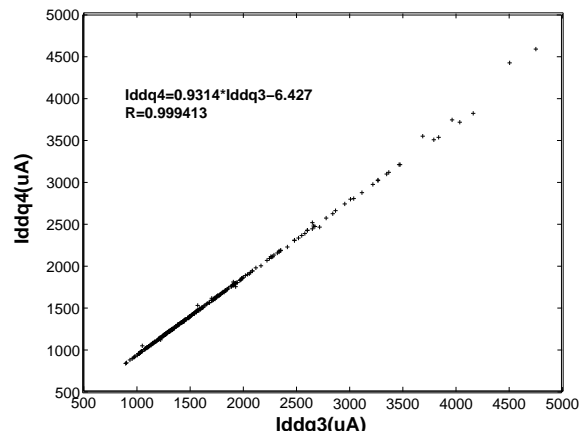


Figure 2. Iddq4 vs. Iddq3

can be written as

$$I_{2e} = b_1 * I_1 + b_0 \quad (1)$$

where I_{2e} is the expected value of I_2 , b_1 is the slope of the regression line and b_0 is the intercept. V_1 and V_2 can be considered as a test vector pair for ratio-Iddq testing. If b_0 is 0, then the metric b_1 is the ratio of two currents. Dynamic thresholds can be set based on the root-mean-square-error \sqrt{MSE} , e.g., a threshold of $4\sqrt{MSE}$ means any device with I_2 outside the range $(I_{2e} - 4\sqrt{MSE}, I_{2e} + 4\sqrt{MSE})$ will be declared as a defect. \sqrt{MSE} can be expressed as

$$\sqrt{MSE} = \sqrt{1 - R^2} \sigma_{I_2} \quad (2)$$

where σ_{I_2} is the standard deviation of I_2 . Fig. 3 and Table 1 show the $4\sqrt{MSE}$ thresholds for different correlation coefficients. Active defects (defects depending on input patterns) that fall between the solid line and the dash line will be detected if $R = 0.999987$, but would escape the test if $R = 0.998129$. The smallest current variation caused by an active defect that is detectable by the thresholds when R is the maximum is $13.7\mu A$, while the smallest current variation detectable by the thresholds when R is the minimum is $161.2\mu A$. They differ by an order of magnitude. So the performance of ratio-Iddq testing strongly depends on the correlation between the two currents. The stronger the correlation, the tighter the threshold, and the better the fault detection ability.

Based on above observation, we may improve the fault detection ability of ratio-Iddq testing by first esti-

Line Type	R	Threshold(uA)
Solid Line	0.999987(Max)	13.7
Dot Line	0.999386(Avg)	92.4
Dash Line	0.998129(Min)	161.2

Table 1. \sqrt{MSE} and the 4σ threshold at different R values

imating the correlation between currents generated from two input vectors, then selecting test vector pairs with the strongest correlation. Since hspice simulation is impossible for large-size circuits, a practical and accurate method to estimate the correlation coefficient R is needed. The rest of the paper is organized as follows: a model to estimate the correlation is proposed in Section 3, based on this model, we propose three test vector selection methods and a test vector partitioning technique in Section 4.

3. Correlation Model

To explain the strong correlation between Iddq currents for different input vectors, we first study the Iddq current of a single logic gate with different input patterns. We will refer to a specific combination of gate type and input pattern as a configuration. For each configuration, 27 Iddq currents were determined by performing hspice simulation over 27 process runs of the TSMC $0.18\mu m$ technology for which data were available at the MOSIS web site [14]. The dimensions of NMOS and PMOS transistors are obtained from the standard

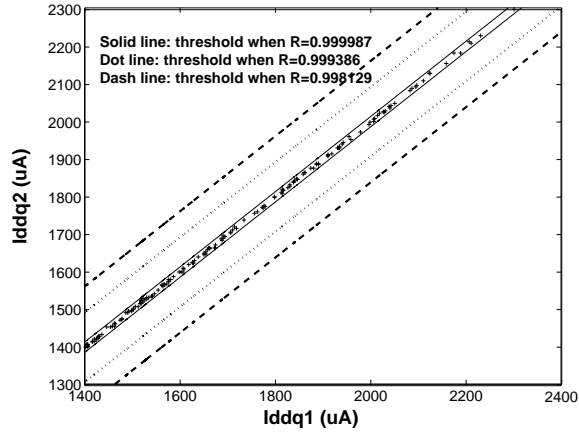


Figure 3. Comparison of 4σ Thresholds with different R

cell library provided by MOSIS [14] and are listed in Table 2. Note that the NMOS/PMOS transistor size does not change for different gate types. The correlation coefficient R between two configurations is calculated based on these I_{ddq} currents. The results for NOT and 2-input NAND gates are listed in Table 3. The notation "Nand00" means the input pattern for the 2-input NAND gate is 00. The correlation coefficient between I_{ddq} currents of configuration Not0 and configuration Not1 is -0.129, which means that there is almost no correlation between the two configurations. However, there is a strong correlation between configuration Not0, Nand00, and Nand10, and a strong correlation exists between configuration Not1 and Nand11.

Gate	$L(\lambda)$	$W_n(\lambda)$	$W_p(\lambda)$
Not	2	6	10
2-in Nand	2	6	10
2-in Nor	2	6	10
3-in Nand	2	6	10
3-in Nor	2	6	10
4-in Nand	2	6	10
4-in Nor	2	6	10

$\lambda = 0.1\mu m$ for $0.18\mu m$ technology

Table 2. Dimensions of NMOS and PMOS transistors from MOSIS standard cell library

Fig. 4 shows the leakage current of a NOT gate for two different input situations. When the input of the

Gate Type	Not 0	Not 1	Nand 00	Nand 10	Nand 11
Not0	1	-0.129	0.918	1	-0.129
Not1	-0.129	1	-0.114	-0.093	1
Nand00	0.918	-0.114	1	0.923	-0.114
Nand10	1	-0.093	0.923	1	-0.093
Nand11	-0.129	1	-0.114	-0.093	1

Table 3. Correlation between I_{ddq} currents for different configurations

NOT gate is '0', the leakage current flows through the NMOS transistor. We denote the leakage current as I_n since it is determined by process parameters related to NMOS. When the input of the NOT gate is '1', the leakage current flows through the PMOS transistor. We denote the leakage current as I_p since it is determined by process parameters related to PMOS. Fig. 5 shows the leakage current of a 2-input NAND gate. When the input of the Nand gate is "10", one NMOS transistor is "on" and one is "off". The leakage current is I_n . When the input of the Nand gate is "00", there are 2 cascaded NMOS transistors in the off-state. Since the resistance of the 2 cascaded off-state NMOS transistors is twice of the resistance for a single off-state NMOS transistor, the leakage current through the 2 cascaded NMOS transistors is $0.5I_n$. When the input of the Nand gate is "11", the leakage current flows through both the PMOS transistors, so the total leakage current is $2I_p$.

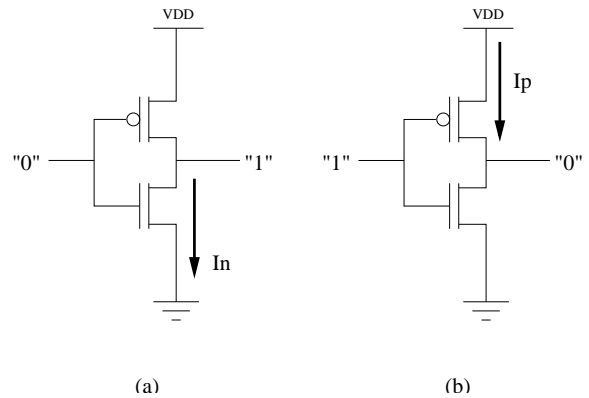


Figure 4. Leakage current for Not gate for different inputs

So we can express the I_{ddq} current as the sum of the

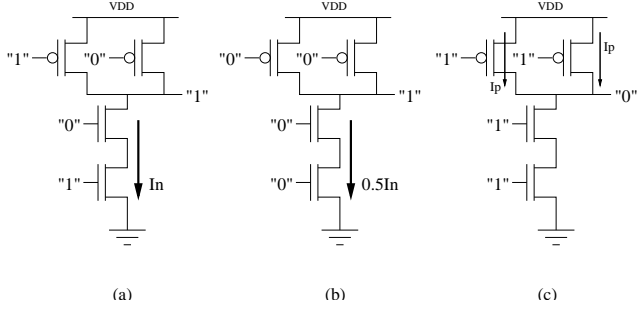


Figure 5. Leakage current for Nand gate for different inputs

leakage current due to NMOS transistors (I_{ddqn}) and the leakage current due to PMOS transistors (I_{ddqp}). We get

$$I_{ddq} = I_{ddqn} + I_{ddqp} = a_n I_n + a_p I_p \quad (3)$$

a_n/a_p is the effective number of NMOS/PMOS transistors that are in “off” state and with leakage current flowing through them. I_n , I_p are determined by process parameters and a_n , a_p are independent of process parameters. a_n and a_p for different configurations are shown in Table 4.

Gate Type	Input Type	a_n	a_p
Not	0	1	0
Not	1	0	1
2-in Nand	00	0.5	0
2-in Nand	10	1	0
2-in Nand	11	0	2
3-in Nand	000	0.33	0
3-in Nand	100	0.5	0
3-in Nand	110	1	0
3-in Nand	111	0	3
4-in Nand	0000	0.25	0
4-in Nand	1000	0.33	0
4-in Nand	1100	0.5	0
4-in Nand	1110	1	0
4-in Nand	1111	0	4

Table 4. a_n , a_p for different configurations

If two Iddq currents I_{ddq1} and I_{ddq2} for test vector pair (V_1 , V_2) can be expressed as

$$\begin{aligned} I_{ddq1} &= a_{1n} I_n + a_{1p} I_p \\ I_{ddq2} &= a_{2n} I_n + a_{2p} I_p \end{aligned} \quad (4)$$

then the correlation coefficient $R_{I_{ddq1}, I_{ddq2}}$ is 1 when

$$\frac{a_{1n}}{a_{1p}} = \frac{a_{2n}}{a_{2p}} \quad (5)$$

So the strong correlation between Iddq currents for different input vectors may be due to the fact that for any two Iddq currents, there exists a relation

$$\frac{a_{1n}}{a_{1p}} \sim \frac{a_{2n}}{a_{2p}} \quad (6)$$

We define the percentage of NMOS transistors in the off-state p_n to be $\frac{a_n}{a_n + a_p}$. So for the two Iddq currents I_{ddq1} and I_{ddq2} of test vector pair (V_1 , V_2), we have

$$\begin{aligned} p_{1n} &= \frac{a_{1n}}{a_{1n} + a_{1p}} \\ p_{2n} &= \frac{a_{2n}}{a_{2n} + a_{2p}} \end{aligned} \quad (7)$$

The condition $\frac{a_{1n}}{a_{1p}} \sim \frac{a_{2n}}{a_{2p}}$ is converted to

$$p_{1n} \sim p_{2n} \quad (8)$$

To demonstrate this, we calculated the average and standard deviation of p_n of the combinational part of several ISCAS89 benchmark circuits over 400 randomly generated test vectors. The results are listed in Table 5. The standard deviation σ_{p_n} is normalized to the average. The distribution of p_n for benchmark circuit s38417 is shown in Fig. 6. As observed from Table 5, the normalized standard deviation is very small, which means the above relation holds.

The correlation coefficient R can be expressed as

$$\begin{aligned} R_{I_{ddq1}, I_{ddq2}} &= \frac{cov(I_{ddq1}, I_{ddq2})}{\sigma_{I_{ddq1}} \sigma_{I_{ddq2}}} \\ &= \frac{cov(I_{ddq1}', I_{ddq2}')}{\sigma_{I_{ddq1}'} \sigma_{I_{ddq2}'}} \end{aligned} \quad (9)$$

Where $I_{ddq1}' = p_{1n} I_n + (1 - p_{1n}) I_p$ and $I_{ddq2}' = p_{2n} I_n + (1 - p_{2n}) I_p$. Let d_n be the percentage difference of a_{1n} and a_{2n} , then

$$d_n = p_{1n} - p_{2n} \quad (10)$$

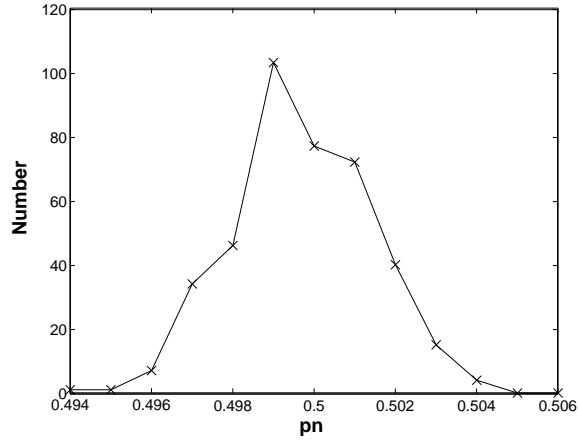


Figure 6. Distribution of pn for s38417

Circuit	# Gates	\bar{p}_n	$\sigma_{p_n}^*$
s444	181	0.506	0.0503
s1196	529	0.488	0.0095
s1238	508	0.486	0.0203
s1423	657	0.508	0.0316
s1488	653	0.495	0.0094
s5378	2779	0.535	0.0061
s15850	9772	0.514	0.0131
s38417	22179	0.500	0.0033
s38584	19253	0.531	0.0314

* Normalized standard deviation

Table 5. Average and standard deviation of p_n for several benchmark circuits

Let

$$K = \frac{\text{cov}(I_{ddq1}', I_{ddq2}')}{\sigma_{I_p} \sigma_{I_n}}$$

$$= p_{1n} p_{2n} \frac{\sigma_{I_n}}{\sigma_{I_p}} + (1 - p_{1n})(1 - p_{2n}) \frac{\sigma_{I_p}}{\sigma_{I_n}} + (p_{1n}(1 - p_{2n}) + p_{2n}(1 - p_{1n})) R_{I_n, I_p} \quad (11)$$

Then we get

$$R_{I_{ddq1} I_{ddq2}} = \frac{K}{\sqrt{K^2 + d_n^2(1 - R_{I_n, I_p}^2)}}$$

$$= \frac{1}{\sqrt{1 + \frac{d_n^2(1 - R_{I_n, I_p}^2)}{K^2}}} \quad (12)$$

It is shown in Table 5 and equation 10 that d_n is small, then

$$R_{I_{ddq1} I_{ddq2}} \sim 1 - \frac{d_n^2(1 - R_{I_n, I_p}^2)}{2K^2} \quad (13)$$

Table 5 shows that $p_{1n} \sim p_{2n} \sim 0.5$ and Table 3 shows that $R_{I_n, I_p} \sim 0$, so

$$R_{I_{ddq1} I_{ddq2}} \sim 1 - 2d_n^2 \quad (14)$$

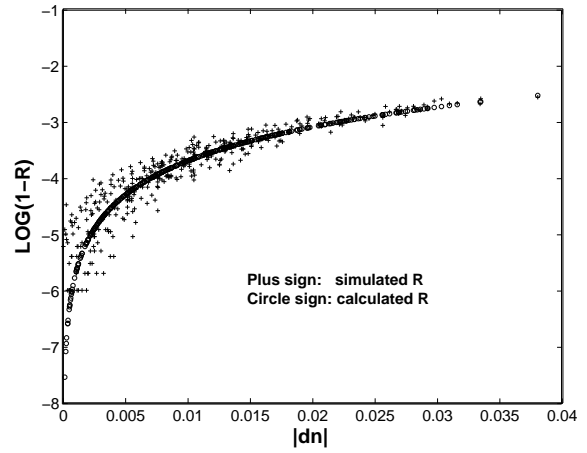


Figure 7. Comparison of calculated and simulated R for different d_n (MOSIS library, benchmark s1238)

To validate the above model, we perform hspice simulation on the combinational part of benchmark circuit s1238 over 400 randomly generated test vector pairs. Every test vector pair consists of two test vectors, and 27 Iddq currents are obtained over 27 process runs of TSMC 0.18 μ m technology [14] for each test vector. The correlation coefficient R for a test vector pair is calculated based on these currents. Two sets of standard cell libraries have been tried. One is the library provided by MOSIS where the transistors for different gate types have the same size (Table 2), the other is a self-constructed library where the transistors for different gate types have different sizes (Table 6). Fig. 7 (MOSIS library) and Fig. 8 (self-constructed library) compare the calculated result (equation 14) and simulated result of R for different d_n . For both standard cell libraries,

the calculated R and the simulated R match well when d_n is greater than 0.01. When d_n is below 0.01, there is a small variation for simulated R, and the variation grows as d_n decreases. This is because when d_n is small, the error generated from the estimation of a_n and a_p can not be ignored.

Gate	$L(\lambda)$	$W_n(\lambda)$	$W_p(\lambda)$
Not	2	6	10
2-in Nand	2	12	10
2-in Nor	2	6	20
3-in Nand	2	18	10
3-in Nor	2	6	30
4-in Nand	2	24	10
4-in Nor	2	6	40

$\lambda = 0.1\mu m$ for $0.18\mu m$ technology

Table 6. Dimensions of NMOS and PMOS transistors from self-constructed standard cell library

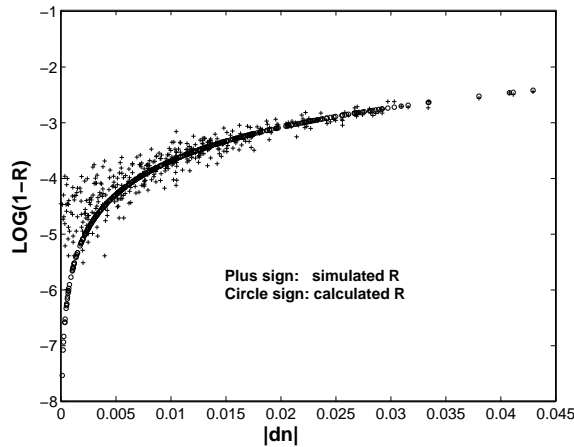


Figure 8. Comparison of calculated and simulated R for different d_n (self-constructed library, benchmark s1238)

Fig. 9 shows the calculated result (equation 14) and simulated result of R for different d_n for benchmark circuit s5378. The hspice simulations were performed over 200 randomly generated test vector pairs. The benchmark circuit s5378 is about 4 times larger than s1238. Fig. 9 shows that there is no significant degradation for the correlation model due to scaling.

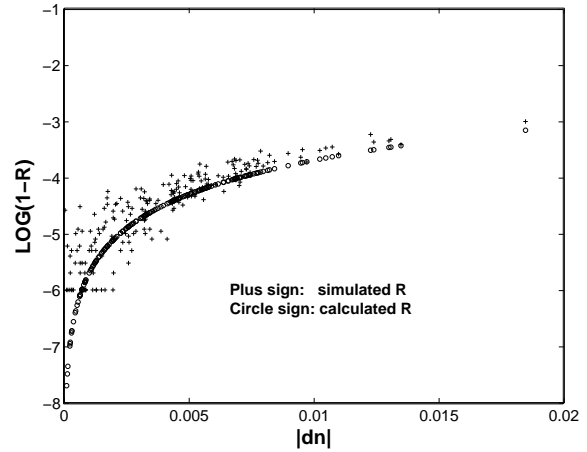


Figure 9. Comparison of calculated and simulated R for different d_n (MOSIS library, benchmark s5378)

The effectiveness of the correlation model is affected by several factors. First, the model is simple and not accurate enough for small d_n , so there will be a large error for the model for circuits with small σ_{p_n} . Second, the model to estimate a_n, a_p (Table 4) works well for TSMC $0.18\mu m$ technology, but may be inaccurate for some other technologies. Third, the intra-die variation may degrade the performance of the model. Fourth, for some technologies, there is no strong correlation between two Iddq currents of different test vectors. The correlation model may not work in such a case.

To solve some of the above problems, we are in the process of developing a more accurate model to estimate a_n, a_p .

4. Application to Test Vector Generation

4.1. Test Vector Selection

Based on the relationship between correlation and performance, and the model for estimating correlation described in the last section, we can improve the fault detection ability of ratio-Iddq testing by selecting test vector pairs whose currents have a high correlation. We describe three approaches for vector selection below.

4.1.1. First approach

The first approach selects vectors according to their p_n values. The p_n values for test vector candidates are

estimated based on the model described in the last section. Only those vectors with estimated p_n value in the range $(\overline{p_n} - \delta_{p_n}, \overline{p_n} + \delta_{p_n})$ are selected, where $\overline{p_n}$ is the estimated average value of p_n over all test vectors and δ_{p_n} is a predefined threshold. As a result, d_n for any two selected vectors should not be larger than $2\delta_{p_n}$ and the correlation coefficient R for the two Iddq currents generated by the two selected vectors should not be lower than $1 - 4\delta_{p_n}^2$.

δ_{p_n}	Simu. Min R	Simu. Avg. R	Normal. Threshold
No	0.995993	0.999591	1
0.01	0.999402	0.999868	0.566
0.005	0.999704	0.99996	0.311
0.002	0.999912	0.999987	0.178
0.001	0.999946	0.999993	0.129
0.0005	0.999986	0.999997	0.084

Table 7. Simulated R and normalized threshold for different δ_{p_n}

The hspice simulation was performed on the combinational component of the ISCAS89 benchmark s1238. For a given δ_{p_n} , 20 vectors were selected from a large number of randomly generated test vectors. For every selected vector, 27 Iddq currents were obtained from hspice simulation over 27 process runs of the TSMC $0.18\mu m$ technology for which data were available at the MOSIS web site [14]. 190 test vector pairs were formed by the 20 selected vectors and correlation coefficient R for each vector pair was calculated based on these currents obtained from hspice simulation. Table 7 shows the minimum and average R and the normalized threshold for different δ_{p_n} . The first row of the Table shows the simulation results for 400 randomly generated test vector pairs without applying the selection method. The threshold value for different δ_{p_n} is calculated from equation 2 where R is the average value listed in the third column of Table 7, and is normalized to the threshold when the selection method is not applied. Table 7 shows that the threshold can be set 10 times tighter, and the smallest current variation caused by an active defect that is detectable is reduced by 10 times when selection criterion is $\delta_{p_n} = 0.0005$. As a result, the fault detection ability is improved by an order of magnitude when $\delta_{p_n} = 0.0005$.

Table 8 shows the normalized threshold for several

Circuit	# Gates	σ_{p_n} *	Normal. Thres.
s444	181	0.0503	0.097
s1423	657	0.0316	0.077
s1238	508	0.0203	0.129
s1196	529	0.0095	0.155
s1488	653	0.0094	0.182
s5378	2779	0.0061	0.160

* Normalized standard deviation

Table 8. Normalized threshold for several benchmark circuits when $\delta_{p_n} = 0.001$

benchmark circuits when $\delta_{p_n} = 0.001$. For all the six benchmark circuits, the threshold when $\delta_{p_n} = 0.001$ is about an order of magnitude smaller than that when no selection method is applied.

The first approach can be combined with a common ATPG method and serve as a selection criterion, which means that any test vector generated by the ATPG method should pass the predefined selection criterion.

4.1.2. Second approach

In the second approach, a number of vectors are selected as benchmark vectors. The p_n values of the benchmark vectors are equally spaced between the maximum and minimum p_n values (the maximum and minimum p_n values are defined as $\overline{p_n} + 4\sigma_{p_n}$ and $\overline{p_n} - 4\sigma_{p_n}$). For example, if 7 benchmark vectors are chosen, then their p_n values will be $\overline{p_n} - 3\sigma_{p_n}$, $\overline{p_n} - 2\sigma_{p_n}$, $\overline{p_n} - \sigma_{p_n}$, $\overline{p_n}$, $\overline{p_n} + \sigma_{p_n}$, $\overline{p_n} + 2\sigma_{p_n}$, and $\overline{p_n} + 3\sigma_{p_n}$. So we may form a vector pair using any test vector and a benchmark vector with the p_n value closest to the p_n value of that vector. So the maximum d_n of any vector pair will not exceed half of the distance between two neighboring benchmark vectors. For example, for the case of 7 benchmark vectors, the maximum d_n of any vector pair will not exceed $0.5\sigma_{p_n}$.

The hspice simulation was performed on the combinational component of the ISCAS89 benchmark s1238. The benchmark vectors were chosen from a large number of randomly generated test vectors so that their p_n values were equally spaced between the maximum and minimum p_n values. 100 test vectors were randomly generated. For each test vector V_i of the 100 test vectors, a vector pair was formed using V_i and a selected benchmark vector with the best correlation to V_i . The correlation coefficient R for each vector pair was obtained using the same way as that in Section 4.1.1. Ta-

Number of Benchmark	Simu. Min R	Simu. Avg. R	Normal. Threshold
0	0.995993	0.999591	1
7	0.999923	0.999979	0.227
15	0.999967	0.999992	0.140
31	0.999979	0.999995	0.112
63	0.99999	0.999997	0.084

Table 9. Simulated average and minimum R for different number of benchmark vectors(equal-space approach)

ble 9 shows the hspice simulation result of minimum R, average R and normalized threshold of the 100 vector pairs for different numbers of benchmark vectors. The first row of the Table shows the simulated R for 400 randomly generated test vector pairs without the use of benchmark vectors. Table 9 indicated that compared to the case when no benchmark vector is used, the threshold can be set 10 times tighter, and the performance is improved by an order of magnitude when 63 benchmark vectors are used.

The second approach can also be combined with a common ATPG method and a test vector pair will be formed using any test vector V generated by the ATPG method and a selected benchmark vector with the best correlation to V.

4.1.3. Third approach

Lloyd proposed a method to find an optimal quantizer [15]. This method can also be used to find the benchmark vectors. Assume p_n is distributed in the interval $[l, m]$ with density function $p(p_n)$. The interval $[l, m]$ is partitioned into N parts. Each part corresponds to a benchmark vector. The endpoints of these N parts are $x_0, x_1, x_2, \dots, x_N$, and satisfy

$$x_0 = l < x_1 < x_2 < \dots < x_{N-1} < x_N = m \quad (15)$$

The p_n values for the N benchmark vectors are y_1, y_2, \dots, y_N , and satisfy

$$y_1 < y_2 < \dots < y_N \quad (16)$$

And

$$x_{i-1} < y_i < x_i, i = 1, 2, \dots, N \quad (17)$$

For any test vector with p_n value falling into interval x_{i-1}, x_i , the benchmark vector with $p_n = y_i$ is the closest benchmark vector to this test vector.

The optimal set of benchmark vectors should minimize $\overline{d_n}$. According to [15], the endpoints x_i and the p_n values of the benchmark vectors y_i should satisfy the equations

$$y_i = \frac{\int_{x_{i-1}}^{x_i} xp(x)dx}{\int_{x_{i-1}}^{x_i} p(x)dx} = E[p_n | x_{i-1} \leq p_n \leq x_i] \quad (18)$$

$$x_i = \left(\frac{1}{2}\right)[y_i + y_{i+1}] \quad (19)$$

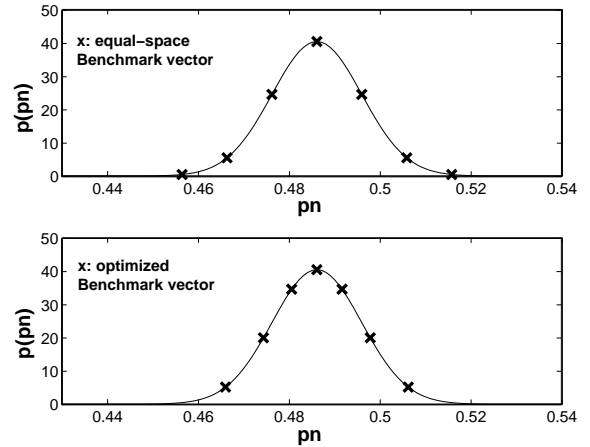


Figure 10. Comparison of the second approach and the third approach(7 benchmark vectors)

Assuming normal distribution for p_n (this assumption may not be correct, but it will not affect the final results), a set of benchmark vectors are selected from a large number of randomly generated vectors based on the above equations. The comparison between benchmark vectors in the second approach(equal-space approach) and benchmark vectors in the third approach(Lloyd-Max approach) is shown in Fig. 10. In the third approach, more benchmark vectors are located near the center(highest probability of p_n). We performed the hspice simulation similar to that described in Section 4.1.2 and the results are listed in Table 10. It is shown from Table 10 and Table 9 that, compared to the second approach(equal-space approach),

the performance is improved by using Lloyd-Max approach to find benchmark vectors.

Number of Benchmark	Simu. Min R	Simu. Avg. R	Normal. Threshold
0	0.995993	0.999591	1
7	0.999883	0.999989	0.164
15	0.999984	0.999995	0.112
31	0.999987	0.999997	0.084
63	0.999993	0.999999	0.047

Table 10. Simulated average and minimum R for different number of benchmark vectors(Lloyd-Max approach)

4.2. Test Vector Partitioning

For Iddq testing of a chip with scan design, the test vector includes the primary inputs and the data in the scan cells. The test vector can be partitioned based on the physical location of the primary inputs and scan cells. For example, Fig. 11 shows a simplified chip with three blocks and a scan chain. We may partition the test vector into 3 groups: (PI2, PI3, S1, S2, S3) for block X, (PI4, PI5, PI6, S4, S5, S6, S7) for block Y, and (PI1, PI7, PI8, S8, S9, S10) for block Z. Test vector pair(V1, V2) is chosen such that V1, V2 only differ in one group. For example, V1, V2 only differ in the input group for block X, and input groups for block Y and Z are same for V1, V2.

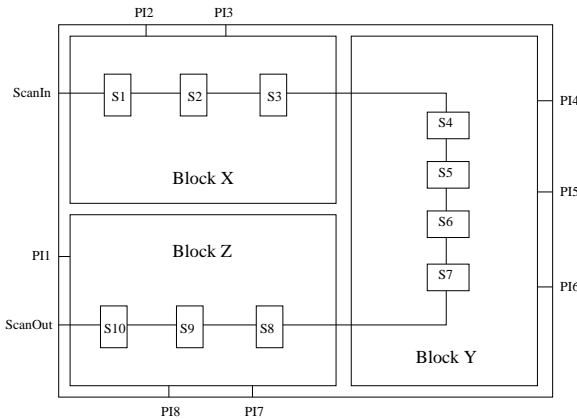


Figure 11. A chip with 3 blocks and a scan chain

If Iddq1, Iddq2 are the Iddq current of the chip in Fig. 11 for test vector V1, V2, they can be written as

$$\begin{aligned}
 Iddq_1 &= (a_{1nx} + a_{1ny} + a_{1nz})I_n + \\
 &\quad (a_{1px} + a_{1py} + a_{1pz})I_p \\
 Iddq_2 &= (a_{2nx} + a_{2ny} + a_{2nz})I_n + \\
 &\quad (a_{2px} + a_{2py} + a_{2pz})I_p
 \end{aligned} \tag{20}$$

Without partitioning the test vectors, the percentage difference d_n can be expressed as

$$\begin{aligned}
 d_n &= \frac{(a_{1nx} + a_{1ny} + a_{1nz}) - (a_{2nx} + a_{2ny} + a_{2nz})}{a_{total}} \\
 &= \frac{(a_{1nx} - a_{2nx})}{a_{total}} + \frac{(a_{1ny} - a_{2ny})}{a_{total}} + \frac{(a_{1nz} - a_{2nz})}{a_{total}}
 \end{aligned} \tag{21}$$

With partitioning the test vectors, since the input groups for block Y and Z are same for V1, V2, then $a_{1ny} \sim a_{2ny}$ and $a_{1nz} \sim a_{2nz}$. So the second and third terms disappear and d_n becomes

$$d_n = \frac{a_{1nx} - a_{2nx}}{a_{total}} \tag{22}$$

We may consider the three terms in equation 21 as independent random variables with normal distribution, so the sum of the three terms d_n is a random variable with standard deviation three times larger than that of d_n in equation 22. The effect of partitioning is shown in Fig. 12, which compares the density function of d_n for the cases with partitioning and without partitioning. The standard deviation of the density function for the case of partitioning decreases by a factor of 3. As a result, \bar{d}_n is reduced by a factor of 3. According to equation 14, correlation between two Iddq currents of test vectors V_1, V_2 increases as d_n decreases, so test vector partitioning improves the performance of ratio-Iddq testing.

5. Conclusion

For ratio-Iddq testing, the test performance is significantly affected by the correlation between two Iddq currents of different test vectors. In this paper we first showed that the strong correlation between Iddq currents for different test vectors is due to stability of the ratio of the number of NMOS/PMOS transistors in the off-state. We then built a practical model to estimate the correlation. Based on this model, three methods have been proposed to improve the fault detection ability of ratio-Iddq testing by selecting test vector pairs

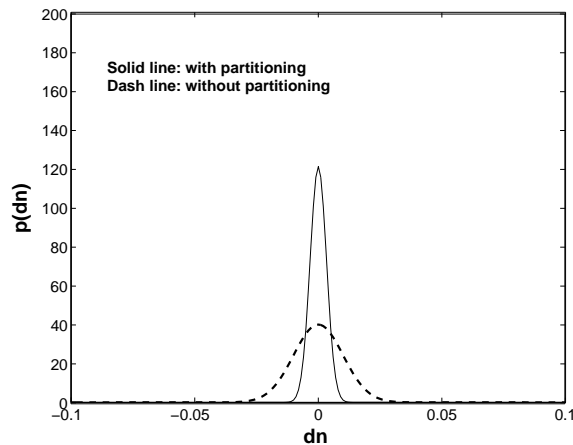


Figure 12. Density function of d_n with partitioning and without partitioning

with the highest correlation. Hspice simulation showed that the fault detection ability can be improved by as much as an order of magnitude. A test vector partitioning technique has also been described which increases the correlation between Iddq currents of different test vectors. We are currently in the process of developing an accurate model to estimate a_n, a_p , and validating the approaches in Section 4.1.2 and 4.1.3 through simulations on more benchmark circuits.

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