HYSTERESIS OF INTRINSIC IDDQ CURRENTS

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ABSTRACT: *Empirical analyses of the I_{DDQ} signatures of 0.18 μm devices indicate that I_{DDQ} currents exhibit hysteresis. A newly proposed test method, SPIRIT (Single Pattern Iteration I_{DDQ} Test), demonstrates that the test pattern and the device clock speed before measurements must be maintained to assure the integrity of I_{DDQ} measurements, which is the fundamental assumption of I_{DDQ} applications: testing, diagnosis, monitoring, and static power estimation. Newly proposed I_{DDQ} signature and hysteresis models show that hysteresis phenomena are caused by the global transient threshold voltage shifts induced by the direct tunnel charges to the pre-existing border traps under nominal operating conditions.*

1. INTRODUCTION

Pass/fail testing, physical diagnosis, and process monitoring based on I_{DDQ} currents have been conducted from the early stages of CMOS manufacturing. However, the large I_{DDQ} amplitude and large I_{DDQ} variance of deep submicron (DSM) devices prevent these applications [1]. To continue I_{DDQ} testing, the test methods based on I_{DDQ} signatures have been proposed [2, 3, 4, 5, 6, 7, 8, 9]. The initial purpose of this study was to determine the best test method for 0.18 μm products. However, as described in this paper, 0.18 μm devices show hysteresis which was not reported in the previous studies.

I_{DDQ} specialists gathered at DBT2002 agreed that I_{DDQ} models which can simulate intrinsic I_{DDQ} signatures are required to advance the research on I_{DDQ} testing [10]. In our review, proposed simulation models [11, 12, 13] are not verified by I_{DDQ} signatures as regards to the large variance simulated by a statistical model [14] or an analytical formal model [15], so these large variance models are not easily described by the signature models. On the other hand, we searched actual I_{DDQ} signatures showing a large variance for common patterns, and observed linear regularity from which several test methods were derived [16]. Analyzing the regularity of the hysteresis will advance I_{DDQ} modeling.

To complete an I_{DDQ} test, I_{DDQ} currents are measured under the different test conditions focusing on the following purposes: 1) to obtain precise signatures to derive test methods, 2) to maintain detailed pass/fail logs to evaluate the derived methods, and 3) to minimize production test costs. To maintain the integrity of the above measurements, the same test pattern, V_{DD}, and temperature should be applied. However, if the other parameters vary the I_{DDQ} currents for the hysteresis, the results will not be predictable.

This paper will first present the background of this study and the device under study, then the hysteresis phenomena will be described. Next, hysteresis mechanism models will be presented based on the newly proposed I_{DDQ} signature models, and finally, an application of the hysteresis and I_{DDQ} estimation errors will be discussed.

2. BACKGROUND

The I_{DDQ} signatures of the Sony 0.25 μm ASIC devices showed regular test vector dependence. The I_{DDQ} signatures of 0.18 μm devices of several designs were measured to confirm the regularity. However, these signatures showed unpredictable behavior, as described in this paper, the amplitude and shape of the I_{DDQ} signatures depend not only on the conditions during the measurements but also on the operation histories from power-on to the measurements. The narrow meaning of "hysteresis" indicates the ferromagnetic characteristics, hysteresis loops or memory effects. On the other hand, "hysteresis phenomenon" means broadly that the response of a system to an external excitation depends not only on the present excitation but also on the previous history of the system. Therefore, we can say the unpredictable behavior is caused by hysteresis phenomena.

Since I_{DDQ} measurements are error-prone tasks [17, 18], several designs showing the hysteresis had been treated as I_{DDQ} un-testable designs for non-quiescent currents. However, the design under study showing the hysteresis is the design used in the previous 0.25 μm studies [7, 16], 180MHz video DSP-ASIC with 1.5 million logic gates. The quiescence of the design on a 0.25 μm process had been proven by the success of considerable I_{DDQ} testing. Design reviews of the 0.18 μm version were carefully applied and passed non-quiescent current checks: leakage from the circuits such as pull-up/pull-down, no-static, and DRAM; bus collision currents caused by invalid test patterns or invalid tester pin assignments; and leakage from test fixtures or measurement units.

The hysteresis mechanisms were derived from six corner wafers intentionally skewed to verify the performance of the design. Therefore, measuring a relative small number of wafers can show the device behavior over broad variance of the process.

3. HYSTERESIS PHENOMENA

Typical hysteresis I_{DDQ} signatures are shown in Fig. 1 (a), I_{DDQ} responses of a device to the test patterns which were generated by a commercial ATPG tool. There are two characteristics, a global fall and up down changes. The global fall is observed to be a rapid fall from the first to the 24th vector and a leisurely fall from the 25th to the last vector. Up down

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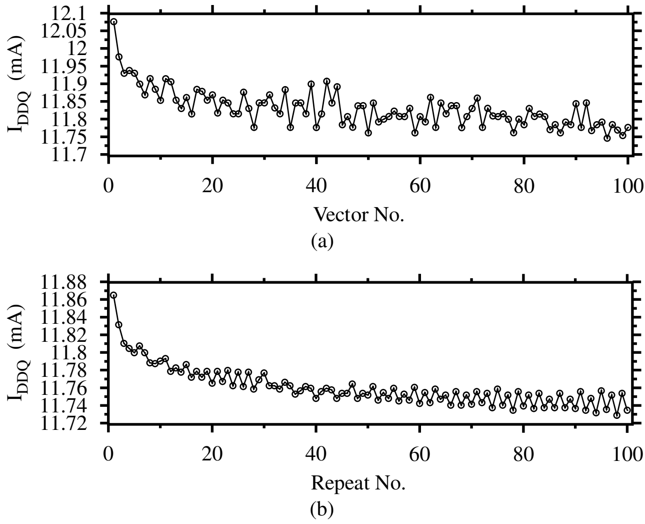

Fig. 1 Typical hysteresis I_{DDQ} signatures: (a) conventional signature; and (b) SPIRIT (Single Pattern Iteration I_{DDQ} Test) signature; (Die-12-7-3).

changes are observed from the 25th vector as having test vector dependence, which is observed in all vectors of 0.25 μm devices which show no global fall.

To separate the global fall from the test vector dependence, the same vector is applied, i.e. "single scan followed by a I_{DDQ} measurement" is repeated, and this is called SPIRIT (Single Pattern Iteration I_{DDQ} Test). In other words, SPIRIT is the conventional I_{DDQ} test that loads the same scan pattern at all vectors. The first test vector of the ATPG pattern set was repeated one hundred times. Figure 1 (b) shows a typical I_{DDQ} signature of SPIRIT, henceforth called SPIRIT signature, where the X-axis is repeat number not vector number. Each I_{DDQ} must be the same, because the node voltages of transistors at all repeats are the same, but measured I_{DDQ} currents are not the same and show a tendency to fall.

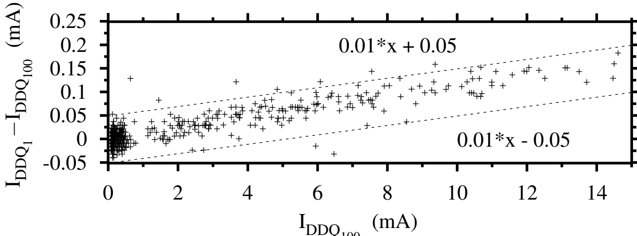

Fig. 2 $I_{DDQ_1} - I_{DDQ_{100}}$ vs. $I_{DDQ_{100}}$ of 420 dies. Hysteresis amplitude is nearly proportional to I_{DDQ} amplitude, 1% of $I_{DDQ_{100}}$.

Figure 2 shows the relationship between the first and the 100th elements of the conventional I_{DDQ} signatures, I_{DDQ_1} $I_{DDQ_{100}}$, of 420 dies which passed a scan test. The dies having an $I_{DDQ_{100}}$ larger than 1 mA show that hysteresis amplitudes, $I_{DDQ_1} - I_{DDQ_{100}}$, are nearly proportional to $I_{DDQ_{100}}$. The hysteresis amplitude is about 1% of $I_{DDQ_{100}}$. This proportionality indicates that the fall characteristics are not random phenomena, but may be caused by parametric defects, systematic defects, or the intrinsic phenomenon of I_{DDQ}.

Seven dies under several conditions were measured many times until repeatable data was obtained, which were applied to multiple analyses. The results of the multiple analyses of the seven dies were applied to the other dies of the corner wafers and production wafers. In this and the next sections, the characteristics of hysteresis will be described on the data measured from Die-12-7-3 under the following conditions: V_{DD} was 1.2 V; the scan-in frequency was 4 MHz; the strobe time (the period from the end of system clock to the start of measurement) was 4 milliseconds; and the temperature was 25 °C.

3.1 Clock Speed Dependence

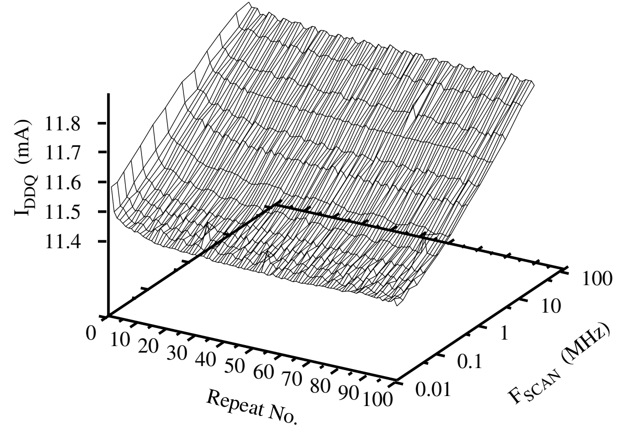

Fig. 3 Functional dependence between SPIRIT signature and scan clock frequency F_{SCAN}.

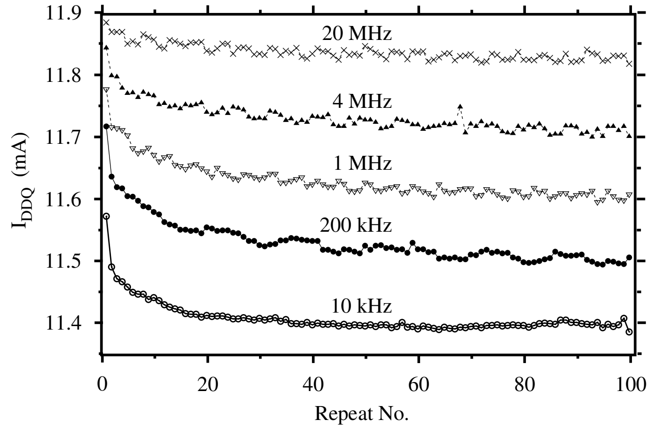

Fig. 4 SPIRIT signatures with scan clock frequency F_{SCAN} as a parameter. This is a two dimensional plot of Fig. 3.

In a production test, an I_{DDQ} test often runs at different operating speeds: at different scan clock speeds and at different strobe times, for ATE limitations or moving from wafer tests to package tests. The degree of hysteresis depends on the scan clock speed and the strobe time. The strobe time dependence of I_{DDQ} will be presented in Section 4.2. The effect of the scan clock speed on the hysteresis will be shown in this sub-section.

Figure 3 and 4 show a typical example, scan clock frequency F_{SCAN} on SPIRIT is parameterized from 20 MHz to 10 kHz with a strobe time of 4 milliseconds. The smooth surface composed by the 13 SPIRIT signatures in Fig. 3 indicates that there is a functional dependency between hysteresis and the scan clock speed. The five SPIRIT signatures in Fig. 4 show the dependency more clearly, the scan clock speed changes not only shapes of SPIRIT signatures but also amplitudes of I_{DDQ}:

1) $I_{DDQ_1} - I_{DDQ_{100}}$ at 10 kHz is 0.175 mA, about 58 times larger than that at 20 MHz; and
2) The $I_{DDQ_{100}}$ at 10 kHz is 11.38 mA, which is 0.44 mA lower than that at 20 MHz.
Before modifying the scan clock speed, the effect of the modification on hysteresis should be estimated. However, carefully select the sample for the estimation, because dies showing low I_{DDQ} indicate weak dependence as shown in Fig. 5.

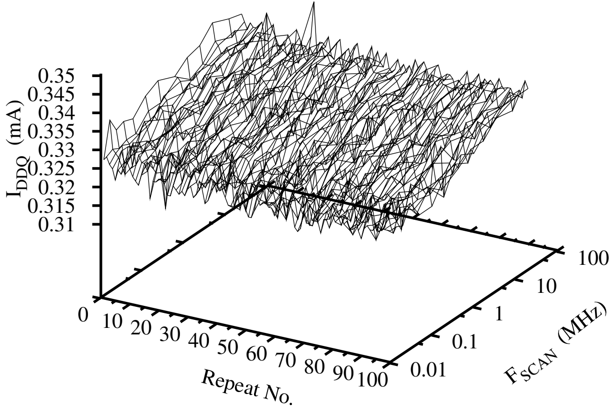

Fig. 5 Weak dependence of SPIRIT signature on scan clock frequency F_{SCAN} (Die-11-9-1).

3.2 Preceding Pattern Dependence

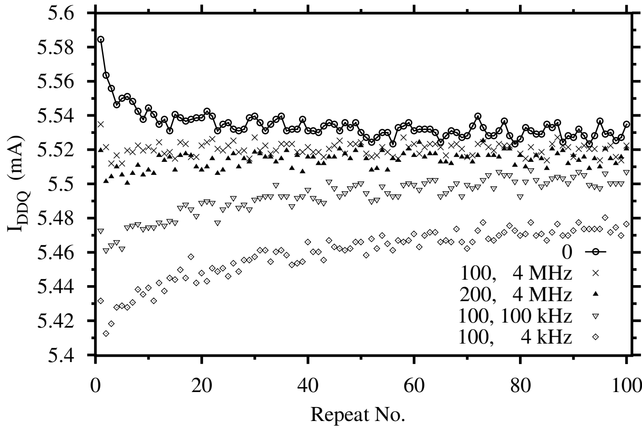

Fig. 6 I_{DDQ} signatures are affected by the preceding scan test. SPIRIT signatures of Die-22-4-4 — "0:" signature with no preceding scan test, and "$\#\ of\, scan\ vectors,\ \ scan\ speed$:" signatures after the scan test with the specified scan vectors at the specified scan speed.

An I_{DDQ} test often runs after the other tests, which can change I_{DDQ} currents. In this sub-section, the effect of scan tests on the following I_{DDQ} test will be shown.

Figure 6 shows the effect of scan tests on the following SPIRIT signature of Die-22-4-4 measured at a scan speed of 4 MHz. Since the effect of scan tests depends on the number of scan vectors and scan speeds of the scan tests, the number of scan vectors is modified to 100 and 200 at a scan speed of 4 MHz and the scan speed is modified to 100 kHz and 4 kHz with fixing the number of scan vectors to 100. The signature marked "0," which was observed immediately after power-on, shows a global fall. The other signatures marked "$\#\ of\, scan\ vectors,\ \ scan\ speed$" were obtained after the scan test with the specified scan vectors at the specified scan speed. The preceding scan tests change the shapes of SPIRIT signatures and lower I_{DDQ} amplitudes. Increasing the number of vectors and lowering scan speed cause larger influence on the following I_{DDQ} tests.

4. HYSTERESIS MECHANISMS

To obtain the hysteresis mechanisms, an I_{DDQ} signature model will be derived from a sub-threshold transistor leakage model, then the actual signatures will be analyzed based on the derived I_{DDQ} signature model.

4.1 I_{DDQ} Models

The dominant leakage component of DSM MOSFETs is sub-threshold leakage [19, 11, 20, 12]. The sub-threshold leakage I_{sub} without short channel effects is modeled in BSIM [21] as

$$I_{sub} = I_{s0} e^{(V_{GS}-V_T)/nv_t}(1 - e^{(-V_{DS}/v_t)}) \quad (1)$$

$$I_{s0} = \frac{W}{L_{eff}} \mu_0 C_{ox} v_t^2 \quad (2)$$

where V_{GS} is gate to source voltage, V_T is the threshold voltage, n is the sub-threshold swing parameter, v_t is the thermal voltage given by $K_B T/q$, since Boltzmann's constant K_B and unit of charge q are physical constants, v_t depends on temperature T. V_{DS} is drain to source voltage. W is the gate width. L_{eff} is the effective gate length. μ_0 is the zero bias mobility. C_{ox} is the gate oxide capacitance. Only v_t depends on temperature, the other parameters are affected by the variations of transistors. However, assuming that all transistors in a die have the same V_T and n, then I_{sub} of each transistor I_{sub_j} is

$$I_{sub_j} = e^{(-V_T/nv_t)} I_{s0_j} e^{(V_{GS_j}/nv_t)}(1 - e^{(-V_{DS_j}/v_t)}) \quad (3)$$

$$I_{s0_j} = \frac{W_j}{L_{eff_j}} \mu_{0_j} C_{ox_j} v_t^2 \quad (4)$$

where j is the transistor number. I_{s0_j}, V_{GS_j} and V_{DS_j} are I_{s0}, V_{GS} and V_{DS} of the transistor j, respectively. Summing I_{sub_j} of all the transistors in off-state yields I_{DDQ} as

$$I_{DDQ} = e^{(-V_T/nv_t)} \sum_{j=1}^{m} O_j I_{s0_j} e^{(V_{GS_j}/nv_t)}(1 - e^{(-V_{DS_j}/v_t)}) \quad (5)$$

where m is the number of the transistors in the die. O_j is the status switch of transistor j: $O_j = 1$ when transistor j is in off-state and $O_j = 0$ in on-state. Since the leakage of a transistor stack is represented by the sub-threshold leakage of one transistor in the stack [13], O of the representing transistor is 1 and Os of the other transistors in the stack are 0. The I_{DDQ} signature of die k at the test vector i is

$$I_{DDQ}(i,k) = e^{(-V_{T_k}/n_k v_t)} I_{DT}(i,k) \quad (6)$$

$$I_{DT}(i,k) = \sum_{j=1}^{m} O_j(i) I_{s0_j} e^{(V_{GS_j}(i)/n_k v_t)}(1 - e^{(-V_{DS_j}(i)/v_t)}) \quad (7)$$

where V_{T_k} and n_k are V_T and n of die k, respectively. $O_j(i)$, $V_{GS_j}(i)$, and $V_{DS_j}(i)$ are O_j, V_{GS_j}, and V_{DS_j} at the test vector i, respectively. The ratio of the I_{DDQ} currents of the die k at the

different test vectors i_1 and i_2, $R_{Vec}(i_1,i_2,k)$, is

$$R_{Vec}(i_1,i_2,k) = \frac{I_{DDQ}(i_2,k)}{I_{DDQ}(i_1,k)} = \frac{I_{DT}(i_2,k)}{I_{DT}(i_1,k)} \quad (8)$$

Assume that all dies show the same $O_j(i)$, I_{s0_j}, $V_{GS_j}(i)$, $V_{DS_j}(i)$, and n, then $R_{Vec}(i_1,i_2,k)$ at the same temperature is independent of the die, depends on i_1 and i_2, i.e. $R_{Vec}(i_1,i_2,k) = R_{Vec}(i_1,i_2)$. Also, the ratio of the elements of the I_{DDQ} signature to the mean I_{DDQ} signature of a die, $\boldsymbol{E_M}$ i.e. $E_{M_i} = I_{DDQ_i}/(\sum_{i=1}^{n} I_{DDQ_i}/n)$ where n is the number of test vectors. The 0.25 μm devices showed that $\boldsymbol{E_M}$ is constant [16].

Figure 7 (a) shows $\boldsymbol{E_M}$ of Die-12-7-3 and Die-7-9-1. Although Die-12-7-3 shows a $I_{DDQ_{100}}$ of 11.7 mA, which is two times higher than that of Die-7-9-1, the $\boldsymbol{E_M}$s are similar. To check the similarity, the difference of the two $\boldsymbol{E_M}$s is shown in Fig. 7 (b). The 85% of E_M elements are in the variance range of ± 0.002, which is $1/5$ of the $\boldsymbol{E_M}$ range of 0.02, therefore, E_M is considered to be constant. The variance of the E_M difference in the hysteresis fall from 1 to 24 vectors and that in the vector dependent change from vector 25 are in the same range. Therefore, hysteresis falls and vector dependent changes are considered to be caused by sub-threshold leakage currents. The $\boldsymbol{E_M}$s of the other dies of the corner wafers will be shown in Section 4.4.

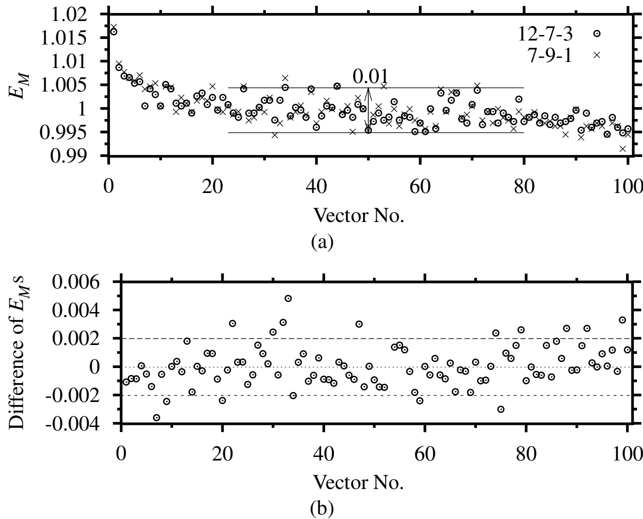

Fig. 7 $\boldsymbol{E_M}$ of Die-12-7-3 and Die-7-9-1: (a) $\boldsymbol{E_M}$ and (b) difference of $\boldsymbol{E_M}$ of Die-12-7-3 to that of Die-7-9-1.

Assume that I_{s0_j} can be written as, $I_{s0_j} = A_j I_{s0u}$, then Eq. (6) is written as

$$I_{DDQ}(i,k) = e^{(-V_{T_k}/nv_t)} I_{s0u} S(i) \quad (9)$$

$$S(i) = \sum_{j=1}^{m} O_j(i) A_j e^{(V_{GS_j}(i)/nv_t)} (1 - e^{(-V_{DS_j}(i)/v_t)}) \quad (10)$$

Equation (9) means that there are two possible mechanisms causing hysteresis, V_T shifts and $S(i)$ shifts. To cause a global fall by the $S(i)$ shifts, Eq. (10) indicates that all transistors vary V_{GS} or V_{DS} by the same amount. Since V_{GS} and V_{DS} depend on the circuit topology and V_{DD}, uniform shifts of V_{GS} and V_{DS} are unnatural. On the other hand, uniform V_T shifts are more reasonable.

Consider the effect of the V_T shift on I_{DDQ} when change of $S(i)$ is negligibly small. From Eq. (8) and (9), $R_{Vec}(i_1,i_2)$ is

$$R_{Vec}(i_1,i_2) = e^{-\Delta V_T(i_1,i_2)/nv_t} \quad (11)$$

$$\Delta V_T(i_1,i_2) = V_T(i_2) - V_T(i_1) \quad (12)$$

where $V_T(i_1)$ and $V_T(i_2)$ are V_T at vector i_1 and i_2, respectively. Since v_t at room temperature is 25 mV, n is 1 to 1.5, and $e^{\alpha} \approx 1+\alpha$ where $-0.04 \le \alpha \le 0.04$, in a $\Delta V_T(i_1,i_2)$ range of ± 1 mV, $R_{Vec}(i_1,i_2)$ is

$$R_{Vec}(i_1,i_2) \approx 1 - \Delta V_T(i_1,i_2)/nv_t \quad (13)$$

The global fall in Fig. 7 (a) is caused by a V_T shift of 0.6 to 0.8 mV, because $R_{Vec}(1,100)$ is $0.978 = 1 - 0.022$. I_{DDQ} currents can detect such a small shift.

4.2 Hysteresis Models

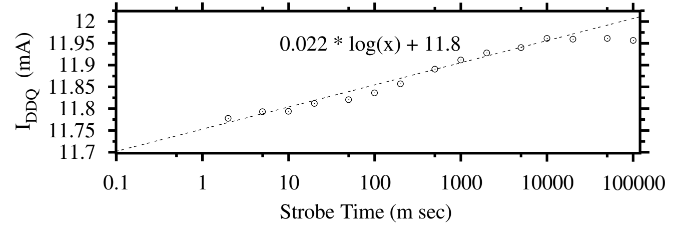

Fig. 8 I_{DDQ} vs. strobe time shows a nearly logarithmic time dependency.

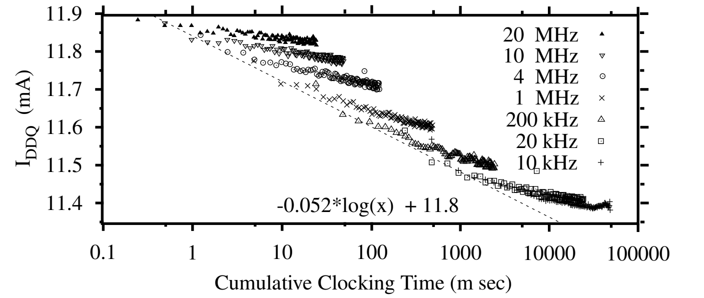

Fig. 9 SPIRIT signature on cumulative clocking time shows an approximately logarithmic time dependency.

Nigh and Gattiker reported "significant I_{DDQ} vs. time variations [22]," or large I_{DDQ} drifts. To confirm their experience on the devices under study, I_{DDQ} versus strobe time was observed. We scanned in a SPIRIT pattern, then measured I_{DDQ} several times from 2 milliseconds to 100 seconds. Figure 8 shows a typical result: I_{DDQ} is rising to 10 seconds and exhibits a nearly logarithmic time dependency.

To analyze I_{DDQ} signatures in a time domain, the SPIRIT signatures in Fig. 4 are re-plotted in Fig. 9 with a logarithmic X-axis of cumulative clocking time, or the total amount of scan-in time before measurements defined as $(Repeat\#) \times (\#of\,ScanClocks) \times (ClockPeriod)$. About half of the plots of each signature show an approximately logarithmic time dependency.

The above two logarithmic time dependencies can be interpreted as caused by the charging and discharging in the gates of transistors, which cause positive or negative V_T shifts. The V_T shifts with logarithmic time dependencies have been published extensively for the studies of device reliability, wearout, and breakdown [23, 24, 25, 26]. In the most of these studies, V_T shifts are caused by applying catastrophic stresses— high voltages, high temperatures, and radiations— not by nominal

operating conditions. Such high stresses can create traps in insulators, which are charged by Fowler-Nordheim tunneling or avalanche injection, which cause V_T instability or permanent shifts.

However, the small V_T shifts of MOS FETs [27, 28] and MOS capacitors [29] under nominal device conditions have been studied to improve the performance of analogue circuit, drifts of AD converter and $1/f$ noises [30]. Without acceleration of the above stresses, intrinsically, MOS devices have traps in insulators: Si/SiO_2 interface traps, border traps, and oxide traps [31]. It is difficult to show the firm distinctions in the three traps, however, interface traps and border traps within 3 nm of Si/SiO_2 interfaces can communicate with the Si in the time scales of microseconds to seconds [32, 33, 34]. Tewksbury and Lee demonstrated that the transient V_T shifts at nominal operation are caused by the direct tunnel exchange of charges between a channel and pre-existing border traps [28]. The shifts were observed as:

1) When N-FETs and P-FETs are operating in a linear or a saturation region for microseconds to tens of milliseconds, V_T increases with the logarithmic stress time dependence; and

2) When bias changes to off-state, increased V_T recovers, or relaxes, with the logarithmic time dependence of hundreds of milliseconds.

The hysteresis signatures can be explained by the above transient V_T shift. The scan based I_{DDQ} tests are composed by the two modes, scan mode and quiescent mode. At the scan mode, FETs in on-state are stressed and increase V_T. FETs which turn off at the quiescent mode decrease V_T until the end of measurements. For SPIRIT, the same FETs are stressed and relaxed again, which repeats, if the increase at a scan mode and the decrease at the following quiescent mode are balanced, signatures will saturate. Figure 10 shows the relationship between I_{DDQ} and scan-in time defined as $(\#of\,ScanClocks) \times (ClockPeriod)$ of the signatures in Fig. 3. There are three scan-in time dependencies— those of I_{DDQ} at the first, second, and 100th vectors. The I_{DDQ_1} and I_{DDQ_2} show nearly logarithmic dependencies, but the saturated current, $I_{DDQ_{100}}$, shows a clear logarithmic time dependency to 50 milliseconds.

The above two logarithmic dependencies are observed in the other dies of the corner wafers as described in Section A.

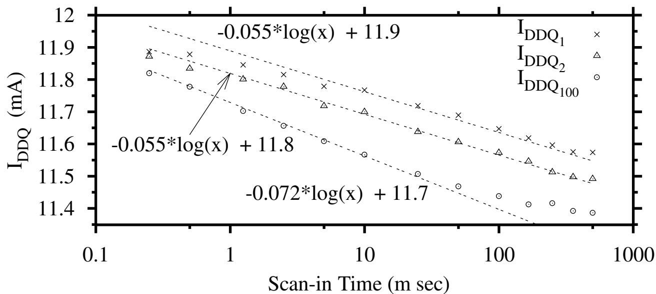

Fig. 10 I_{DDQ_1}, I_{DDQ_2}, and $I_{DDQ_{100}}$ vs. scan-in time show logarithmic time dependencies in the different time ranges: 10 - 500 m sec of I_{DDQ_1}, 0.25 - 500 m sec of I_{DDQ_2}, and 0.25 - 50 m sec of $I_{DDQ_{100}}$.

Consider the reason causing the preceding pattern dependence shown in Section 3.2. If some of FETs in off-state at the quiescent mode are stressed at scan tests, V_T shifts of the stressed FETs are larger than that without scan tests, therefore, following I_{DDQ} tests show lower currents. Lowering the speed of the scan test increases stress time, and causes more large V_T shifts. Since scan tests have no quiescent mode, where V_T recovers, the effect of lowering clock speed of the scan test is higher than the effect of lowering clock speed of the I_{DDQ} test.

4.3 Hysteresis Signatures

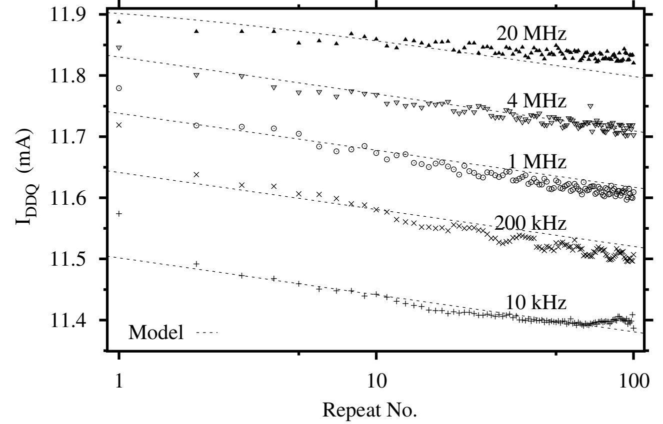

Fig. 11 I_{DDQ} signatures with scan clock frequency as a parameter show nearly logarithmic repeat number dependencies.

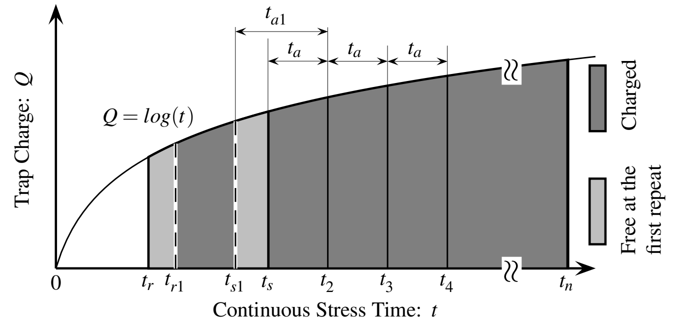

Fig. 12 Illustration of the mechanism causing hysteresis I_{DDQ} signatures on a continuous stress charge characteristic.

In this sub-section, the regularity of the hysteresis signature will be derived from the hysteresis models shown in the preceding sub-section.

The SPIRIT signatures in Fig. 4 are re-plotted in Fig. 11 with a logarithmic X-axis of the repeat number. The data points with the exceptions of the ones corresponding to the repeat number one of each curve, are on the logarithmic lines. The mechanism causing the logarithmic characteristics is illustrated in Fig. 12. Applying continuous stress fills empty traps with charges. The total charge, Q, is expressed as $Q = log(t)$. The time required for a trap to be charged depends on the distance to Si/SiO_2 interface, i.e. longer distance requires longer time [33], therefore, traps seem to be in a charge-discharge occuring order. The total charges at signatures are expressed by the following steps:

1) At the first scan mode, charging fills the traps from $t = 0$ to t_s where t_s is the corresponding continuous stress time of the scan-in time, total charge is expressed as $Q_t = log(t_s)$.

2) At the first quiescent mode, discharging occurs from the traps

which are charged in a period of $t = 0$ to t_r, and total charge after quiescent mode is $Q_t = log(t_s) - log(t_r)$.
3) At the next scan mode, first, re-charging occurs to the traps which were discharged at the preceding quiescent mode, secondly the traps over t_s are charged in an interval of t_a.
4) At the next quiescent mode, re-discharging occurs from the traps which were discharged at the preceding quiescent mode. Therefore, the remaining total charge is $Q_t = log(t_s + t_a) - log(t_r)$.
5) After the next repeat, total charge is increased by the charges filled in the same period of t_a.
Therefore, the total charge after the ith repeat, Q_{T_i}, is written as

$$Q_{T_i} = log(t_s + (i-1)t_a) - log(t_r) \quad (14)$$

$$= log(\frac{t_s}{t_r}) + log(1 + (i-1)\frac{t_a}{t_s}) \quad (15)$$

Since V_T shift is proportional to the total charge in traps [28], from Eq. (8) and (13), the hysteresis I_{DDQ} signature in a ΔV_T range of 1 mV is written as

$$I_{DDQ_i} \approx I_{DDQ_f}(1 - \alpha(log(\frac{t_s}{t_r}) + log(1 + (i-1)\frac{t_a}{t_s}))) \quad (16)$$

where I_{DDQ_f} is a stress free I_{DDQ} current, α is a constant. Since $t_s = t_r + t_a$, $t_a/t_s = 1 - t_r/t_s$, therefore if t_r is sufficiently small that $t_a/t_s = 1$, the above equation is written as

$$I_{DDQ_i} \approx I_{DDQ_f}(1 - \alpha(log(\frac{t_s}{t_r}) + log(i))) \quad (17)$$

The above equation means that I_{DDQ} signatures show logarithmic vector number dependencies.

The model curves obtained by Eq. (16) with an I_{DDQ_f} of 11.92 mA and an α of 0.0022 are plotted in Fig. 11: $t_s/t_r = 2$ and $t_a/t_s = 0.5$ for 20 MHz; and a t_s/t_r of 30, 1000, 4×10^4, and 8×10^6 with a t_a/t_s of 0 are for 4 MHz, 1 MHz, 200 kHz, and 10 kHz, respectively. The first repeats of 4 MHz, 1 MHz, 200 kHz, and 10 kHz are far from the straight lines, which is interpreted as that the traps charge order is different at the first repeats and the following repeats, i.e. $t_{s_1} < t_s$ or $t_{r_1} > t_r$.

Increasing stress time increases the amplitude of falls and estimation error, the difference between an observed current and the true I_{DDQ} current, about a DC shift of 0.5 mA is observed at 10 kHz. It seems to be that there is a strong correlation between the amplitude of fall and the DC shift. Rapid falls are observed on the signatures at higher V_{DD}. Figure 13 shows a signature at a V_{DD} of 1.7 V: a global fall with an amplitude of 0.2 mA is terminated at the 18th repeat. Please note that a large DC shift may be occuring at higher V_{DD}. Much more research is needed in order to obtain the I_{DDQ} DC shift.

On the other hand, temperature dependence is negligibly small. Figure 14 shows the correlation of conventional signatures at 25°C and 50°C. Although the I_{DDQ} amplitude of 50°C is about two times larger, r^2 shows such a high correlation of 0.86.

4.4 Signatures of the Other Dies

In previous sections, characteristics are derived from only one die. In this sub-section, these characteristics will be confirmed to the other dies of the corner wafers. As shown in Section 4.1, the mean I_{DDQ} signature, $\boldsymbol{E_M}$, is independent of dies.

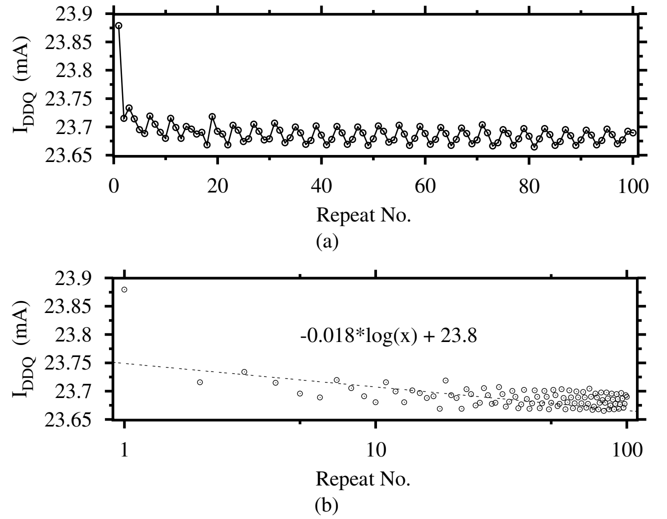

Fig. 13 SPIRIT signature at V_{DD}= 1.7 V: (a) linear plot; and (b) semi-logarithmic plot.

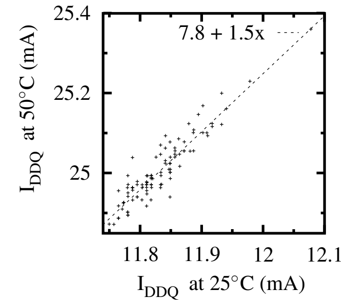

Fig. 14 Correlation of conventional signatures at 25°C and 50°C; r^2 is 0.86.

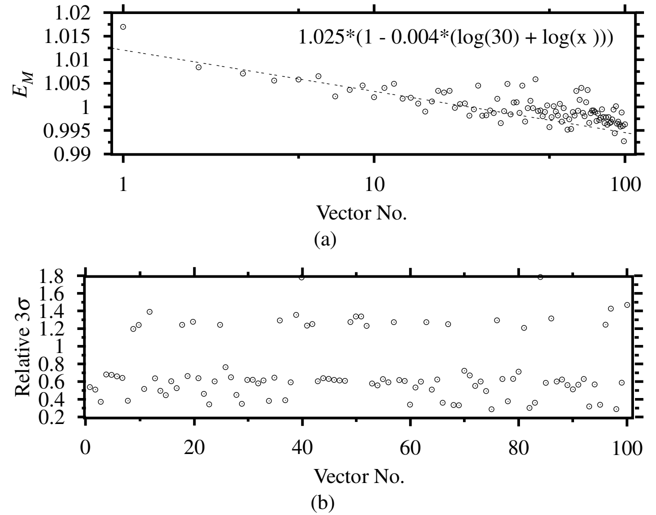

Fig. 15 Average $\boldsymbol{E_M}$ from 174 dies showing $I_{DDQ_{100}} > 1$ mA: (a) $\boldsymbol{E_M}$ shows a logarithmic vector number dependency; and (b) relative standard deviation at each vector.

As shown in Section B, $\boldsymbol{E_M}$ is constant in the hysteresis signatures having the same t_s/t_r and α. Averaging of $\boldsymbol{E_M}$ was applied on the 174 dies showing an $I_{DDQ_{100}}$ higher than 1 mA. To compare the variance of the elements of the $\boldsymbol{E_M}$, the standard deviation at each vector, σ_i ,was obtained, and σ_i was normalized by the range of $\boldsymbol{E_M}$, i.e. $3\sigma_i/(E_{M_1} - E_{M_{100}})$. The average $\boldsymbol{E_M}$ in Fig. 15 (a) shows a logarithmic vector number dependency.

The normalized 3σ in Fig. 15 (b) shows the two groups: the 25 vectors have a large variance and the 75 vectors have a small variance of 0.8.

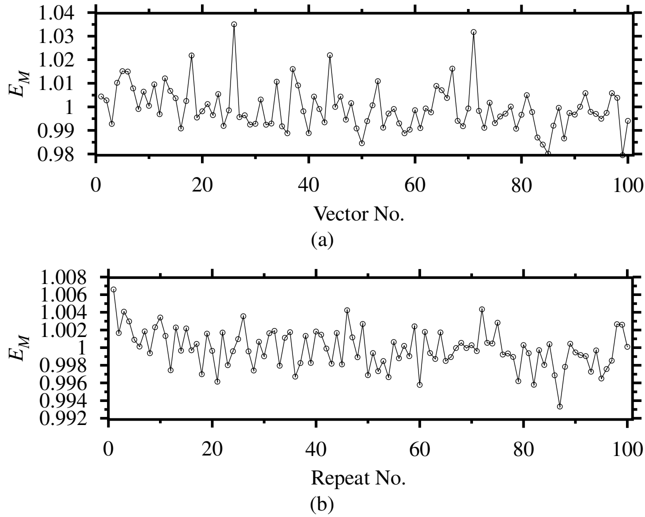

Fig. 16 Average $\boldsymbol{E_M}$s from 246 dies showing $I_{DDQ_{100}}$ < 1 mA: (a) conventional signature; and (b) SPIRIT signature.

Figure 16 shows the average $\boldsymbol{E_M}$s of 246 dies showing $I_{DDQ_{100}}$ less than 1 mA. There is no fall in the $\boldsymbol{E_M}$ of the conventional signature in Fig. 16 (a), however a small fall is observed in the $\boldsymbol{E_M}$ of SPIRIT signature in (b). The small fall seems to be hidden in the test vector dependent up down change in (a).

4.5 Pseudo Hysteresis Currents

Similar time dependencies of I_{DDQ} currents caused by the other reasons are observed in simulations and actual devices. In this sub-section, the differences between these currents and hysteresis currents will be discussed to distinguish them.

The SPICE simulations of DSM logic cells indicate that the time required for currents to settle quiescent states is large [12, 13]. The long tail transition currents in the simulations are nearly proportional time dependence, not logarithmic dependence. The BSIM3/4 models focus on the pure static leakages. These models have a discontinuity between a linear region and a sub-threshold region [35, 36]. The side effects of the simulations may be causing the long tail transitions.

I_{DDQ} drifts are caused by the discharge currents from capacitors or complementary-pair-on currents induced by floating gates. Since the capacitor leakage currents will show exponential time dependencies, signature plots with logarithmic vector number or settling time characteristics on semi-logarithmic plot will distinguish them.

If inputs of CMOS logic gates hold intermediate potential, N-FETs and P-FETs of the gates connected to the inputs are in on-state simultaneously and large currents will flow, complementary-pair-on currents. The intermediate potential is caused by not only random defect such as open gates [37], but also systematic defects: too lower V_{DD}[3], no-driven internal busses, and the floating tester pins connected to input external buffers. Decaying the potential of floating wires from V_{DD} or ground to intermediate potential or reverse decaying cause increasing or decreasing I_{DDQ}. It may take a long time to cause a change, but the change will saturate rapidly without a long tail change which is observed in the logarithmic time dependence. The amplitudes of complementary-pair-on currents depend on the saturation currents of FETs, which are larger than observed hysteresis amplitudes, and may show a weak correlation to I_{DDQ} amplitudes.

5. DISCUSSION

In this section, three topics will be discussed: an application of the hysteresis phenomena, the notes about I_{DDQ} estimation errors, and an unsolved phenomenon observed in this study.

5.1 Trap Defects

The reliability of gate oxides of MOS devices is the top priority in seventeen reliability concerns of nine manufacturers [38]. Intrinsically, the silicon substrate interface to SiO_2 is imperfect, having dangling bonds and impure materials. Therefore, oxide damage called traps occurs during or after fabrication [34]. In fabrication, impure materials such as nitrogen, hydrogen, or water react with Si and oxygen, and create traps. During operation, hot carrier injection (HCI) [24, 34] or negative bias temperature instability (NBTI) [25] can cause border traps.

However, the existence of traps in LSIs could not be detected. The results of catastrophic ruptures or degradations are detected as failures such as gate oxide shorts [39] or large V_T shifts. For example, a delay test under low V_{DD} was proposed for detecting the global and local V_T shift of 0.2 V [40]. However, DSM reliability screening requires the detection of a V_T shift of 10 mV [25]. Tewksbury and Lee measured the output of the voltage amplifier in a test chip to observe the single transistor which caused the small transient V_T shifts— a shift of 0.01 - 0.7 mV on a L_{eff} of 4 - 5 μm with a T_{ox} of 25 - 75 nm [28]. In DSM LSIs, V_T sensitive sub-threshold currents are modulated by the small V_T shifts occurring in almost all transistors, which will be detected as the indicator of a global parametric defect.

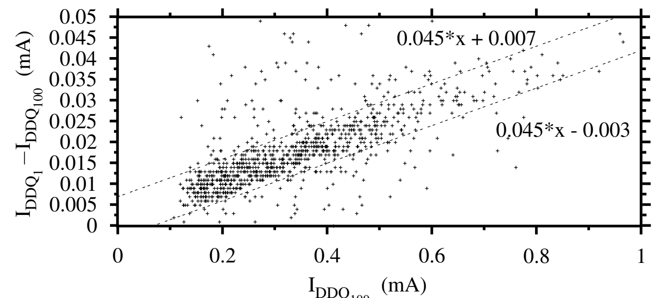

Fig. 17 $I_{DDQ_1} - I_{DDQ_{100}}$ vs. $I_{DDQ_{100}}$ of 992 dies of a rouge lot. Hysteresis amplitude is about 5% of $I_{DDQ_{100}}$.

Figure 17 shows hysteresis amplitude versus I_{DDQ} amplitude of a rouge lot, 992 dies from 16 wafers. These dies show that hysteresis amplitude, $I_{DDQ_1} - I_{DDQ_{100}}$, is about 5% of $I_{DDQ_{100}}$, which is five times larger than that of the corner wafers shown in Fig. 2. Figure 18 shows the average $\boldsymbol{E_M}$ of conventional signatures of the rouge lot at a V_{DD} of 1.2 V in (a) and at 2.0 V in (b). Whereas the dies of the corner wafers with $I_{DDQ_{100}}$ lower than 1 mA show no fall in $\boldsymbol{E_M}$ in Fig. 16 (a), the rouge dies shows a large fall in Fig. 18 (a) where vector dependent

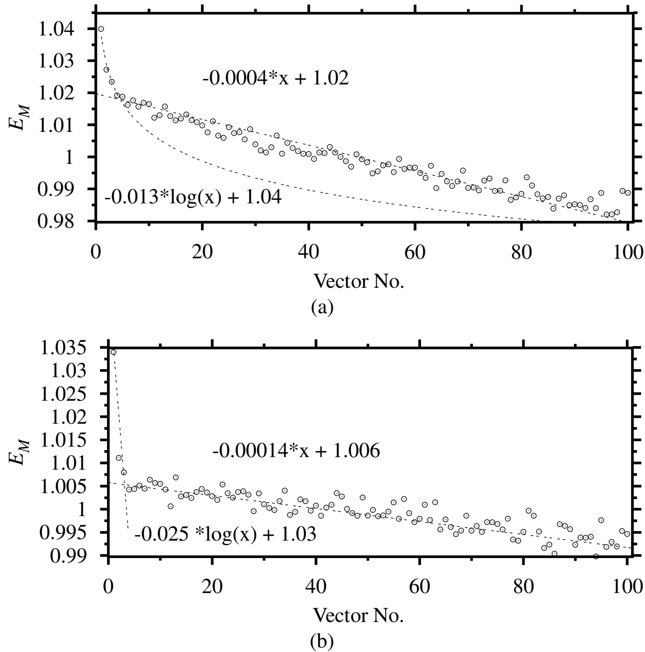

Fig. 18 Average $\boldsymbol{E_M}$s of conventional signatures of the rouge lot: (a) at a V_{DD} of 1.2 V; and (b) at a V_{DD} of 2.0 V. There are a logarithmic dependency and a linear dependency on vector number.

up down changes are difficult to identify because of the strong hysteresis characteristics. The average $\boldsymbol{E_M}$ of the rouge dies is classified into the two dependencies: logarithmic dependence and linear dependence on the vector number. The rapid logarithmic changes from the first vector to the fifth vector indicate that there are large differences between V_T-shift-free I_{DDQ} and the first I_{DDQ}, i.e. large DC shifts. Since the linear dependence is not terminated at the 100th vector, large V_T shifts may occur under actual operating conditions. The above simple qualitative extrapolations indicate that I_{DDQ} shifts are larger than 5%. We are studying the relationship between signatures and physical defects in order to set a threshold for parametric defect rejection.

The detection of global and local traps will become more important with advancing transistor down-sizing, which requires thinner oxide having high possibility to be damaged and generate border traps [33, 41]. The availability of trap detection depends on the high V_T sensitivity of sub-threshold leakage, or the sub-threshold swing parameter. Since the swing parameter is independent of T_{ox}, L_{eff}, and V_{DD} [42], this detection will be effective beyond 0.18 μm devices where V_T shifts occur.

5.2 I_{DDQ} Estimation Errors

The measured I_{DDQ} currents from hysteresis devices may include errors, underestimation errors. There are two approaches to eliminate the errors, measure before V_T shifts occur and measure after the relaxation of V_T shifts. The most simple way to avoid the V_T shifts is to measure immediately after power on, when there is no trap charge. However, running some clocks may be required to set standby mode or ATPG pattern load. As shown in Fig. 4, if enough high clocking can not be applied, then low clocking will increase V_T shifts. The relaxation characteristics shown in Fig. 8 indicates that longer strobe time will

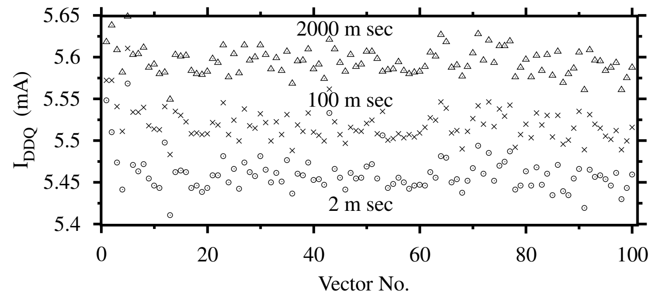

Fig. 19 I_{DDQ} signatures of Die-22-4-4 with strobe time as a parameter: 2, 100, and 2000 m sec.

decrease estimation error. The three signatures measured at the different strobe times in Fig. 19 show this. However, Fig. 8 indicates that 10 second strobe time is required to measure the true I_{DDQ}, too long for production tests.

At the non ideal environment, the effects of the estimation error on the applications should be predicted. If the effect is important, then the trap charging and discharging conditions should be maintained. It will be needed to compensate measured currents by I_{DDQ} drift characteristics for the applications requiring I_{DDQ} at shift-free V_T such as standby power estimation. The hysteresis effects on I_{DDQ} testing are very complex, because many differences exist in the models of the test methods, the targets of tests, the I_{DDQ}variance, and the degree of hysteresis. The variance in the hysteresis effects on signatures is more important than the estimation error. Because if large fluctuations occur in test thresholds, the minimum detectable defect current will be increased. As noted in Section 4.3, hysteresis causes fluctuations in signature shapes and in DC shifts. The fluctuation in the shapes is more easily predicted than that in DC shifts. Therefore, it is easier to predict the effects on the tests which focus on random defect currents, because these tests are based on the relative values of a signature, or the signature shape. It becomes more difficult to detect DC defect currents which are caused by the bridges between power and ground rails or the bridges between low controllable signals.

5.3 Another Threshold Voltage Shift

Die-11-5-8 showed opposite characteristics to the previous hysteresis studies. Die-11-5-8 was selected for the multiple analyses, because of showing no fall in the SPIRIT signature at 4 MHz in Fig. 20 (b). However, the signatures at 20 MHz and 200 kHz show nearly logarithmic rises and the signature at 100 kHz shows a peak. A logarithmic fall is observed in I_{DDQ} versus strobe time shown in Fig. 20 (a). The SPIRIT operates as an ordinal scan test. Scan-out signatures at every repeats are checked. Since Die-11-5-8 passed the all repeat scan tests, the same stress is applied on transistors at each repeat. If another mechanism changes the V_Ts of almost all transistors, I_{DDQ} will change.

It should be noted that large I_{DDQ} change such as 50% of amplitude can not be overpassed for static power consumption of mobile systems where it is important to preserve the battery. Nigh and Gattiker reported similar characteristics in the 1% of devices [22]. Much more research is needed to these phenomena.

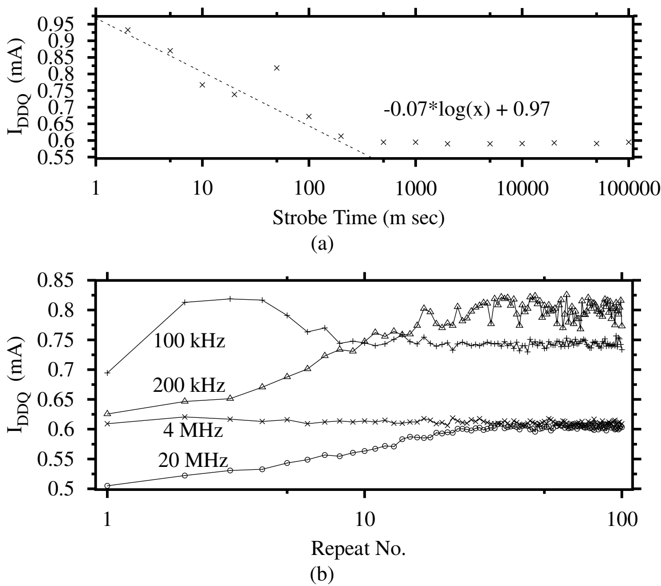

Fig. 20 Die-11-5-8 shows opposite characteristics to the other dies: (a) I_{DDQ} vs. strobe time; and (b) signatures with scan clock frequency as a parameter.

6. CONCLUSION

The newly proposed test method SPIRIT clearly indicates that intrinsic DSM I_{DDQ} currents show hysteresis phenomena. Multiple analyses of SPIRIT signatures based on the proposed theoretical I_{DDQ} model show that small threshold voltage shifts occur in almost all transistors, which varies sub-threshold leakage currents and causes I_{DDQ} shifts. The logarithmic time dependencies of I_{DDQ} fall characteristics and settling characteristics support the notion that threshold voltage shifts are caused by direct tunneling charges to pre-existing border traps. The threshold voltage shifts have been observed in long channel transistors, but cause no I_{DDQ} shift until the DSM device. Sizing of DSM devices yields high sub-threshold leakage which is highly sensitive to threshold voltage shifts. To assure the integrity of I_{DDQ} measurements, the pattern and device clock speed before measurements and the strobe time, which affect the charge, should be carefully set.

This study will assist not only in eliminating the difficulties associated with practical I_{DDQ} applications, but also in advancing knowledge about what I_{DDQ} is detecting. In long-channel devices, I_{DDQ} currents are directly increased by the currents caused by defects such as bridges or disjunctions. DSM I_{DDQ} currents are increased or decreased by the global threshold voltage shifts caused by systematic or parametric defects in almost all transistors of dies, which will open new applications of signature-based I_{DDQ} testing.

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Appendix

A. LOGARITHMIC TIME DEPENDENCIES OF OTHER DIES

I_{DDQ} versus strobe time of four dies are shown in Fig. 21 (a) with a Y-axis of the relative I_{DDQ}, the ratio of each I_{DDQ} to the I_{DDQ} at the minimum strobe time of 2 milliseconds. Although the dies having different I_{DDQ}s at the minimum strobe time, show a logarithmic dependence. Please note that these data sets are obtained after applying the same stress, the pattern used in the SPIRIT is applied one time which start immediately after power-on.

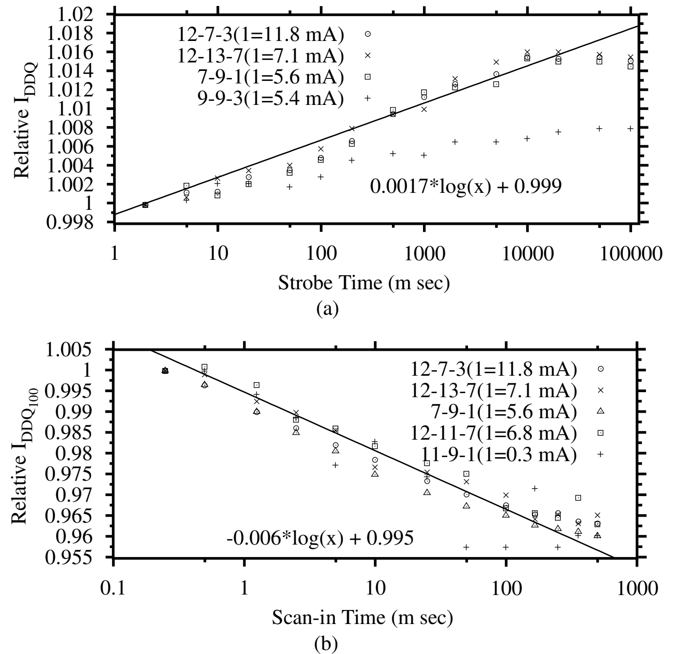

Fig. 21 Relative I_{DDQ} plots show nearly logarithmic time dependencies: (a) relative I_{DDQ} vs. strobe time; and (b) relative $I_{DDQ_{100}}$ vs. scan-in time.

Figure 21 (b) shows $I_{DDQ_{100}}$ versus scan-in time of five dies in relative $I_{DDQ_{100}}$, the ratio to the $I_{DDQ_{100}}$ at 20 MHz. The five dies show a logarithmic dependence. Die-11-9-1 shown a weak frequency dependence in Fig. 5, however, shows smooth plots on a straight line in Fig. 21 (b).

B. E_M IN HYSTERESIS SIGNATURES

From Eq. (17),

$$\begin{aligned}\sum_{i=1}^{n} I_{DDQ_i} &\approx I_{DDQ_f}(n-\alpha(nlog(t_s/t_r)+\sum_{i=1}^{n} log(i))) \\ &= I_{DDQ_f}(n-\alpha(nlog(t_s/t_r)+log(n!)))\end{aligned}$$

where n is the number of test vectors. Therefore,

$$\begin{aligned}E_{M_i} &= \frac{I_{DDQ_i}}{\overline{I_{DDQ}}} = \frac{I_{DDQ_i}}{\sum_{i=1}^{n} I_{DDQ_i}/n} \\ &\approx \frac{1-\alpha(log(t_s/t_r)+log(i))}{1-\alpha(log(t_s/t_r)+log(n!)/n)} \qquad (18)\end{aligned}$$

For the signatures having the same t_s/t_r and α, E_{M_i} is constant.