Screening VDSM Outliers using Nominal and Subthreshold Supply Voltage IDDQ

C. Schuermyer, B. Benware, K. Cota, R. Madge
LSI Logic Corporation, Gresham, Oregon

R. Daasch, L. Ning
IC Design and Test Laboratory, Portland State University, Portland, Oregon

Abstract

Very Deep Sub-Micron (VDSM) defects are resolved as Statistical Post-Processing™ (SPP) outliers of a new IDDQ screen. The screen applies an IDDQ pattern once to the Device Under Test (DUT) and takes two quiescent current measurements. The quiescent current measurements are taken at nominal and at subthreshold supply voltages. The screen is demonstrated with 0.18µm and 0.13µm volume data. The screen's effectiveness is compared to stuck-at and other IDDQ screens.

1. Introduction

This paper describes a new, two-measurement IDDQ test scheme called STIDDQ. The screen applies an IDDQ pattern once to the Device Under Test (DUT) but takes two quiescent current measurements. The first IDDQ measurement is taken at or above the nominal supply voltage and the second at a supply voltage less than 2Vt. Similar to Statistical Post-Processing™ methods, the ATE collects the raw-data and pass/fail is determined off-tester. The paper shows that the two-measurement IDDQ yields an outlier screen that is suitable for very-deep sub-micron technologies. The paper presents results for a 0.18µm ASIC and a 0.13µm large die, low yield ASIC.

Reliable screening of defective die with parametric measurements such as IDDQ is a well-recognized problem in Very Deep Sub-Micron (VDSM) technologies [1]. In short, the challenge is to separate the IDDQ measurement of normal process variation from IDDQ measurements of specific, defective dies [2]-[6]. The overlap of the two raw-data distributions poses a significant risk of test escapes, excessive yield loss or both. These circumstances have led to predictions that IDDQ, indeed any parametric measurement of the die, is unsuitable for screening VDSM defects.

In the case of IDDQ the overlap of current distributions for process variation and defective parts does not imply the defects that increase quiescent current are no longer significant in the defect pareto. Without effective screens at wafer-sort for this defect class, the part containing such a defect shifts from being a time-zero fail to a potential reliability fail. Detecting these defects and removing the parts that contain them makes a significant contribution to product quality improvement. For VDSM technology nodes it is generally accepted that a single limit threshold can be set low enough to select a large fraction of IDDQ defective parts but the screen removes healthy parts as well. The screen’s low-limit is too aggressive in identifying and removing outlier die. Balancing defect detection and yield loss from overkill is a significant concern. The yield loss and overkill concerns are the root of the prediction that VDSM technologies mark the end of IDDQ testing.

In recent years, Statistical Post-Processing (SPP) has been shown to be an effective method to screen outlier die from the original measurement distribution [3][5][6]. The generalizing idea of SPP is variance reduction of the test response distribution by data-driven techniques. To achieve reduced variance, an estimate of a part’s test response is needed assuming the part is healthy. The SPP data-driven technique obtains the estimate directly from the test response and not on measurements from pre-characterization lots or other simulation data. SPP has been shown to be effective for single parameter estimates and two parameter estimates based on nearest neighbors, location averaging and others. Studies show that removing SPP IDDQ outlier die decreases early-failure rates of the remaining die with yield loss (overkill) consistent with other VDSM screens. The key-enabling feature for production applications of SPP is off-tester binning. By changing the ATE's role from die-to-die pass/fail binning to a data acquisition role all wafer or lot test response can be brought to bear on the task of computing the test response estimate. Using only die test response and no wafer or lot statistics on-tester SPP modules are possible but the estimates are not as statistically robust.

Estimates can be obtained from the test response of the die itself (intra-die) or from neighboring die on the wafer (inter-die). SPP and other methods share the idea of variance reduction. Examples of inter-die IDDQ estimates are nearest neighbor in [3], location-averaged neighborhoods in [6] and neighbor outlier rejection in [7]. Other IDDQ methods have been reported that use intra-die, vector-to-vector data to estimate normal leakage [2][4]. This paper does not consider the vector-to-vector methods for two reasons. First, the focus of the research is data-driven per vector intra-die and inter-die IDDQ estimation. Second, the vector-to-vector methods such as ΔIDDQ in [2] cannot detect a defect that shifts all IDDQ vectors [5]. For intra-die estimates the premise is that a defect does not alter all test response measurements of a part. For inter-die estimates, an additional premise is that neighboring silicon can be used as well to estimate the effects from wafer-to-wafer or lot-to-lot processing variation on test response. For example, the Current Ratios method combines a regression analysis of characterization lots with a die's test response of a pre-selected IDDQ vector [4]. The SPP methods of Nearest Neighborhood Residual (NNR) and Location Averaging (LA) do not rely on characterization lots and use off-tester, data-driven nonparametric methods [3][6].

With an estimate for die's measurement in hand a residual is computed. The residual ($\tilde{M}$) is the difference between the original measurement (M) and the estimate ($\hat{M}$) as shown in Equation 1.

$$\tilde{M} = M - \hat{M} \tag{1}$$

If the die is healthy its residual should be near zero and the mean of the residual distribution is also near zero. For the residual distribution any deviation from zero mean depends on the ability of SPP to compute an estimate of the healthy part's test response. The zero mean is helpful but the key property for isolating outliers (defective parts) is the variance of the residual distribution. For almost any estimate method, the residual variances for both healthy and defective parts are smaller than the variance of the original test response. Methods that yield better estimates will reduce variance more and make limit setting to screen outliers from healthy parts easier.

The remainder of the paper is organized as follows. STIDDQ is described in the next section. The results sections of the paper demonstrate that two, intra-die measurements of each IDDQ vector provide an effective outlier screen and a significantly reduced SPP residual variance. The effectiveness of the STIDDQ screen is shown with 0.18µm and 0.13µm ASIC volume data by comparing STIDDQ results with two other SPP IDDQ methods; the inter-die Nearest Neighbor Residual IDDQ and intra-die speed binned IDDQ. The paper ends with an evaluation of STIDDQ limitations and a short conclusion.

2. Description of STIDDQ

The new scheme – called SubThreshold IDDQ, STIDDQ – is a modified wafer-sort IDDQ test. Normally, each IDDQ pattern is applied to the DUT at a nominal core voltage of the DUT. An IDDQ measurement is taken after the DUT supply current settles to its quiescent level. The pass/fail of the DUT's is determined on-tester by comparison of test response to a pre-selected threshold limit. In production the test is stop-on-first-fail. To obtain an estimate for each die's healthy response, STIDDQ modifies several parts of the IDDQ test. The first STIDDQ modification removes the on-tester comparison step. In its place the nominal core voltage IDDQ test response is measured and stored. The second modification is the core supply voltage is lowered to a level below 2Vt without advancing the IDDQ pattern. The reduced voltage shifts the DUT transistor operating point below subthreshold. The third, final modification is recording a second quiescent current measurement at the subthreshold voltage. The second measurement is before the IDDQ pattern is changed thus preserving the state of most DUT nodes. As described earlier the key to the success of SPP is a test response estimate for each die assuming the die is healthy. If a new IDDQ pattern were applied at second ultra-low core voltage, it would be unlikely the DUT would advance to a correct state.

With the circuit in nearly the same state the subthreshold test response estimates the die's healthy nominal voltage IDDQ. To clarify this idea Figure 1 provides a simplified circuit for the two VDD voltages. The defect is modeled as resistive and the nominal voltage on the input from the IDDQ pattern detects the defect. Figure 1a shows the circuit operating at the nominal voltage VDD (NVDD). With the input high and all but the smallest resistive defects, the NFET is operating in the linear mode and the circuit is a resistive divider. The branch current, that is the IDDQ defect current, is determined by the sum of the defect resistance and the NFET effective resistance. At subthreshold supply voltage (STVDD) the NFET gate is bias is low and the transistor operates in the subthreshold mode. At STVDD bias the NFET is best represented as a voltage controlled current source in Figure 1b. The two conditions are summarized in equations below Figure 1.

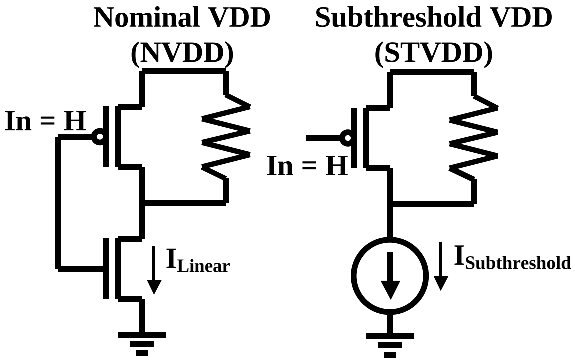

Figure 1: a) Simplified circuit IDDQ model for Nominal Voltage; b) Subthreshold Voltage Supply

$$I_{\text{Linear}} = \frac{\text{VDD}}{R_{\text{effective,NFET}} + R_{\text{defect}}}$$

$$I_{\text{subthreshold}} = I_{\text{ES}}(1 - \exp[(V_{gs} - V_T)/nKT])$$

Where I_{Linear} and $I_{\text{Subthreshold}}$ are the defect currents of the IDDQ measurement at Nominal VDD (NVDD) and Subthreshold VDD (STVDD), respectively. The current source controls the branch current independent of the size of the defect. At subthreshold VDD the current through the healthy transistor branch limits the defect's contribution to the IDDQ current and is the basis of the STIDDQ estimate of a healthy die nominal supply voltage IDDQ.

Defect-free and single defect simulations of a one thousand inverters using a 0.25µm technology are summarized in Table 1. The defect is modeled as a resistor. A defect current range is obtained by varying the resistor value. At all supply voltages defects are significantly larger than the defect-free current. The supply voltage is shown in the first column and defect free and defective currents in the remaining columns. The last row the supply voltage was initially set to 2.5V and after the circuit reached its quiescent current level the voltage was reduced to 0.4V – well below 2Vt.

Vdd (V)	I_{defectfr} (ìA)	$I_{4.5\text{KÙ}}$ (ìA)	$I_{45\text{kÙ}}$ (ìA)	$I_{200\text{kÙ}}$ (ìA)	$I_{450\text{kÙ}}$ (ìA)	$I_{4500\text{kÙ}}$ (ìA)
2.5	0.019	124.77	46.62	12.04	5.48	0.57
2.0	0.016	79.57	36.09	9.56	4.37	0.46
1.5	0.012	41.35	25.16	7.08	3.26	0.34
1.0	0.010	12.48	11.54	4.50	2.13	0.23
0.4	0.007	0.040	0.059	0.059	0.057	0.040

Table 1: Simulation of Defect-free and Defect IDDQ for Range of Supply Voltages

As expected reducing VDD reduces the IDDQ current (see Table 1 by row) and at all operating voltages above subthreshold the defect size is reflected in IDDQ current (see Table 1 by column). The last row of Table 1 represents the STIDDQ voltage program. Note for defect-free and defect size (rows and columns, respectively) the IDDQ current trends are removed. For the STIDDQ voltage program the defect test response currents are consistent with the defect-free current and the current range across all defect sizes is significantly reduced. This profile meets a key requirement of a defect-free estimate of a part's test response.

The SPP second requirement is correlation between the estimate and test response for healthy die. Estimates for the nominal voltage IDDQ are obtained by regression of I_{NIDDQ} versus I_{STIDDQ}. Several simple regression functions were used successfully. The log-log regression shown in equation 3 is a typical example.

$$Log(\hat{I}_{NIDDQ}) = b_0 + m \cdot Log(I_{STIDDQ}) \quad (3)$$

As shown in equation 1 the residual is difference of original measurement and the estimate from the subthreshold regression.

$$\tilde{I}_{NIDDQ} = I_{NIDDQ} - \hat{I}_{NIDDQ} \quad (4)$$

STIDDQ has a close relationship with the screens Current Ratio [4] and VLV [8][9]. The key differences are STIDDQ lowers the supply voltages below the ~2Vt levels used in VLV screens and unlike Current Ratios STIDDQ uses a current measurement at a reduced supply voltage to estimate the expected quiescent current of the die at nominal supply voltage levels. Finally, a supply voltage setting below 2Vt captures some of the advantages of changing the body bias to control intrinsic leakage [10].

3. Study Vehicles

Volume data for STIDDQ was collected for two ASICs. ASIC1 is 0.18μm. ASIC1 sample size is 26,021 parts. ASIC2 is a 0.13μm product and the sample size is 1600. ASIC2 was chosen because it provides a SPP VSDM test vehicle where a technique such as NNR is likely to have difficulty. First, the selected lot is lower yield than ASIC1. Second ASIC1 is a large die size. The combination of large die size and low yield is known to frustrate evaluation of NNR estimates [6]. Third, 0.13μm technology nodes have higher intrinsic leakage than 0.18μm. These characteristics potentially limit the value of IDDQ screens for VDSM technologies.

The SPP modules investigated are STIDDQ introduced in the previous section, NNR IDDQ and a third SPP module called Delay. The Delay module estimates the IDDQ leakage based on a regression fit of the IDDQ test response to the transistor delay. The transistor delay is obtained from an on-chip process monitor. The Delay module is based on the common observation that transistor delay is positively correlated to IDDQ; the slower the die the lower the leakage.

4. ASIC1 Results

Regressions are computed off-tester and recomputed for each wafer in a lot. In Figures 2 and 3 data regression is demonstrated with 0.18μm ASIC1 volume data. The NVDD IDDQ test response is on the vertical axis and the low STVDD IDDQ on the horizontal axis. Seventeen IDDQ vector pairs of 500 die that passed all other tests are plotted. The best-fit regression is used to calculate the estimate for a healthy die response. Using this regression line, the estimate and residual for all die are computed. Figure 3 is a plot of the residuals for all die. The good parts are symbolized by gray and the outliers are above the 95% limit. The 95% confidence intervals are included to demonstrate the STIDDQ downgrade thresholds for die residuals.

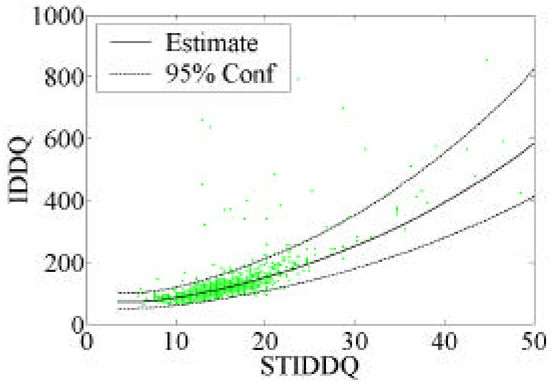

Figure 2: Nominal Voltage IDDQ vs. subthreshold IDDQ with best-fit linear regression

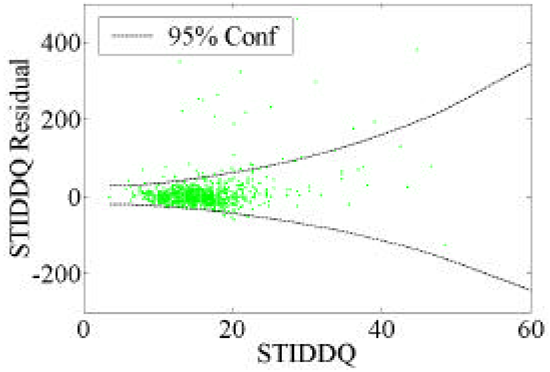

Figure 3: Residual vs. subthreshold IDDQ, horizontal lines are the downgrade thresholds

As shown in Figure 4, the expected the residual mean is near zero and the variance is significantly reduced. For all wafers (26,000 die) the STIDDQ residual variance is reduced 30% compared to the original variance. The long tail of the original distribution has disappeared to expose the outliers (see Figure 3). This analysis establishes the key SPP requirement for STIDDQ analysis. SPP estimates of a healthy part from its subthreshold IDDQ response results in a residual with zero mean and reduced variance. Note range of variance reduction obtained for the three methods. STIDDQ estimate provides a significant reduction of variance. SPP methods consistently provide the variance reduction but the results for any method will vary. The long tail in the original distribution is removed. The reduced tail is particularly dramatic for regression methods of

STIDDQ and Delay. All the SPP methods ease limit setting for outlier screening.

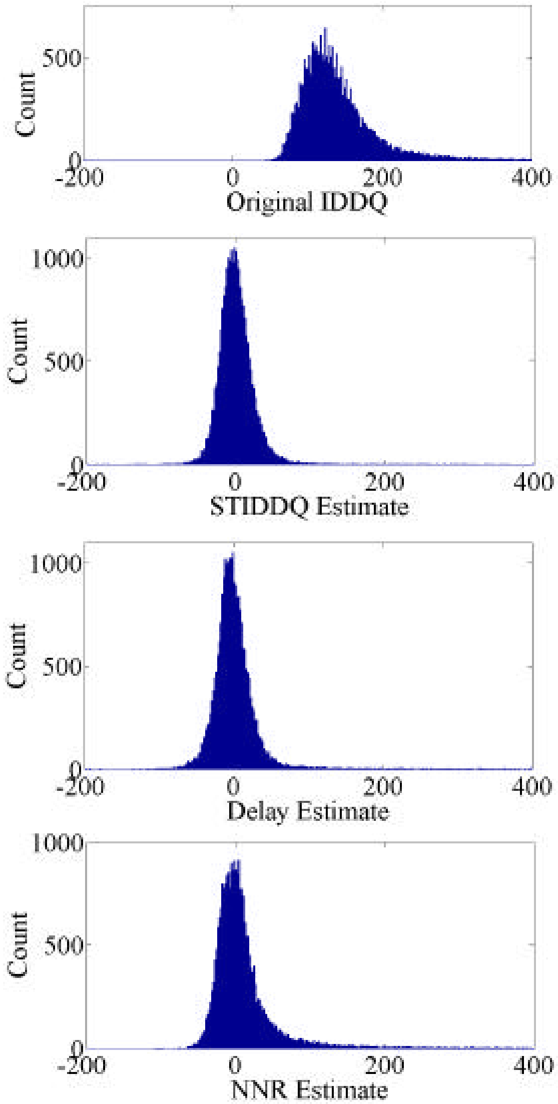

Figure 4: Residual distributions for ASIC1 for Original, STIDDQ, Delay and NNR, respectively

ASIC1, Overlap with Other Screens

Figures 5 and 6 summarize the ASIC1 results of the overlap of STIDDQ with other SPP outlier screens. The analysis used all 26,000 die. Thresholds for each of the outlier screening methods is set to keep the yield constant for each screen. The three-outlier screening methods studied are STIDDQ, NNR and Delay. STIDDQ and Delay estimates are obtained from regression models and the NNR estimate is obtained as the median value of eight to twelve nearest neighbors.

Each die in Figure 5 is plotted with its IDDQ value versus Delay, the results of a process monitor delay measurement. The symbol legend displays the pass/fail results of each outlier screen and the various combinations. For example, a die failing STIDDQ only is represented by an open diamond ‘ ’ and die failing STIDDQ and NNR by a open circle ‘ . The cross ‘×’ represents die that failed all tests. The results of passing all tests (e.g. scan, functional etc.) as well as the outlier screens are indicated in Figures 5 and 6 by the labels “Good Die” and “Pass All Tests”, respectively.

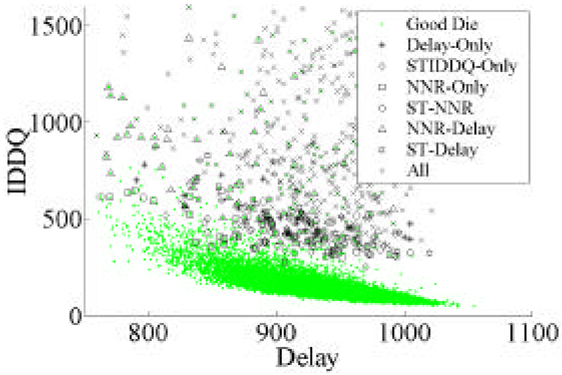

Figure 5: IDDQ versus Delay for ASIC1 Outlier Screens

In Figure 5 the common general characteristic of increasing IDDQ with decreasing delay is clearly evident. Die passing all tests form the familiar common intrinsic distribution with a wide scatter of outliers at IDDQ levels above the intrinsic limit. All screens account for the majority of the screened dies. The STIDDQ only and NNR only dies are closest to the intrinsic distribution. For NNR this characteristic is consistent with other NNR studies and what is observed in production. Although difficult to resolve NNR fails a somewhat larger fraction of die passing other tests than STIDDQ and less than Delay. The key observation from analysis is while each screen did have uniquely screened die no one screen identified all the outlier die of the IDDQ versus Delay intrinsic distribution.

Figure 6 provides a Venn diagram view of the three outlier screens. Inside each cell of the Venn diagram is the number of screened die and a small pie-chart indicating the fraction of indicated die that passed or failed tests other than the outlier screens. For example in the Venn cell labeled STIDDQ there were 57 die that uniquely failed the STIDDQ screen. The pie-chart highlights that a bit more than three-fourths of the die failed other tests. Other tests are scan and functional tests. Reading from Figure 6, there are nineteen unique Delay fails and approximately fifteen of the nineteen passed all other tests. The pie-chart in the left corner of Figure 6 shows the yield for the data set.

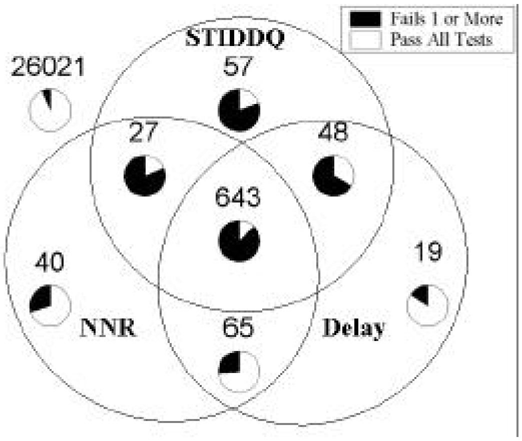

Figure 6: Venn of Outlier Screening each pie-chart shows the fraction of cell failing other tests

Examination of Figure 6 reveals a number of interesting results for the screens. All screens have a significant fraction of uniquely failing die. The center cell naturally has the largest fraction of die that failed one or more other tests. The STIDDQ screen identifies a much larger fraction of die that failed other tests. Considering the die that passed other tests, the STIDDQ screen is likely providing additional coverage that are missed by the stuck-at screen. The cells for combined STIDDQ-NNR and STIDDQ-Delay shows a larger fraction of die failing other tests. NNR and Delay both identify a much larger fraction of die that passed other tests. Unique delay is screening fractions near the rate of the overall population. As a screen NNR has been shown to screen dies that passed other tests but failed burn-in [6]. This is likely continuing in this study however a burn-in study is not planned. The different pie-chart characteristics in the cells suggest that each screen and their combinations are sensitive to different defects. This strongly suggests that all of these outlier screens need to be applied. No single screen will provide sufficient fault coverage.

The goal of the overlap and overkill analysis is to put numbers to these ideas. This analysis is summarized in Figure 7 for ASIC1. The analysis again uses stuck-at pass/fail as the basis of comparison. For the three SPP screens the overkill rates are similar. For example, 10% healthy parts scrapped means that one in ten of the scrapped die are otherwise healthy parts. Reading the rate of defective die removed at the 10% overkill shows that NNR has a slightly higher rate of removing faulty parts at 57% than STIDDQ at 55% and 51% for Delay. The rapid rise suggests that for the first 1% of overkill the screens remove 40%-45% of the defective parts. All screens similarly saturate at approximately one in five (20%) good parts and a 65% to 70% defective die screening. It is important to remember that the basis of comparison is the scan pass/fail results. A 50% failed part detection rate means that the SPP modules fail 50% of all scan fails and also failed approximately one in fifty (2%) scan passes. The implications of this analysis require additional research.

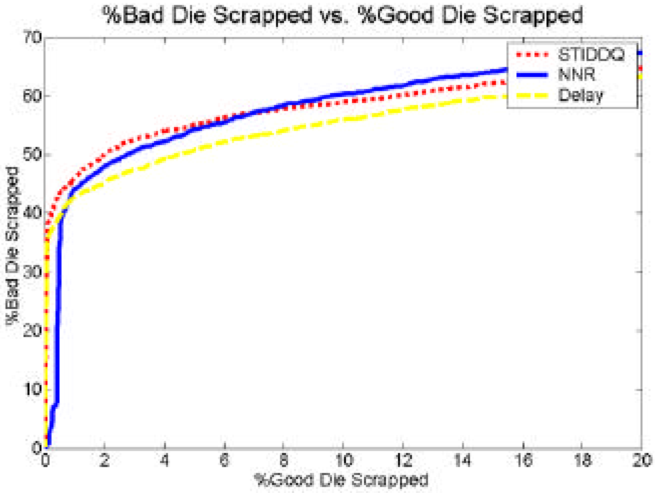

Figure 7: Screening rate of faulty parts versus scrape rate of healthy parts for SPP screens

5. ASIC2, Results

Compared to the inter-die NNR and intra-die Delay SPP modules the ASIC1 results demonstrated that STIDDQ performs well and likely identifies different defects. To continue the use of IDDQ and other parametric screens low yield and VDSM technologies pose key challenges. ASIC2 was selected to explore these challenges. ASIC2 is a 0.13µm technology, large die size and low yield sample. For inter-die based NNR the low yield is of particular concern. Recall that NNR computes the estimate of healthy die test response from the response of a die’s nearest neighbors. The foundation of the estimate is that a simple, non-parametric local model of eight to fifteen neighbors models normal process variation. Location averaging helps from the generalized and expanded the neighborhood beyond the adjacent die. Regardless of the neighborhood definition NNR cannot compute an estimate if there is no data; that is a low yield scenario. The only alternative is base the estimate on some intra-die model. The ASIC2 study concentrates on the intra-die screens. The flow of the ASIC2 study is similar to ASIC1. In the interests of brevity the presentation will be condensed to a comparison of variance reduction, overkill and overlap study.

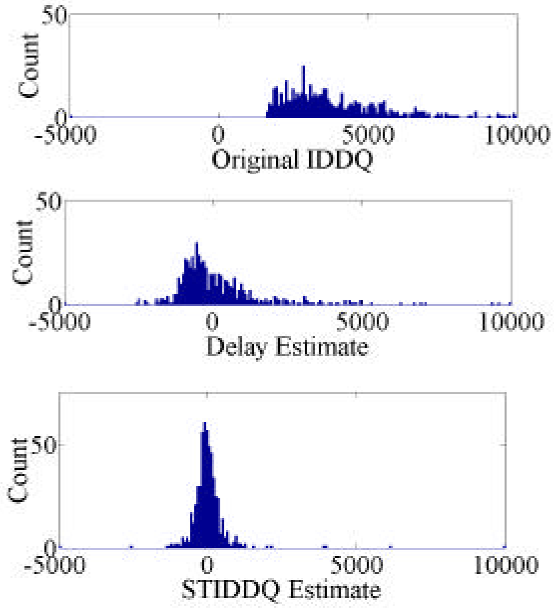

Figure 8: Residual distributions for ASIC2 for Original, STIDDQ, and Delay, respectively

Figure 8 presents the residual variance for the SPP modules Delay and STIDDQ. NNR for this data set was not possible because of the low neighbor count. Unlike the high yield ASIC1 the residuals for ASIC2 display significant differences. Specifically note the presence of a long tail in the Delay residual. Long tails are symptomatic of poor estimates. Regardless the estimate from such a regression model is poor, variance reduction is compromised and the Delay screen fails. Finally, note that the STIDDQ estimates continue to provide a significant reduction of variance in the residual. STIDDQ residual variance is roughly 50% smaller than NNR or Delay. Based on results from ASIC1 this suggests that STIDDQ will provide a superior outlier screening method at low yields and continue to be a valuable tool for VDSM outliner screening.

Figure 9 summarizes ASIC2 overkill study. For high yield the overkill was similar for the SPP modules. For ASIC2 the results clearly show STIDDQ outperforming Delay. Indeed with the exception of a lower selectivity at the highest screening and overkill ratios the STIDDQ is virtually unchanged by the shift to VDSM and low yield. This result provides additional support to the viability of STIDDQ for VDSM technologies.

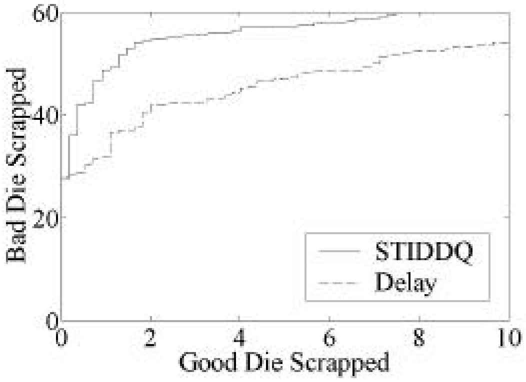

Figure 9: Screening rate for ASIC2 of faulty parts versus scrape rate of healthy parts for SPP screens

6. Conclusion and Future Work

This paper presented a new Statistical Post-Processing IDDQ screen called STIDDQ. The new IDDQ screen measures the quiescent current at two supply voltages, nominal and at a voltage below 2Vt. The second supply voltage sets the operating point of the device under testing in the subthreshold region. It was shown that the subthreshold measurement reduces the effects of IDDQ detectable defects and is well correlated with the expected, defect free IDDQ response of the die at nominal supply voltage levels. Using die that pass all tests a regression model based on the subthreshold IDDQ and nominal IDDQ is computed for each wafer. The regression model provides the essential SPP requirement, a reliable healthy die estimate for all die. Using a data-driven method such as STIDDQ alleviates the uncertainty of modeling IDDQ leakage currents from first principles [11].

STIDDQ is classified as an intra-die, intra-vector method. The key characteristics for a SPP method that is robust to large die, low yields, or both. The value of combining intra-die SPP with inter-die SPP modules alleviates the low-yield concerns when only using inter-die SPP. Using a high-yield, low DPM study vehicle the STIDDQ results show the value of adding intra-die estimate to outlier screening. The screen does not use a vector-to-vector comparison and instead uses the subthreshold operating point of the transistors to form the intra-die estimate. This eliminates the problem common to the vector-to-vector methods of not screening defects that shift all IDDQ values. The off-tester SPP screens such as NNR and STIDDQ take maximum advantage of parametric data sets. This data-driven framework provides multiple statistical views of the data to isolate outliers without significant increases in test time or test cost.

Research is ongoing to determine the limitations of STIDDQ. An assumption of STIDDQ is the leakage current is primarily subthreshold source-to-drain. The observed correlation of the subthreshold current measurement to the nominal measurement supports this assumption. When the gate oxide gets so thin that oxide tunneling dominates the leakage mechanism, STIDDQ will probably not to be an effective solution. This does not appear to be the case for the next one or two generations. A second concern is ATE requirements to discriminate measurement accuracy and the contributions of low subthreshold, current leakage. Finally, data retention in the storage elements is assumed at subthreshold levels. It is possible that data in the storage elements is lost at subthreshold levels and could place additional restrictions on the future storage element design.

The number and nature of VDSM technology unique fails are of particular interest. The need for new screens like STIDDQ will only increase as the device geometry shrinks and the intrinsic and defect leakage distributions merge.

7. References

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