

# A Scalable Scan-Path Test Point Insertion Technique to Enhance Delay Fault Coverage for Standard Scan Designs

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## Abstract

In this paper, an automatic test pattern generator (ATPG)-based scan-path test point insertion technique, which can achieve high delay fault coverage for scan designs, is proposed. In the proposed technique, shift dependency between adjacent scan flip-flops that causes some delay faults to be untestable in standard scan environment, is broken by inserting test points, which can be combinational gates as well as flip-flops. Instead of topology-based approaches used in prior publications, the proposed technique uses a special ATPG to identify pairs of adjacent scan flip-flops between which test points are inserted to improve fault coverage. Since the proposed technique inserts test points only where they are necessary, it can drastically reduce hardware overhead compared to circuit topology-based techniques. 100% transition delay coverage was attained for all ISCAS89 benchmark circuits except one. This is achieved with very small numbers of test points. On an average, about 40% reduction in scan chain length against a prior approach was achieved by the proposed method for benchmark circuits with default scan chain order.

## 1 Introduction

Ascertaining correct operation of digital circuits at desired speed is becoming more important. In the past, at-speed testing was typically accomplished with functional test patterns. However, developing functional test patterns that attain satisfactory fault coverage is unacceptable for large scale designs due to the prohibitive development cost. Even if functional test patterns that can achieve high fault coverage are available, applying these test patterns at-speed for high speed chips requires very stringent timing accuracy, which can be provided by very expensive automatic test equipments (ATEs). The scan-based delay test approach where test patterns are generated by an automatic test pattern generator (ATPG) on designs that involve scan chains is increasingly used as a cost efficient alternative to the at-speed functional pattern approach to test large scale chips for performance-related failures [1, 12].

The transition delay fault model [15] is widely used in industry for its simplicity. Due to its similarity to the stuck-at fault model, ATPGs and fault simulators that are developed for stuck-at faults can be reused for transition delay faults with minor modifications. Unlike the path delay fault model [13] where the number of target faults is often exponential, the number of transition delay faults is linear to the number of circuit lines.

This eliminates the need for critical path analysis and identification procedures, which are necessary for the path delay fault model.

Detection of a delay fault requires application of a two-pattern test; the first pattern that initializes the targeted faulty circuit line to a desired value and the second pattern that launches a transition at the circuit line and propagates the fault effect to one or more primary outputs or scan flip-flops. There are two different approaches to apply two-pattern tests in standard scan environment. In both approaches, the first pattern of a test pattern pair is scanned in through scan chains in the same fashion as a test pattern for a stuck-at fault is scanned in and the second pattern is derived from the first pattern. In the first approach, referred to as skewed-load [10] or launch-by-shift, the second pattern is obtained by shifting in the first pattern by one more scan flip-flop. Hence, given a first pattern, there are only two possible patterns for the second pattern that differs only at the value for the first scan flip-flop whose scan input is connected to the scan chain input. This *shift dependency* restricts the number of combinations of test pattern pairs to  $2^n \times 2$  [9] in standard scan environment, where  $n$  is the number of scan flip-flops in the scan chain. In the second approach, referred to as broadside-load [10, 11] or launch-from-capture, the second pattern is obtained from the circuit response to the first pattern. Hence, the second pattern is given by the circuit response to the first pattern. Due to restriction to apply the second pattern in both approaches, transition delay fault coverage in standard scan environment is sometimes significantly lower than stuck-at fault coverage [10].

Several techniques have been proposed to improve delay fault coverage in standard scan environment. In [4, 8], extra logic is inserted into the functional path to improve delay fault coverage in standard scan environment. The main drawback of this method is performance degradation entailed due to additional logic that is inserted into the functional path. Enhanced scan testing [3] is a powerful scan technique that allows to apply all possible  $2^n \times (2^n - 1)$  combinations of pattern pairs to the circuit. We refer to faults that are not testable under standard scan environment but testable under full enhanced scan environment as *dependency untestable faults*. Since this technique requires to replace all standard scan cells by enhanced

scan cells, which can hold two bits, the drawback of enhanced scan testing is high area overhead of enhanced scan cells. In order to reduce area overhead, partial enhanced scan technique where only selected scan flip-flops are replaced by enhanced scan flip-flops is proposed by [2]. As a similar approach to the partial enhanced scan technique, in [10], dummy flip-flops are inserted to break shift dependency between selected pairs of adjacent scan flip-flops in the scan chain. In [7, 9], scan flip-flops are rearranged to minimize the number of pairs of adjacent scan flip-flops that drive same fanout cones. This reduces the number of transition delay faults that are untestable due to shift dependency between scan flip-flops. However, rearranging scan chains to enhance fault coverage may increase scan path routing overhead. Furthermore, for circuits where most state inputs are topologically correlated, satisfactory transition delay fault coverage may not be achieved in any order of scan flip-flops.

In this paper, we present an ATPG-based technique to enhance delay fault coverage for standard scan designs. Since necessary test points are identified from suitable test cube pairs for target faults, which are generated by a special ATPG, rather than circuit topology, it can drastically reduce hardware overhead compared to circuit topology-based techniques. Unlike [10], which uses only flip-flops to break shift dependency between adjacent scan flip-flops, the proposed technique inserts combinational gates as well as flip-flops. This minimizes the increase in scan chain lengths, which determines test application time in scan testing, due to adding extra flip-flops into scan chains. Since combinational gates can be implemented with less silicon area, this can also reduce hardware overhead.

The rest of this paper is organized as follows. Definitions and notations that are used in the rest of paper are described in Section 2. Overall concept and contribution of the paper are described in Section 3. Section 4 introduces scan path test point insertion that is used to break shift dependency in the scan chain. The algorithms to compute test point vector and the global test point vector are also described. A special ATPG that is used to generate suitable test cubes that incur the minimum number of test points is described in Section 5. Section 6 discusses a clustering technique to reduce routing overhead for test point enable signals. The overall algorithm is summarized in Section 7. Section 8 reports experimental results. Finally, Section 9 gives the conclusions.

## 2 Definitions and Notations

In this paper, we assume that the sequential circuit under test (CUT), which has  $m$  primary inputs,  $p_1, p_2, \dots, p_m$ , and  $n$  state inputs,  $s_1, s_2, \dots, s_n$ , employs full scan and state input  $s_i$ , where  $i = 1, 2, \dots, n$ , is driven by a corresponding scan flip-flop  $D_i$  during test application. We assume that all scan flip-flops in the CUT,  $D_1, D_2, \dots, D_n$ , where  $n$  is the number of scan flip-flops in the scan chain (state inputs), are connected to comprise one scan chain without loss of generality. The chain input of the scan chain is connected to the scan input of scan

flip-flop  $D_1$  and the scan output of  $D_1$  is connected to the scan input of  $D_2$ , and so on, and finally the scan output of  $D_n$  is connected to the scan chain output. We also assume that the scan path is constructed with only non-inverting outputs of scan flip-flops, which are also used to drive the functional path. Under the assumption, during scan shift cycles, the value loaded into scan flip-flop  $D_i$  at time  $t$  is always the same as the value at the immediate predecessor of  $D_i$ , i.e.,  $D_{i-1}$ , at the previous cycle time  $t-1$ . The above two assumptions are only for convenience of illustration and the proposed method can be used for CUTs that have multiple scan chains and whose whole or part of scan paths are constructed with inverting outputs of scan flip-flops.

Let  $V^j = \{V_1^j, V_2^j\}$  be a two pattern test (or test cube pair), which may be fully or partially specified, where  $V_1^j$  is the *initialization pattern* and  $V_2^j$  is the *activation and propagation pattern* of  $V^j$ . Each pattern  $V_f^j$ , where  $f = 1$  or  $2$ , consists of two parts: primary input part that is applied to primary inputs and scan input part that is applied to scan inputs. The scan input part of initialization pattern  $V_1^j$  is applied to the CUT at *initialization test cycle*  $T_1^j$  via the scan chain and corresponding activation and propagation pattern  $V_2^j$  is applied the CUT at *activation and propagation test cycle*  $T_2^j$  by functional justification (when the broadside-load approach is used) or a shift operation (when the skewed-load approach is used).

If two pattern tests are applied via standard scan chains by using the skewed-load approach, all transition delay faults that require a 1 (0) at state input  $s_{i-1}$  at the initialization test cycle and a 0 (1) at state input  $s_i$  at the activation and propagation test cycle to be detected are untestable even if they are testable in enhanced scan environment. Hence, a pair of values, the value assigned at  $s_{i-1}$  in  $V_1^j$  and the value assigned at  $s_i$  in  $V_2^j$  are important to determine testability of transition delay faults when the skewed-load approach is used. We introduce  $d_i^j$  to denote the pair of values, i.e., the value assigned at  $s_{i-1}$  in  $V_1^j$  and the value assigned at  $s_i$  in  $V_2^j$ . If two pattern test  $V^j$  is applied via a standard scan chain by using the skewed-load approach and  $V^j$  is fully specified, then  $d_i^j$  is always 00 or 11.

## 3 Overview of Main Contribution

### 3.1 Motivation

Figure 1 shows a circuit that has three state inputs,  $s_1, s_2$ , and  $s_3$ , which are respectively driven by scan flip-flops  $D_1, D_2$ , and  $D_3$  during test application. Consider generating a test pattern pair  $V = \{V_1, V_2\}$  for the slow-to-rise (STR) fault at line  $l$  that is to be applied to the circuit by using the skewed-load approach. Initializing line  $l$  to a 0 requires assigning either  $s_1$  or  $s_2$  to a 0 at initialization test cycle  $T_1$ . On the other hand, activating and propagating the STR fault at line  $l$  require assigning all state inputs  $s_1, s_2$ , and  $s_3$  to 1's at activation and propagation test cycle  $T_2$ . However, if  $D_1$  ( $D_2$ ) is loaded with a 0 at time  $T_1$  to initialize line  $l$ , then the 0 at  $D_1$  ( $D_2$ ) shifts to  $D_2$  ( $D_3$ ) at the next cycle  $T_2$  and  $s_2$  ( $s_3$ ) is assigned a 0. This conflicts with the

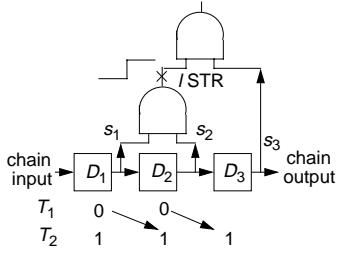


Figure 1: Shift Dependency

value 1, which is required at  $s_2$  ( $s_3$ ) to activate and propagate the fault effect. Hence, the STR fault at line  $l$  is untestable by the skewed-load approach in standard scan environment.

Consider inserting a dummy scan flip-flop between  $D_1$  and  $D_2$  (see Figure 2(a)). Again, if  $D_1$  is assigned a 0 at  $T_1$ , then the 0 at  $D_1$ , which is applied to initialize line  $l$  at  $T_1$ , shifts to the dummy flip-flop at the next cycle  $T_2$ . If the dummy flip-flop is loaded with a 1 and  $D_2$  is also loaded with a 1 at  $T_1$ , these 1's shift to  $D_2$  and  $D_3$  at  $T_2$ , respectively. Hence, if a 1 is scanned into  $D_1$  from the scan chain input at  $T_2$ , then all state inputs  $s_1$ ,  $s_2$ , and  $s_3$  are assigned 1's and the fault effect at  $l$  is activated and propagated to the circuit output at  $T_2$ .

### 3.2 Key Idea

Figure 2(b) illustrates that the STR fault at  $l$  can also be detected by inserting a two-input OR gate between  $D_1$  and  $D_2$ . Assume that  $D_1$  is assigned a 0 and  $D_2$  and  $D_3$  are assigned 1's at  $T_1$ . If signal  $E_O$ , which drives an input of the OR gate, is assigned a 1 at  $T_2$ , then  $D_2$  is loaded with a 1 instead of the 0, which is shifted from  $D_1$ . Hence, scan flip-flops  $D_2$ , and  $D_3$  can be assigned 1's at  $T_2$  that are required to activate and propagate the STR at  $l$  ( $D_1$  can be assigned a 1 by scanning a 1 into the scan chain input at  $T_2$ ). This is similar to test point insertion techniques [4, 14], which are widely used to facilitate ATPG process, improve fault coverage, and compress test patterns. While test points are inserted into functional paths in traditional test point insertion, in the proposed method, test points are inserted into the scan path, and hence no performance degradation is entailed by inserted test points.

An obvious advantage of inserting combinational gates as test points over dummy flip-flops, which can also be considered as a special type of test point, is that combinational gates such as two-input AND and OR gates can be implemented with less silicon area than flip-flops. Second, test application time of scan testing is typically determined by the number of test patterns and the scan chain length, which is determined by the number of scan flip-flops in the longest scan chain. Hence, inserting dummy scan flip-flops increases test application time by increasing the scan chain length. In contrast, inserting a combinational gate does not increase scan chain length. Another advantage is reduction in test data volume. Since test data should be provided for inserted dummy flip-flops as well as regular scan flip-flops, inserting dummy flip-flops increases test data

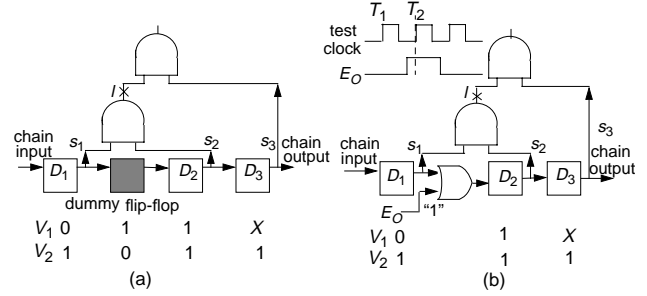


Figure 2: Breaking Shift Dependency (a) Inserting a Dummy Flip-flop (b) Inserting an OR gate

volume, which is one of the major factors that determine test cost. Test data should be provided also to combinational test points to control them. Hence, it is of importance to minimize the number of test points to minimize test data volume. Algorithms to minimize the number of test points are described in Sections 4, 5, and 6. Test data to control test points are further reduced by merging control signals for multiple test points into a single control signal (see Section 6).

Note that since test point enable signals are controlled during only scan shift cycles during which values at all normal chip input pins (primary inputs) are don't cares, test point enable signals can be shared with normal chip input pins. Therefore, no additional chip input pins are necessary to drive test point enable signals. Sharing test point enable signals with normal chip input pins may entail performance penalty since it increases load capacitance at sharing input pins. However, this performance penalty can be eliminated or minimized by inserting dedicated buffers to drive test point enable signals.

Figure 3 illustrates four different types of test points that can be inserted to enhance transition delay fault coverage for standard scan designs and their possible  $d_i^j$  values, i.e., the value assigned at state input  $s_{i-1}$  in  $V_1^j$  and the value assigned at state input  $s_i$  in  $V_2^j$ , that can be applied to a pair of adjacent state inputs  $s_{i-1}$  and  $s_i$  when each different type of test point is inserted between  $D_{i-1}$  and  $D_i$ . Note that  $d_i^j = 01$  or  $10$  cannot be applied in standard scan environment (we assume that the scan path is constructed with only non-inverting outputs of scan flip-flops). If an AND (OR) gate is inserted between scan flip-flops  $D_{i-1}$  and  $D_i$ ,  $d_i^j$  values that can be applied to  $s_{i-1}$  and  $s_i$  are 00 and 10 (11 and 01). Hence, if there exists a dependency untestable transition delay fault that requires  $d_i^j = 01(10)$  to be detected, then the fault can be detected by inserting an OR (AND) gate between  $D_{i-1}$  and  $D_i$ . If there is a set of transition delay faults that require  $d_i^j = 01$  to be detected and there is another set of faults that require  $d_i^j = 10$  to be detected, then an AND-OR (or OR-AND) complex gate or dummy flip-flop can be inserted between  $D_{i-1}$  and  $D_i$  to detect all of them. While test patterns for a set of transition delay faults that require  $d_i^j = 01$  to be detected are being applied to the CUT, the test point enable signal for the OR test point,  $E_O$ , is set to a 1 to enable the OR test point at every activation and propaga-

tion test cycle. On the other hand, while two pattern tests for the other set of transition delay faults that require  $d_i^j = 10$  to be detected are being applied to the CUT, the test point enable signal for the AND test point,  $E_A$ , is set to a 1 to enable the AND type test point and  $E_O$  is set to a 0 to propagate the 0 at the output of the AND gate to the scan input of  $D_i$ . Also when an AND (OR) test point is inserted, the test point needs to be *disabled* while test patterns for faults that require  $d_i^j = 11$  (00), i.e.,  $s_{i-1} = 1$  (0) in  $V_1^j$  and  $s_i = 1$  (0) in  $V_2^j$ , to be detected are applied.

The test application process of the proposed method consists of three phases. In the first test application phase, two pattern tests are applied by the skewed-load approach under standard scan environment. In the second application phase, test patterns, which target faults that are not detected during the first test application phase, are applied by the broadside-load approach also under standard scan environment. The first and the second phase can be exchanged without affecting resulting quality of testing. The third application phase is further divided into several sub-phases. In each sub-phase, a different set of test points are enabled every activation and propagation test cycle and the rest of test points are always disabled; for all pairs of adjacent scan flip-flops  $D_{i-1}$  and  $D_i$  whose test points are disabled, the value at flip-flop  $D_i$  at test cycle  $t$  is the same as the value at its immediate predecessor  $D_{i-1}$  at the previous test cycle  $t - 1$ . This is similar to multi-phase test point insertion [14] where different control points are activated in each test phase.

### 3.3 Comparisons with Prior Work

Unlike combinational test points such as AND and OR gates, dummy flip-flops require no test point enable signals, which entail additional routing overhead. However, dummy flip-flops contribute to extra power consumption even during normal operation (note that combinational test points do not contribute to power consumption since scan chains are not used during normal operation). Hence, if a large number of dummy scan flip-flops are inserted, then clock signals that drive dummy flip-flops should be shut down during circuit's normal operation to save power in power conscious chips such as chips for portable devices. This requires driving dummy flip-flops with a separate clock tree or through individual clock gating logics. Hence, added clock tree(s) or clock gating logics for dummy flip-flops may cost even higher routing as well as area overhead than test point enable signals of combinational test points.

As described in the preceding paragraph, [7, 10] use topological correlation measures to decide between which pairs of scan flip-flops dummy flip-flops are to be inserted and orders of scan flip-flops that minimize decrease in fault coverage due to shift dependency. In order to break shift dependency between all pairs of adjacent scan flip-flops, a large number of dummy flip-flops need to be inserted for some circuits [10]. If both skewed-load and broadside-load approaches are used, many pairs of adjacent flip-flops that have topological correla-

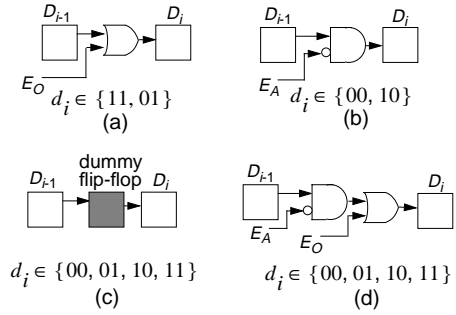


Figure 3: Various Types of Test Points (a) OR (b) AND (c) Flip-flop (d) AND-OR

tion (drive same fanout cones) may not cause any dependency untestable fault since some faults that cannot be detected by the skewed-load approach due to shift dependency between adjacent flip-flops can be detected by the broadside-load approach. Hence, inserting dummy flip-flops, replacing scan flip-flops by enhanced scan flip-flops, or reordering scan flip-flops based only on topological correlation measures, may result in unnecessarily high area and routing overhead.

Unlike [7, 10], [2] uses pre-computed test patterns to select scan flip-flops that are replaced by enhanced scan flip-flops; if there exists pair of adjacent state inputs  $s_{i-1}$  and  $s_i$  for which  $d_i^j$  is 01 or 10 (under the assumption that the scan path is constructed with only non-inverting outputs of scan flip-flops) in a two pattern test  $V^j$  of the pre-computed test pattern set, scan flip-flop  $D_i$  is replaced by an enhanced scan flip-flop. Typically, there may be a large number of two pattern tests for every dependency untestable transition delay fault. Hence, significantly different results in terms of hardware overhead can be obtained depending on which test patterns are used for consideration. In contrast to [2] where test patterns are generated in advance, in the proposed method, only suitable test cube pairs, which will result in minimal number of test points, are generated by a special ATPG (see Section 5).

## 4 Scan Path Test Point Insertion

It is important to minimize the number of test points to minimize hardware overhead and test data volume. In this paper, test points to be inserted are dynamically computed from test cube pairs for transition delay faults that are not testable in standard scan environment. A test cube pair generated by the proposed ATPG is added to a test cube pair set, which is called the *current test cube pair set*. If there currently exists test cube pair  $V^a$  in the current test cube pair set in which values for a pair of adjacent state inputs  $s_{i-1}$  and  $s_i$  are assigned a 0 in  $V_1^a$  and a 1 in  $V_2^a$ , respectively, i.e.,  $d_i^a = 01$ , then an OR gate is required to be inserted and enabled between scan flip-flops  $D_{i-1}$  and  $D_i$  to apply  $V^a$  to the CUT (see Figure 3). If  $d_i^b = 00$  in a newly generated test cube pair  $V^b$ , then  $V^b$  conflicts with  $V^a$  at  $s_i$  since  $V^b$  cannot be applied to the CUT with the OR gate enabled between  $D_{i-1}$  and  $D_i$ . Generated test cube pairs are placed into



set	TP vector	$s_1$	$s_2$	$s_3$	$s_4$	$s_5$	$s_6$	$s_7$
$C^1$	Initial $TP^1$	W	R	W	R	W	W	R
	$V_1^1$	0	X	X	0	1	X	X
	$V_2^1$	0	1	X	0	0	1	0
	updated $TP^1$	W	O	W	W0	W	W	W0
	$V_1^2$	1	1	1	0	1	0	X
	$V_2^2$	1	1	1	0	0	1	0
updated $TP^1$	W	O	W	A	W	W	W0	
final $TP^1$	W	O	W	A	W	W	W	
<b>GlobalTP vector</b>	W	O	W	A	W	W	W	
$C^2$	initial $TP^2$	W	R	W	R	W	W	R
	$V_1^3$	X	1	1	1	X	1	X
	$V_2^3$	1	0	1	0	1	X	1
	updated $TP^2$	W	W0	W	A	W	W	W1
	$V_1^4$	1	1	X	1	X	0	X
	$V_2^4$	1	0	1	X	1	X	1
updated $TP^2$	W	A	W	A	W	W	O	
final $TP^2$	W	A	W	A	W	W	O	
<b>GlobalTP vector</b>	W	AO	W	A	W	W	O	

Figure 5: Example Test Cube Sets and Test Point Vectors

$d_i^j = 11, 01, \text{ or } X1$  ( $d_i^j = 00, 10, \text{ and } X0$ ) can be added into the current test cube pair set without conflict with test cube pairs already existing in the test cube pair set; recall that if  $tp_i^k = A$  ( $O$ ), then  $s_i$  is always assigned a 0 (1) at every activation and propagation test cycle during the entire  $k$ -th test application sub-phase. This is described as the transition from state  $A$  ( $O$ ) to state  $FAIL$  in Figure 4.

**Example:** Figure 5 illustrates calculating test point vectors for two example sets of test cube pairs:  $C^1$  and  $C^2$ . Assume that adjacent pairs of state inputs,  $s_2$  and  $s_3$ ,  $s_4$  and  $s_5$ , and  $s_5$  and  $s_6$ , drive different fanout cones. Therefore,  $tp_3^k, tp_5^k$ , and  $tp_6^k$ , where  $k = 1, 2$ , are always assigned  $W$ 's in every test point vector. When test cube pair  $V^1$  is added to  $C^1$ ,  $tp_1^1$  is updated to  $O$  since  $s_1$  is assigned a 0 in  $V_1^1$  and  $s_2$  is assigned a 1 in  $V_2^1$ , i.e.,  $d_2^1 = 01$ , and  $tp_4^1$  and  $tp_7^1$  are updated to  $W0$  since  $d_4^1 = d_7^1 = X0$  in  $V^1$ . When test cube pair  $V^2$  is added to  $C^1$ ,  $tp_4^1$  is updated to  $A$  since  $d_4^2 = 10$ . On the other hand,  $tp_7^1$  holds the previous value  $W0$  since  $d_7^2 = 00$ . Assume that no test cube pair can be added to  $C^1$  without conflict after  $V^2$  is added. Now, all intermediate symbols,  $R, W0$ , and  $W1$ , are replaced by  $W$ ; in the example, the  $W0$  assigned to  $tp_7^1$  is replaced by  $W$  to produce the final test point vector  $TP^1 = \{W, O, W, A, W, W, W\}$ .

The test point vector  $TP^2$  for test cube pair set  $C^2$  also starts with the same initial vector  $TP^2 = \{W, R, W, R, W, W, R\}$  as initial  $TP^1$ . Since  $d_2^3, d_4^3$ , and  $d_7^3$  are respectively assigned  $X0, 10$ , and  $11$  in  $V^3$ ,  $TP^2$  is updated to  $\{W, W0, W, A, W, W, W1\}$  when  $V^3$  is added into  $C^2$ . Since  $d_2^4 = 10$  and  $d_7^4 = 01$  in  $V^4$ ,  $tp_2^2$  and  $tp_7^2$  are again updated to  $A$  and  $O$ , respectively, when  $V^4$  is added into  $C^2$ .  $\square$

## 4.2 Global Test Point Vector

Hardware overhead for implementing the proposed technique is determined by the number of inserted test points. The types of test points that will be inserted between each pair of adjacent scan flip-flops are expressed in the *global test point vector*,  $GTP = \{gtp_1, gtp_2, \dots, gtp_n\}$ , where  $n$  is the number of

flip-flops in the scan chain and  $gtp_i \in \{W, A, O, AO\}$  ( $i = 1, 2, \dots, n$ ). The global test point vector  $GTP$  is obtained from test point vectors as follows: If  $tp_i^k$ , where  $k = 1, 2, \dots, k_{max}$ , where  $k_{max}$  is the number of test point vectors (test cube pair sets), is assigned only  $W$  or  $O$  ( $A$ ) and assigned  $O$  ( $A$ ) in at least one test point vector, then  $gtp_i$  is assigned  $O$  ( $A$ ). Otherwise, if  $tp_i^k$  is always assigned  $W$  in every test point vector, then no test point is necessary between  $D_{i-1}$  and  $D_i$  and  $gtp_i$  is assigned  $W$ . Finally, if  $tp_i^k$  is assigned  $O$  in at least one test point vector and also assigned  $A$  in at least one test point vector, then both AND and OR test points should be inserted between  $D_{i-1}$  and  $D_i$  and  $gtp_i$  is assigned  $AO$ , i.e., AND-OR complex gate. The global test point vector is updated upon completion of a test point vector computation process.

We assume that two-input AND and OR gates and AND-OR gates are used as test points in this paper. Hence, only symbols  $A, O$ , and  $AO$  are defined for the global test point vector  $GTP$ . However, the proposed technique can be extended to include other types of test points such as dummy flip-flops or XOR gates by adding appropriate symbols to represent new types of test points. Results obtained by using two-input AND and OR gates and dummy flip-flops as test points are also presented and compared with results obtained by using two-input AND and OR gates and AND-OR gates as test points in Section 8.

Test point enable signals are created from the global test point vector as follows: If state input  $s_i$  is assigned  $AO$  in the global generator, then two test point enable signals,  $E_{i,O}$  and  $E_{i,A}$ , are created to control the AND-OR gate that is inserted between  $D_{i-1}$  and  $D_i$ . If state input  $s_i$  is assigned  $O$  ( $A$ ), then one test point enable signal,  $E_{i,O}$  ( $E_{i,A}$ ), is assigned to control the OR (AND) gate. Note that if dummy flip-flops are used instead of AND-OR complex gates, then no test point enable signals are necessary (however dummy flip-flops require additional clock signals). Test point enable signals for test point vectors shown in Figure 5 are shown in Figure 6. Since state input  $s_2$  is assigned  $AO$  in the global test point vector, two test point enable signals,  $E_{2,A}$  and  $E_{2,O}$ , are assigned for  $s_2$  to control the AND-OR test point, which is inserted between scan flip-flops  $D_1$  and  $D_2$ . On the other hand, one test enable signal  $E_{4,A}$  ( $E_{7,O}$ ) is assigned for state input  $s_4$  ( $s_7$ ), which is assigned  $A$  ( $O$ ) in the global test point vector.

## 5 The Proposed ATPG

The proposed ATPG, which is developed based on PODEM [5], generates suitable test cube pairs that will lead to the minimum number of test points by taking current test point vector  $TP^k$  and the global test point vector  $GTP$  into consideration. Controllability, observability, and test generation cost are defined to guide the proposed ATPG to generate a test cube pair that entails the smallest number of new test points when it is added into the current test cube pair set  $C^k$ .

Since testing transition delay faults requires two pattern

tests, the proposed ATPG generates a two pattern test cube pair for every target fault for two different time frames: time frame 1 for the initialization pattern and time frame 2 for the activation and propagation pattern. Therefore, we also define two separate controllability cost functions for each circuit line to take account of the two time frames. The controllability costs are used to guide the proposed ATPG when there are more than one possible backtrace paths for line justification.

The purpose of computing controllability costs of each state input is to estimate hardware cost to be incurred when line  $l$  is set to a binary value  $v$ . The controllability cost to set line  $l$  to a binary value  $v$  in time frame  $f$ , where  $f = \{1, 2\}$ , is denoted by  $Cf_v(l)$ . At any time in a test generation process, if state input  $s_i$  is assigned a 0 (1) in time frame 2, then  $C2_0(s_i) = 0$  ( $C2_1(s_i) = 0$ ) and  $C2_1(s_i) = \infty$  ( $C2_0(s_i) = \infty$ ).  $C2_v(s_i)$ , where  $v \in \{0, 1\}$ , is defined by considering the current test point vectors  $TP^k$  and the global test point vector  $GTP$  as follows: If currently  $gtp_i = AO$ , then an AND-OR gate is already assigned to the pair of scan flip-flops  $D_{i-1}$  and  $D_i$  and no further test point is necessary for the pair no matter what values are assigned to  $s_{i-1}$  and  $s_i$  in test cube pairs added later in the test point vector computation process. Hence, assigning any binary value to  $s_i$  does not cost any more test point and  $C2_0(s_i) = C2_1(s_i) = 0$ . On the other hand, if currently  $gtp_i = A(O)$ ,  $tp_i^k = R$  or  $W0$  ( $W1$ ), and  $s_{i-1}$  is assigned a 0 (1) in time frame 1, then assigning a 1 (0) to  $s_i$  requires a new OR (AND) test point between  $D_{i-1}$  and  $D_i$  (the transition from state  $R$  to state  $O$  ( $A$ ) and the transition from state  $W1$  to state  $O$  ( $A$ ) of the finite state machine shown in Figure 4). Hence,  $C2_1(s_i) = h$  ( $C2_0(s_i) = h$ ), where  $h$  is a large positive number, say 100. There are several cases of  $d_i^k$  assignments where the finite state machine shown in Figure 4 transitions to the state *FAIL*. Those assignments are forbidden due to conflicts with test cube pairs already existing in the test cube pair set and an infinite cost function is given to those assignments. That is: if  $tp_i^k = A(O)$ , then  $C2_1(s_i) = \infty$  ( $C2_0(s_i) = \infty$ ), if  $tp_i^k = W0$  ( $W1$ ) and  $s_{i-1}$  is assigned a 0 (1), then  $C2_1(s_i) = \infty$  ( $C2_0(s_i) = \infty$ ), and finally if  $tp_i^k = W$  and  $s_{i-1}$  is assigned a 0 (1), then  $C2_1(s_i) = \infty$  ( $C2_0(s_i) = \infty$ ). For all other cases,  $C2_v(s_i) = 0$ . Since the controllability costs for time frame 1 can be computed in similar fashion to those for time frame 2, the formula for controllability cost for time frame 1 is omitted due to the page limit. Since no test points are required for primary inputs, controllability costs for all primary inputs are 0.

The controllability costs for internal circuit line  $l$  in the circuit,  $Cf_v(l)$ , where  $f \in \{0, 1\}$ , which are computed in similar fashion to testability measures used in [6], are given by

$$Cf_v(l) = \begin{cases} \min_{l_a} \{Cf_c(l_a)\} & \text{if } v = c \oplus i \\ \sum_{l_a} Cf_{\bar{c}}(l_a) & \text{otherwise,} \end{cases} \quad (1)$$

where  $l_a$  and  $l$  are respectively the inputs and the output of a gate with controlling value  $c$  and inversion  $i$ . The controllability costs of state input  $s_i$  are updated when  $s_{i-1}$  is assigned a

binary value in time frame 1 or  $s_i$  is assigned a binary value in time frame 2 during test generation process and changes of controllability costs of state input  $s_i$  are propagated into internal lines directly or transitively driven by  $s_i$  to update controllability costs of those internal lines accordingly.

During test generation, all gates whose output values are currently unknown and at least one of whose gate inputs has a fault effect belong to *D-frontier* [5]. In the proposed ATPG, the observability cost function serves as a selection criterion to select a gate that is likely to incur minimum amount of additional hardware to propagate the fault effect at its input from *D-frontier*. The observability cost functions are recursively computed from primary and state outputs to primary and state inputs. The observability cost of line  $l$  is given by

$$O(l) = \begin{cases} \min_{l_o} \{O(l_o)\} & \text{if } l \text{ is a fanout stem} \\ \sum_{l_a} C\bar{c}(l_a) + O(l_o) & \text{otherwise,} \end{cases} \quad (2)$$

where in the latter case  $l_o$  is the output of gate with input  $l$  and  $l_a$  are all inputs of  $l_o$  other than  $l$ . The observability cost of line  $l$  is also the minimum cost to propagate a value at line  $l$  to one or more primary or state outputs.

In order to generate a test cube pair to detect a STR (STF) fault at line  $l$ , the fault should be initialized to a 0 (1) by the initialization pattern and activated by setting line  $l$  to a 1 (0) and propagated by the activation and propagation pattern. The cost to initialize line  $l$  to a 0 (1) is  $C1_0(l)$  ( $C1_1(l)$ ). The cost to set line  $l$  to a 1 (0) to activate the fault is  $C2_1(l)$  ( $C2_0(l)$ ). Then, the activated fault effect should be propagated to one or more primary and state outputs. The cost to propagate the activated fault effect at line  $l$  is  $O(l)$ . Hence, the test generation cost to generate a test cube pair for the STR fault at line  $l$  is defined as the sum of three cost functions:

$$T_{STR}(l) = C1_0(l) + C2_1(l) + O(l). \quad (3)$$

Similarly, the test generation cost to generate a test cube pair for the STF fault at line  $l$  is

$$T_{STF}(l) = C1_1(l) + C2_0(l) + O(l). \quad (4)$$

## 6 Clustering Test Point Enable Signals

As described in Section 4, different test points are enabled in each test application sub-phase. However, many test point enable signals are assigned equivalent values (an  $X$  is equivalent and also opposite to any binary value) in every test application sub-phase. Any two test point enable signals  $E_{a,y}$  and  $E_{b,z}$  ( $y, z \in \{O, A\}$ ) are not *compatible* if  $E_{a,y} = v$  and  $E_{b,z} = \bar{v}$  ( $v \in \{0, 1\}$ ) in any generator. Otherwise,  $E_{a,y}$  and  $E_{b,z}$  are compatible. The definition of compatible inputs can be expanded by considering inverse relation, i.e., test point enable signals that are always assigned opposite values. A set of compatible or inversely compatible test point enable signals are grouped together and driven by a common control signal.

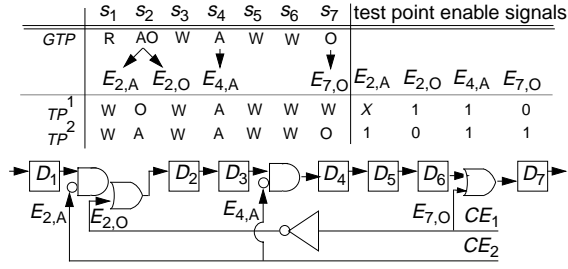


Figure 6: Clustering Test Point Enabled Signals

For example, in the two test point vectors shown in Figure 6,  $E_{2,A}$  and  $E_{4,A}$  are assigned equivalent values ( $E_{2,A}$  is a don't care ( $E_{2,A} = X$ ) and  $E_{4,A}$  is enabled ( $E_{4,A} = 1$ ) in  $TP^1$  and  $E_{2,A} = E_{4,A} = 1$  in  $TP^2$ ),  $E_{2,O}$  and  $E_{7,O}$  are assigned opposite values in both  $TP^1$  and  $TP^2$  ( $E_{2,O} = 1$  and  $E_{7,O} = 0$  in  $TP^1$  and  $E_{2,A} = 0$   $E_{4,A} = 1$  in  $TP^2$ ). Hence,  $E_{2,O}$  and  $E_{4,A}$ , which are always assigned opposite values, are connected through an inverter and driven by cluster test enable signal  $CE_1$  and  $E_{2,A}$  and  $E_{4,A}$ , which are always assigned equivalent values, are directly connected and driven by cluster test enable signal  $CE_2$ . Note that while test point vectors require 4 test point enable signals,  $E_{2,A}$ ,  $E_{2,O}$ ,  $E_{4,A}$ , and  $E_{7,O}$ , all test point enabled signals can be controlled by only 2 cluster test enable signals,  $CE_1$  and  $CE_2$  (see the bottom circuit of Figure 6)

Since we use a greedy approach to find the minimal number of cluster test point enable signals to minimize routing overhead, the first few clusters have a large number of compatible test point enable signals and the rest of clusters contain very few compatible test point enable signals. Typically, the last few clusters contain only 1 compatible test point enable signal. Hence, for circuits that have routing congested area, it is better to replace combinational test points that are controlled by cluster test enable signals that drive only 1 test point enable signal with dummy scan flip-flops to reduce routing overhead.

## 7 Overall Algorithm

Overall algorithm for test point design is outlined below.

1. Identify dependency untestable transition delay faults by running a regular transition delay ATPG under standard scan environment.
2. Initialize global variables;  $k \leftarrow 0$ ,  $j \leftarrow 0$ , and  $GTP \leftarrow \{W, W, \dots, W\}$ .
3. Initialize the current test cube pair set,  $C^k \leftarrow \phi$ , and the current test point vector,  $TP^k = \{W, I, \dots, I\}$ , where  $I = W$  if corresponding state input  $s_i$  drives no fanout cones that its immediate predecessor state input  $s_{i-1}$  drives; otherwise  $I = R$ , and unmark all faults in the fault list (see Section 4.1).
4. If there are no more faults in the fault list, then go to Step 7. Select an unmarked fault that has the minimum test generation cost in the fault list, mark the fault, and generate a test cube pair  $V^j$  for the fault by the proposed ATPG (see Section 5).
5. If the generated test cube pair  $V^j$  cannot be added into  $C^k$  due to conflict with any test cube pair existing in  $C^k$ , then dis-

card the generated test cube pair and go to Step 4 (see Section 4.1).

6. If there exist no more unmarked faults in the fault list for which a test cube pair can be generated without conflict with already existing test cube pairs in  $C^k$ , then replace all intermediate symbols,  $R$ 's,  $W0$ 's,  $W1$ 's, in the current test point vector  $TP^k$  with  $W$ 's, and generate two pattern tests for all faults for which test cube pairs are added into  $C^k$  with test points enabled according to  $TP^k$ , run fault simulation with the generated two pattern tests to drop detected faults, update the global test point vector according to the final test point vector  $TP^k$ , increment  $k$  by 1, and go to Step 3. Otherwise, add the test cube pair  $V^j$  into  $C^k$ , increment  $j$  by 1, and update  $TP^k$  accordingly and go to Step 4 (see Section 4.1).

7. Insert test points and generate test point enable signals according to the global test point vector (see Section 4.2).

8. Find compatible test point enable signals and create cluster test enable signals (see Section 6).

## 8 Experimental Results

Table 1 shows experimental results for full scan versions of IS-CAS 89 benchmark circuits. The experiments were conducted on a SUN Microsystem's Ultra 1 with 1 Giga bytes of memory. The column # *FFs* shows the number of scan flip-flops in each benchmark circuit. Experiments were conducted for two different versions of circuits whose scan flip-flops are arranged in a different order.

Columns under the label *Default Scan Chain Order* are results for versions of circuits where scan flip-flops are ordered in the scan chain in the order they appear in the netlist and columns under the label *Optimal Scan Chain Order* are results for versions of circuits where scan flip-flops are ordered to minimize the number of pairs of adjacent scan flip-flops that drive same fanout cones. Experimental results are shown for circuits whose default scan chain order versions have at least one dependency untestable transition delay fault. Columns # *dep. fts* show numbers of dependency untestable transition delay faults considered for scan path test point insertion, which remain undetected after all transition delay faults that are detected by the skewed-load and the broadside-load approach under standard scan chain environment are dropped. Columns # *dep. FF* show numbers of pairs of adjacent scan flip-flops that drive same fanout cones. Columns under headings *A*, *O*, *AO* are results when two-input AND, OR gates and AND-OR complex gates are used as test points, and columns under headings *A*, *O*, *DFF* when two-input AND and OR gates and dummy flip-flops are used as test points. Columns *time sec.* present CPU times in seconds for the entire process for the proposed technique, which include dependency untestable fault identification, test point vector computation, and test pattern generation and fault simulation using inserted test points, and clustering compatible test point enable signals. Results obtained by using the proposed technique compared with those obtained by a topology-based approach [10], where a dummy flip-flop is inserted into

Table 1: Experimental Results

CKT Name	# FFs	Default Scan Chain Order											Optimal Scan Chain Order										
		# dep. fts	[10]		Proposed								# dep. fts	[10]		Proposed							
			# dep. FFs	A,O,AO				A,O,DFF				# dep. FFs		A,O,AO				A,O,DFF					
				TL %	HO %	# TP	# CE	time sec.	TL %	HO %	# TP			# CE	TL %	HO %	# TP	# CE	time sec.	TL %	HO %	# TP	# CE
s208	8	15	7	44	75	7	1	0.1	44	75	7 (0)	1	17	7	44	75	7	2	0.2	44	75	7 (0)	1
s298	14	16	7	32	82	3	4	0.2	23	68	3 (2)	1	10	5	25	80	3	2	0.1	18	70	3 (1)	1
s344	15	8	14	47	95	2	2	0.1	43	91	2 (1)	1	5	11	41	93	2	2	0.1	13	89	2 (1)	1
s349	15	8	14	47	95	2	2	0.1	43	91	2 (1)	1	5	11	41	93	2	2	0.1	13	89	2 (1)	1
s386	6	11	5	42	75	4	4	0.3	17	65	4 (1)	1	17	5	42	70	4	3	0.3	25	50	4 (2)	1
s420	16	31	15	47	75	15	4	0.7	41	82	15(2)	2	15	15	47	82	11	9	0.8	25	47	11(7)	2
s444	21	18	13	37	68	6	3	0.5	23	60	6 (5)	1	5	4	15	88	1	1	0.2	9	75	1 (1)	0
s510	6	20	5	42	65	5	5	0.6	8	15	5 (4)	1	25	5	42	55	5	5	0.8	8	15	5 (4)	1
s526	21	49	14	39	79	8	4	0.6	25	63	7 (5)	1	9	5	19	85	3	3	0.3	11	75	2 (1)	1
s820	5	63	4	40	56	4	6	4.6	10	19	4 (3)	1	63	4	40	56	4	6	4.6	10	19	4 (3)	1
s832	5	63	4	40	56	4	6	5.0	10	19	4 (3)	1	63	4	40	56	4	6	5.0	10	19	4 (3)	1
s838	32	65	31	48	73	31	5	3.5	40	60	31(6)	4	40	31	48	81	23	12	4.3	34	60	23(9)	4
s953	29	18	5	14	70	5	3	3.2	11	60	5 (1)	2	0	0	0	-	0	0	-	0	-	0(0)	0
s1423	74	8	62	45	98	4	1	12	45	98	4 (0)	1	0	58	44	-	0	0	-	44	100	0(0)	0
s1488	6	46	5	42	50	5	6	8	0	0	5 (5)	0	48	5	42	50	5	7	9.9	0	0	5(5)	0
s1494	6	46	5	42	50	5	6	8	0	0	5 (5)	0	48	5	42	50	5	8	10.2	0	0	5(5)	0
s5378	179	120	114	39	88	43	13	35	34	81	43(15)	3	16	35	16	94	6	3	24.7	11	91	6(2)	2
s9234	228	231	178	44	90	53	12	211	38	82	54(25)	3	42	72	24	92	19	3	146	17	92	9(1)	3
s13207	669	234	404	38	92	105	23	302	36	89	106(22)	5	2	61	8	99	2	1	202	8	99	2(0)	1
s15850	597	428	406	40	91	120	29	1140	36	85	120(40)	5	7	109	15	99	4	1	790	15	99	4(0)	1
s38417	1636	88	1038	39	99	30	4	2962	39	99	30 (6)	3	73	75	4	99	1	1	2768	4	100	1(0)	1
s38584	1452	753	1296	47	95	221	16	3616	45	92	221(70)	4	75	64	4	97	6	2	2911	4	96	6(1)	1

every pair of adjacent flip-flops that have topological correlation. Columns *TL %* show expected reduction in test application time in per cent when same numbers of test patterns are applied by using [10] and the proposed method. Numbers of cluster test enable signals (columns # *CE*) and numbers of test point enable signals (columns # *TP*), which include both combinational gates and dummy flip-flops, are reported for both default and optimal scan chain order versions (numbers in shown in parentheses in columns # *TP* denote numbers of dummy flip-flops). Columns *HO %* show reduction in area overhead in per cent obtained by the proposed technique over [10]. We calculated area overhead without considering routing overhead under the assumption that sizes of flip-flop and an AND-OR gate are respectively four times and twice larger than that of an AND and the size of an OR gate is the same as that of an AND gate.

100% transition delay fault coverage was achieved for all circuits except s38417 for which the proposed ATPG aborted test generation for 7 faults when backtrack limit of 20,000 was used. This is achieved with small numbers of test points, which are significantly fewer than numbers of pairs of adjacent flip-flops that drive same fanout cones. Ratios of numbers of test points (columns # *TP*) to numbers of pairs of adjacent flip-flops with topological correlation (columns # *dep. FF*) are even lower for large benchmark circuits. For all benchmark circuits, numbers of test points inserted for optimal scan chain order versions are smaller than or equal to those of test points inserted

for default scan chain order versions. Very few test points are inserted even for large circuits when scan chains are ordered to minimize numbers of pairs of adjacent scan flip-flops that are topologically correlated.

All transition delay faults were detected for optimal scan chain versions of s953 and s1423 in standard scan environment. Hence, no test points were inserted for these circuits. Note that the optimal scan chain version of s1423 has 58 pairs of topologically correlated adjacent flip-flops. However, all transition delay faults were detected without any test point. This demonstrates that if both skewed-load and broadside-load approaches are used, using only topological analysis to break shift dependency between adjacent flip-flops may result in unnecessarily high hardware overhead.

Columns *TL %* show that scan chain length can be reduced by 14-48% for default order versions of circuits when only combinational gates are used as test points. Even when dummy flip-flops are used as test points, about 40% of reduction in scan chain lengths is obtained for default scan chain order versions of large benchmark circuits. Note that when dummy flip-flops are used as test points as well as combinational gates, the majority of test points inserted are combinational gates, which do not increase scan chain length, for default scan chain order versions of all benchmark circuits. This implies that test application time will not significantly increase even if dummy flip-flops are used as test points. For optimal scan chain order versions of some

large circuits such as s38417 and s38584, reduction in scan chain length is not spectacular. However, optimal scan chain ordering is often not practical since it may cost prohibitively high routing overhead. Even for those circuits, the proposed method reduced significant numbers of test points (74 and 58 test point reduction, respectively).

Experimental results demonstrate that area overhead can be drastically reduced by the proposed technique. Similar or higher reduction is obtained even for optimal scan chain order versions of circuits. Larger reduction in area overhead is obtained for large circuits (for all largest benchmark circuits, higher than 90% reduction in area overhead is achieved when only combinational test points are used). It is notable that for s38417 the proposed technique requires only 1 % area overhead of [10].

Cluster test enable signals contribute to routing overhead. While a dummy flip-flop requires only one extra signal (clock signal) to be routed, an AND-OR test point require two test point enable signals to be routed. Hence, it is more desirable to use dummy flip-flops instead of AND-OR complex gates for circuits that are routing congested. On the other hand, if a chip is area limited, or reducing test application time is a primary concern, using AND-OR gates will be a better choice. This flexibility is one of strong advantages of the proposed techniques among others over prior publications [2, 3, 10]. The reported run times of our programs are comparable to those of regular ATPG and fault simulator. This demonstrates the feasibility of the proposed technique. Run times of our program for both default and optimal scan chain order versions are similar.

## 9 Conclusions

In this paper, an ATPG-based scan-path test point insertion technique, which can achieve high delay fault coverage for scan designs, is proposed. Experimental results show that the proposed technique can achieve very high delay coverage with low hardware overhead. Instead of topology-based approaches [10, 7], the proposed technique uses a special ATPG to identify pairs of scan flip-flops between which test points are inserted to improve fault coverage. Since the proposed technique inserts test points only where they are necessary, it can drastically reduce hardware overhead compared to circuit topology-based techniques. The reduction in numbers of inserted dummy flip-flops in turn reduces the increase in scan chain length, which is one of major factors that determine test application time in scan testing. Use of combinational gates as test points further reduces increase in scan chain lengths. Since only small numbers of dummy flip-flops for which test data should be provided are inserted, the proposed technique can also reduce test volume. The time complexity of the proposed ATPG is comparable to those of regular ATPGs. Hence the proposed design methodology is applicable to large circuits.

In this paper, we focus only on the transition delay model. However, the proposed method can be extended to improve

fault coverage for other fault models that require two pattern testing such as path delay and stuck-open fault models. The framework of the proposed method can also be used in random pattern testing as well as deterministic testing. In random pattern testing, cluster test point enable signals should be driven by a random pattern generator.

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