

First IC Validation of IEEE Std. 1149.6

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Abstract –This paper provides proof of concept for the newly-approved 1149.6 standard by investigating the first silicon implementation of the test receiver. EXTEST and EXTEST_PULSE tests were applied to functional channels as well as channels with a set of externally-induced hard defects. All valid signals were correctly received, and all defects were detected, thus validating both 1149.6's anticipated backwards compatibility with 1149.1 and fault coverage. Mission-mode tests showed no performance degradation due to the test circuits. Characterization across PVT of the test receiver suggests 1149.6's robustness with respect to noise.

Index Terms – 1149.6, test receiver.

I. INTRODUCTION

IEEE Std 1149.6 [1] extends the capability of IEEE Std 1149.1 [2] to test AC-coupled external connections as well as differential nets. The goals of 1149.6 are to provide high fault coverage, robust noise rejection, scalability to higher frequency designs, reliability across process, voltage and temperature, and compatibility with existing test standards and devices. Mission-mode performance testing is not covered by the standard. For details on the technical background of the standard including the test receiver please consult [3].

An 1149.6-compliant IC must include, among other things, test receivers that monitor all AC coupled and differential input pins. The test receiver must be capable of performing two functions: 1) level detection, for DC coupled connections as defined in 1149.1 using the EXTEST instruction, and 2) edge detection, for AC coupled connections using the EXTEST_PULSE or EXTEST_TRAIN instruction. When detecting edges, the test receiver is designed to reject input signals that do not persist above a specified hysteresis voltage, V_{hyst} , for at least a minimum time period, T_{hyst} .

To provide the first IC validation of the 1149.6 standard as detailed in Draft 2.3 [4] (this was the latest draft version of the proposed standard at the time of the design), a 0.13 micron, 1.2V IC was implemented with the following boundary scan additions:

- test receivers on each leg of the differential receiver pins of nine TX (transmitter) and RX (receiver) pairs: eight on-board AC coupled pairs and one on-chip AC coupled pair
- TX boundary scan changes for pulse launch
- new TAP instruction – EXTEST_PULSE

Both EXTEST and EXTEST_PULSE were subjected to a test suite of normal operation input signals as well as injected defects in order to demonstrate correct functional operation, high fault coverage, and backward compatibility of the test receiver. Preliminary noise rejection characterization of the test receiver was performed. In particular, V_{hyst} and T_{hyst} of the input signal were measured.

The paper first gives an overview of the test receiver and test setup. Test results and receiver characterization data is reported next. Lastly, results and conclusions are discussed.

II. TEST RECEIVER

The test receiver is the most critical part of the 1149.6 standard since it is responsible for correctly detecting transmitted logic levels and edges. Figure 1 shows a basic block diagram of the implemented test receiver. Please note that this diagram is essentially the same as Figure 31 of P1149.6 Draft 2.3 [4].

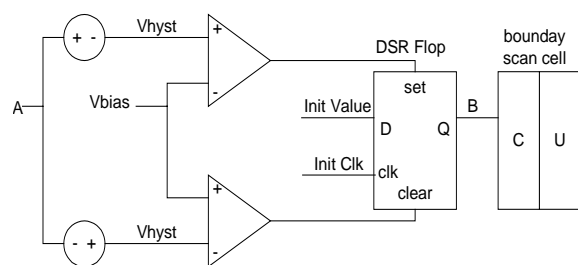


Figure 1: Test Receiver

Label A in Figure 1 indicates the test signal input to the test receiver. The received data is compared to a voltage bias, V_{bias} (by permission 6.2.3.2 of 1149.6 because each test receiver will always be AC coupled to its driver and to be operating in edge-detection mode). The two comparators control the set and clear inputs to the D flip-flop (DSR Flop) that then provides data to the boundary scan cell (C and U represent the Capture and Update flops in the cell).

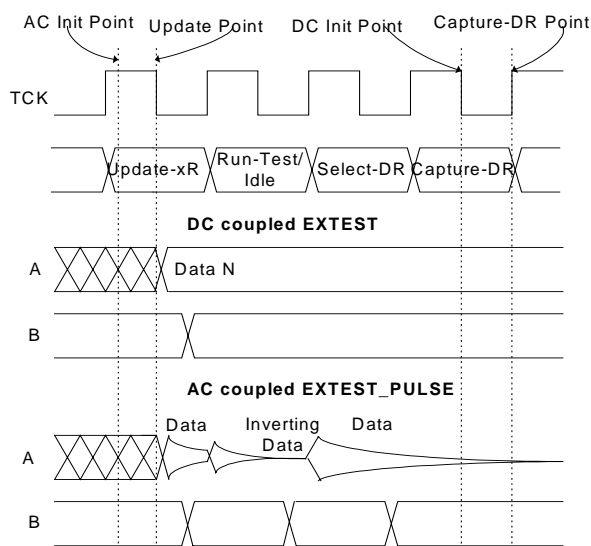


Figure 2: Test Receiver Timing

A timing diagram of EXTEST/EXTEST_PULSE is shown in Figure 2. During the 1149.1 EXTEST instruction, the DSR Flop captures the Init Value on the falling edge of TCK during the Capture-DR state of the TAP controller, which is when the Init Clk fires. A valid level detected by the test receiver will cause either a set or clear. If this event occurs after the Init Value is captured but before the next rising edge of TCK, the boundary scan cell will capture the logic level. If a valid level is not detected, the boundary scan cell will capture the Init Value.

During the new 1149.6 EXTEST_PULSE instruction, the DSR Flop captures the Init Value upon entering the Update-DR state, which is when the Init Clk fires. A valid edge recognized by the test receiver, after entering the Update-DR state and before exiting the Capture-DR state, will cause a set or clear to overwrite the Init Value. Upon exiting the Capture-DR state, the boundary scan cell will capture the output of the DSR Flop. Please note that the input transition that occurs when entering the RTI state must decay away before exiting the RTI state.

III. TEST SETUP

Each packaged part was tested in a socket on a characterization board that connected to I/O channels by SMA (Sub-miniature Type A) connectors. Coaxial cables were used to make SMA-to-SMA connections. All tested TX/RX pairs were AC coupled on chip or on board.

A diagram of an on-board AC coupled TX/RX pair is shown in Figure 3. An on-chip AC coupled pair is configured the same except that the capacitors are moved to the other side of the RX termination resistors.

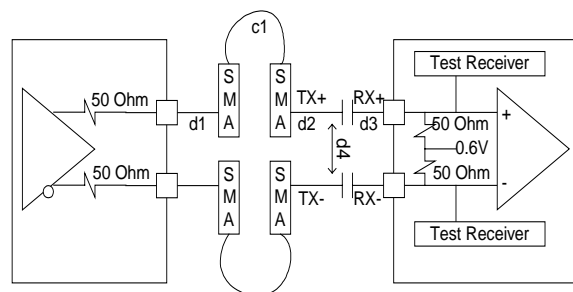


Figure 3: On-board AC coupled TX/RX Pair

The distances labeled d1-d4 are ranges over the TX/RX pairs tested. These values were d1=2889-9020mils, d2=343-375mils, d3=4804-8615mils, and d4=50-500mils. The distances between traces of adjacent TX/RX pairs fit into the d4 range. The label c1 indicates an SMA-to-SMA coaxial cable. The cables were 50 Ohms, 14.7pF, and 6 inches in length. The AC coupling capacitors were 10nF. Please note that the RX termination was through 50 Ohm resistors to a high impedance common mode voltage, V_{com} , nominally 0.6V. All defects were induced at the Fault Points labeled TX+, TX-, RX+, and RX-. Defects could not be induced on the RX+/- nodes for the on-chip AC coupled pair (as these nodes are inside the silicon and not accessible on the board).

The V_{hyst} and T_{hyst} measurements were obtained by driving edges into the test receiver from a Bit Error Rate Tester that produced edges with a 10-90% transition time of less than 30ps. The on-chip transmitters, used in all other tests to drive the test receivers, produced edges with rise and fall times of approximately 60ps. A 2G SA/s, 500MHz HP54542C oscilloscope with 10:1, 9pF, 1M Ω probes was used to capture all data images. TCK was run at 1.042 MHz in compliance with the RTI duration rule mentioned in Section II.

IV. TEST RESULTS

Tests were performed on nine TX/RX pairs (eight on-board AC coupled pairs, one on-chip AC coupled pair) over a Process, Voltage, Temperature (PVT) matrix: one slow, nominal, and fast process part each, voltages 1.08V, 1.2V, and 1.32V, and temperatures 0°C, 55°C, and 110°C.

Except where noted, all tests were performed on both on-board and on-chip AC coupled pairs over all Init Values. “V” indicates the test receiver’s boundary scan cell captured the Init Value.

A. MISSION MODE

Bench characterization of the TX/RX pairs in mission mode (i.e. normal operation) indicated that there was no measurable impact on performance due to the presence of the 1149.6 test circuitry.

B. EXTEST (1149.1 Compatibility)

The EXTEST results of driving the TX+/- nodes to specific logic levels for both AC and DC coupled connections are shown in Table 1. Induced DC shorts across on-board AC coupled capacitors were used in DC coupled tests. Results are as expected.

Table 1 EXTEST Results across PVT

Test driving levels TX+ TX-	DC Coupled captured data RX+ RX-	AC Coupled captured data RX+ RX -
a. 00	00	VV
b. 01	01	VV
c. 10	10	VV
d. 11	11	VV

C. EXTEST_PULSE – Driving Edges

Table 2 shows the captured boundary scan cell data while driving the TX+/- nodes with differential and single-ended edges during EXTEST_PULSE. The test receivers detect each driven edge correctly.

Table 2 EXTEST_PULSE Results across PVT

Driving TX+ TX- transitions	On-board AC coupled captured data RX+ RX-	On-chip AC coupled captured data RX+ RX -
a. 00 to 11	11	11
b. 01 to 10	10	10
c. 10 to 01	01	01
d. 11 to 00	00	00

Figure 4 shows the RX nodes' responses to the edges going across the on-board AC coupled capacitor during test b. in Table 2. The RX+ and RX- nodes received valid positive and negative pulses respectively. The pulses caused the DSR Flops to set or clear appropriately resulting in the correct boundary scan cell data.

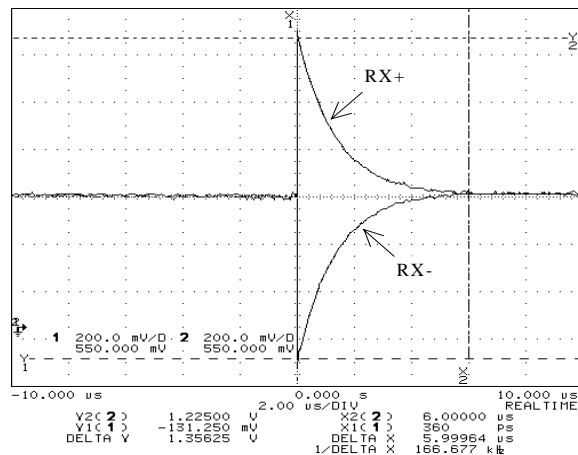


Figure 4: RX+/- for a Passing Edge

D. EXTEST_PULSE – Injecting Defects

The EXTEST_PULSE results with injected faults are shown in Table 3. The defect is listed in the first column, the failure syndromes for the on-board and on-chip coupling cap cases are shown in the next two columns, and the detection status for EXTEST and EXTEST_PULSE appears in the last column. All tests with shorts were performed twice: once with the TX attempting to drive the shorted TX leg, once with the TX disconnected prior to the short (no differences were seen). All tests with opens were performed without driving the open TX leg. Results for non-defective legs corresponded with those of Table 2 except where noted. Every fault in Table 3 was detected. Faults involving shorts across a capacitor (s. and t.) are not detected by EXTEST_PULSE, but are detected by EXTEST since DC shorts are induced. IEEE Std 1149.6 anticipated this result.

Tables 4 and 5 show more detailed results for tests e., i., n., and r. in Table 3. At least one of the four edge-detection tests performed must fail in order to consider the injected fault detected. The tests that identified faults are shown in bold. There was some degree of intermittency as to which test failed for these defects, depending on TX data, Init Value, and PVT conditions, but at least one test always identified the defect.

Figures 5-9 show the analog inputs to the test receivers for several of the injected defect test cases in Table 3. Each waveform was captured when differentially driving a 0-to-1 transition on the TX+/- nodes while injecting the specified defect.

Figures 5 and 6 show the relevant nodes for a TX-short to GND (see test g. in Table 3). For the on-board AC coupled pair, both RX legs received valid pulses that then decayed to V_{com} (nominally 0.6V) as shown in Figure 6. The pulses result in both RX boundary scan cell capturing the same data, which indicates the defect.

For the on-chip AC coupled pair, it was necessary to look at the TX nodes since the RX nodes were unobservable. Figure 5 shows that the TX+ node of the on-chip AC coupled pair received a driven edge while the TX- node was held to GND. Since these signals only pass through the AC coupled capacitors prior to becoming inputs to the test receivers, the RX+ node must have received a pulse while the RX- node did not. This logical deduction explains why the RX+ boundary scan cell captured an edge while the RX- boundary scan cell captured the Init Value (thus indicating the defect).

Figure 7 shows the RX+/- nodes with an RX-short to GND (see test p. in Table 3). The RX+ node observed a rising edge as expected. However, both nodes were subsequently pulled back down to GND, causing both test receivers to detect a logic level 0.

When the TX- node was left open (see test f. in Table 3), Figure 8 shows that both RX legs received the edge being driven onto the TX+ node. Thus, the captured data of the open leg followed that of the driven leg.

In the case of shorting the two TX nodes together (see test b. in Table 3), the RX legs received small pulses for the differentially driven edges, as shown in Figure 9. However, the test receivers rejected the pulses since the amplitudes were too small ($<V_{hyst}$).

Table 3 Test Receiver Injected Defects Results

Injected defect	EXTEST_PULSE On-board AC coupled results	EXTEST_PULSE On-chip AC coupled results	Detected? EXTEST/ EXTEST_PULSE
a. TX+ open	RX+ captures RX- value	RX+ captures RX- value	No / Yes
b. TX+ short to TX-	RX+/- capture V	RX+/- capture V	No / Yes
c. TX+ short to GND	RX+ captures RX- value	RX+ captures V	No / Yes
d. TX+ short to Vdd	RX+ captures RX- value	RX+ captures V	No / Yes
e. TX+ short to another TX+	see Table 4	see Table 4	No / Yes
f. TX- open	RX- captures RX+ value	RX- captures RX+ value	No / Yes
g. TX- short to GND	RX- captures RX+ value	RX- captures V	No / Yes
h. TX- short to Vdd	RX- captures RX+ value	RX- captures V	No / Yes
i. TX- short to another TX-	see Table 4	see Table 4	No / Yes
j. RX+ open	RX+ captures RX- value	can't inject	No / Yes
k. RX+ short to RX-	RX+/- capture V	can't inject	No / Yes
l. RX+ short to GND	RX+/- capture 0	can't inject	Yes / Yes
m. RX+ short to Vdd	RX+/- capture 1	can't inject	Yes / Yes
n. RX+ short to another RX+	see Table 5	can't inject	No / Yes
o. RX- open	RX- captures RX+ value	can't inject	No / Yes
p. RX- short to GND	RX+/- receive 0	can't inject	Yes / Yes
q. RX- short to Vdd	RX+/- receive 1	can't inject	Yes / Yes
r. RX- short to another RX-	see Table 5	can't inject	No / Yes
s. TX+ short to RX+	Detected by EXTEST only	can't inject	Yes / No
t. TX- short to RX-	Detected by EXTEST only	can't inject	Yes / No
u. TX+ short to RX-	RX+ captures RX- value	can't inject	Yes / Yes
v. TX- short to RX+	RX- captures RX+ value	can't inject	Yes / Yes

Table 4 EXTEST_PULSE Results for tests e. and i. in Table 3

TX1 +/- Transitions	TX2 +/- Transitions	e. TX+s shorted on-board AC coupled results RX1 RX2	e. TX+s shorted on-chip AC coupled results RX1 RX2	i. TX-s shorted on-board AC coupled results RX1 RX2	i. TX-s shorted on-chip AC coupled results RX1 RX2
a. 01 to 10	01 to 10	10 10	00 00	10 10	10 10
b. 10 to 01	10 to 01	01 01	11 11	01 01	01 01
c. 01 to 10	10 to 01	00 11	00 11	11 00	1V 00
d. 10 to 01	01 to 10	11 00	11 00	00 11	0V 11

Table 5 EXTEST_PULSE Results for tests n. and r. in Table 3

TX1 +/- Transitions	TX2 +/- Transitions	n. RX+s shorted on-board AC coupled results RX1 RX2	r. RX-s shorted on-board AC coupled results RX1 RX2
a. 01 to 10	01 to 10	10 10	10 10
b. 10 to 01	10 to 01	01 01	01 01
c. 01 to 10	10 to 01	V0 11	1V 0V
d. 10 to 01	01 to 10	V0 11	1V 0V

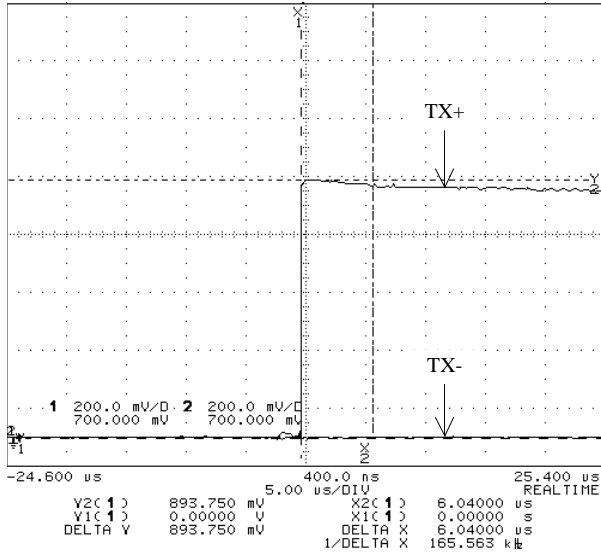


Figure 5: TX- Short to GND – on-chip AC coupled

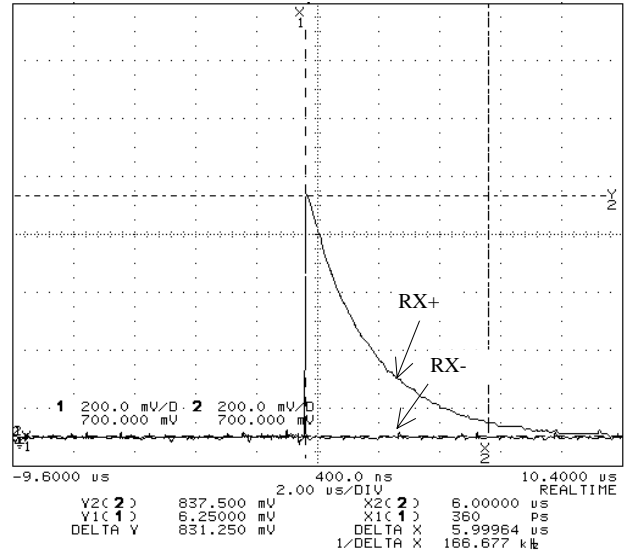


Figure 7: RX- Short to GND – on-board AC coupled

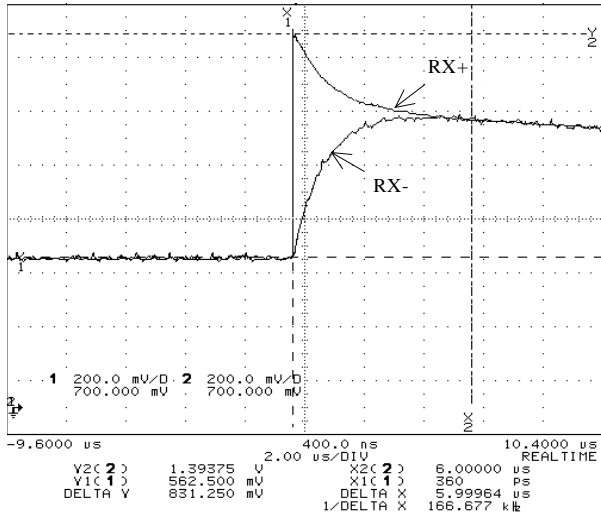


Figure 6: TX- Short to GND – on-board AC coupled

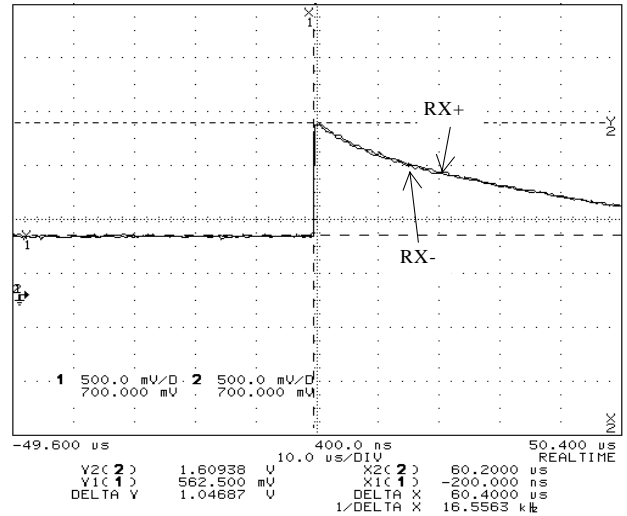


Figure 8: TX- Open – on-board AC coupled

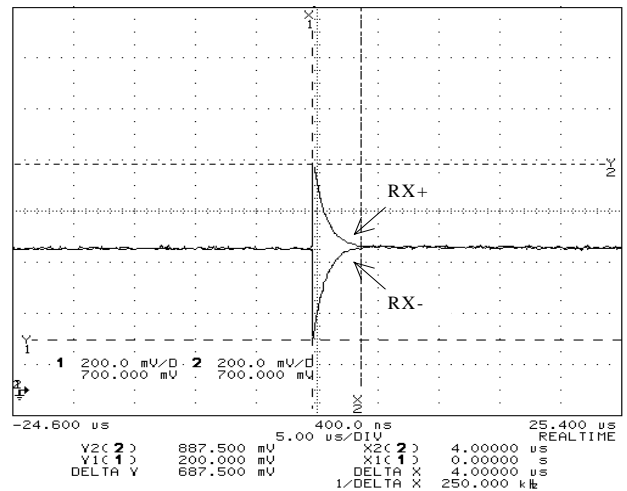


Figure 9: TX+ Short to TX- – on-board AC coupled

V. TEST RECEIVER CHARACTERISTICS

The test receiver's ability to correctly detect edges depended upon its ability to distinguish a valid signal from noise. To characterize this ability, 1) the amplitude (V_{hyst}) and transition (T_{hyst}) requirements of an input signal were measured and 2) noise was induced by heavily switching adjacent TX/RX pairs.

A. V_{hyst}

V_{hyst} was obtained by injecting differential edges into the TX side of an on-board AC coupled capacitor and reducing the amplitude of the edge until the test receiver failed to recognize the edge. Figure 10 shows the input signal on the RX side of an on-board AC coupled capacitor for the "just passing" negative edge of at nominal PVT. V_{hyst} was measured from V_{com} to the peak of the negative edge.

Figure 11 shows a graph of the PVT V_{hyst} results, which range from 265-334mV. V_{hyst} tends to increase with voltage and temperature: 15-35mV

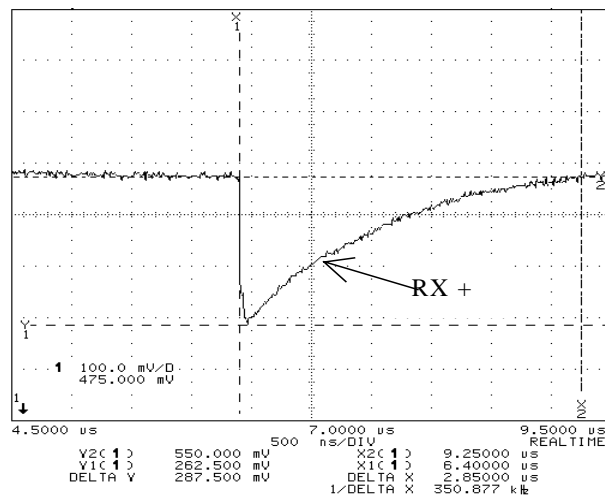


Figure 10: V_{hyst} - Detected Input Signal

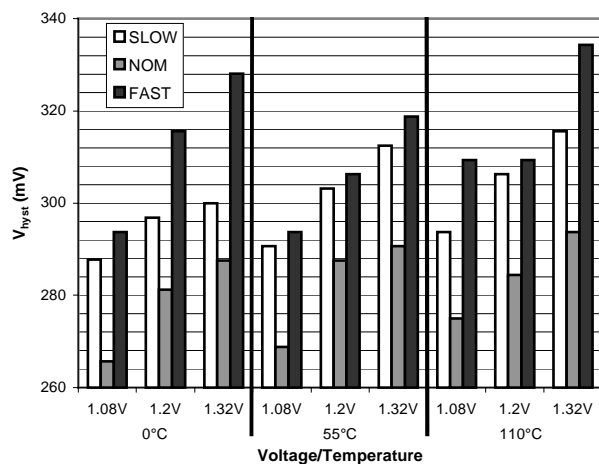


Figure 11: V_{hyst} - PVT data

increase from 1.08V to 1.32V, and 0-16mV increase from 0°C to 110°C. There was no obvious trend in V_{hyst} due to process.

B. T_{hyst}

T_{hyst} was determined by injecting differential 1V peak-peak pulses onto the TX side of an on-board AC coupled capacitor while decreasing the pulse width until the test receiver no longer received an edge. Figure 12 shows the "just passing" negative pulse. T_{hyst} was measured at the passing V_{hyst} for each PVT point.

The PVT results for T_{hyst} , which ranged from 1.14-2.22ns, are shown in Figure 13. Slight but not very distinctive increases due to voltage and temperature are seen in the graph. However, the T_{hyst} results are dependent on the V_{hyst} results shown in Figure 11. Thus, the slight trends are most likely due to the trends in V_{hyst} and not actual T_{hyst} trends.

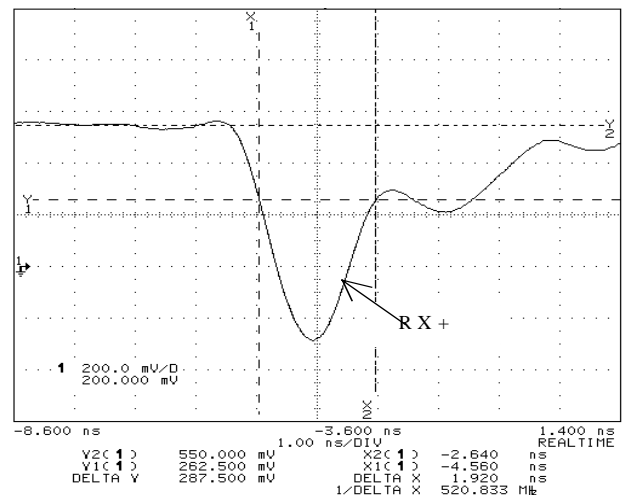


Figure 12: T_{hyst} - Detected Input Signal

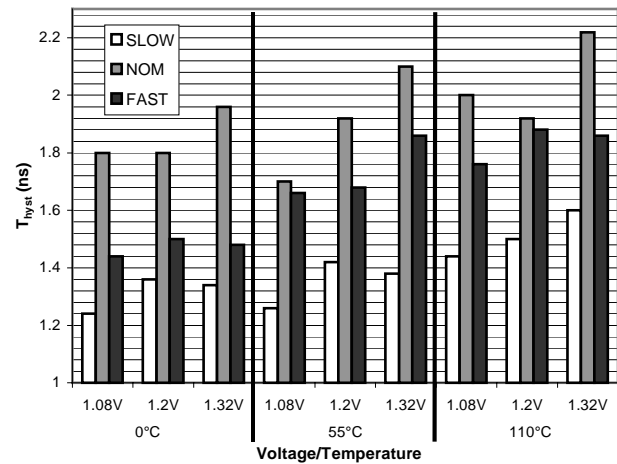


Figure 13: T_{hyst} - PVT data

C. EXTEST_PULSE – heavy switching

Table 6 shows the PVT results of switching eight adjacent TX/RX on-board AC coupled pairs simultaneously. The results show that the added noise did not degrade the test receiver’s ability to detect edges correctly.

Table 6 EXTEST_PULSE - Heavy Switching

Test	Reception Verified?
a) hold one signal static, the rest rising	CAN'T TEST *
b) hold one signal static, the rest falling	CAN'T TEST *
c) drive one rising edge, the rest falling	YES
d) drive one falling edge, the rest rising	YES
e) drive half signals falling, the half rising	YES
f) drive half signals rising, the half falling	YES
g) repeat e) and f) with a log-n checkerboard sequence	YES

* Note: All channels perform the same TAP command. It is not possible to perform EXTEST on some channels while performing EXTEST_PULSE on others; this IC had no “DC-only” I/O pins.

VI. DISCUSSION

The results of the EXTEST tests demonstrate the success of 1149.6’s compatibility with 1149.1. The test receiver correctly detects logic levels during EXTEST while DC coupled to the transmitter, a required behavior as set forth by 1149.1. While AC coupled to the transmitter, the test receiver does not detect levels, and thus captures the Init Value indicating an incorrect connection as far as EXTEST is concerned (and demonstrating one reason for the existence of 1149.6).

The results show that during EXTEST_PULSE tests, the test receiver accurately receives valid edges and detects all injected defects except shorted capacitors. 1149.6 anticipated that EXTEST would detect shorted capacitors, which was the case in this characterization. Thus, the fault detection results fulfill another goal of 1149.6, high fault coverage.

In the case of injected opens on either side of the capacitor, all tested pairs behaved the same. The edge on the driven leg was seen on both legs. This behavior can be explained by the RX termination. Regardless of whether the termination lies on the TX or RX side of the AC coupling capacitor, the driven signal bleeds through the termination to the open leg.

The high impedance nature of V_{com} does little to dampen the high frequency pulse. Thus, the open leg’s test receiver captures the same data as the driven leg.

The on-board and on-chip AC coupled pairs did not behave the same in the presence of injected shorts on the TX side of the capacitor. The on-board AC coupled pairs captured the same results for shorts as for opens. The on-chip AC coupled pairs, however, captured the Init Value on any leg that had an injected short on the TX side of the capacitor. The difference in behavior can be explained by the difference in RX termination placement. When the RX termination is on the RX side of the coupling capacitors, the driven edge bleeds to the shorted leg through the termination, causing both test receivers to detect edges. When the RX termination is on the TX side of the coupling capacitors, the driven edge cannot bleed across the termination since the short exists at the termination point, causing the shorted leg’s test receiver to detect no edges.

In the case of injected shorts on the RX side of the capacitor, the on-board AC coupled test receivers behaved as if receiving DC logic levels. Figure 7 shows a valid edge on the driven leg. The boundary scan cell does not, however, record the valid edge because the induced short pulls the driven leg to the shorted level. The high impedance nature of V_{com} does little to increase the voltage on either leg. The previously detected edge is overwritten in the DSR Flop by the quick return to the shorted level, causing the boundary scan cell to capture the shorted logic level.

Good noise rejection is another goal of 1149.6. The measured V_{hyst} and T_{hyst} values ranged 265-334mV and 1.14-2.22ns respectively. These values compare well with the simulated 307.5mV and 2.2ns at nominal PVT. Board effects, limitations of the test equipment, actual V_{bias} and V_{com} values on the die, T_{hyst} measurement technique, and differences between simulated pulses and actual injected pulses all contribute to differences between measured and simulated results. The measured V_{hyst} and T_{hyst} values indicate that the test receiver does a reasonable job of rejecting noise as designed.

The test board and IC design did not lend themselves well to more aggressive noise immunity testing. A few suggestions for future noise immunity testing include: 1) a test board designed to inject specific logic levels, edges, and types of noise and 2) the ability to switch adjacent pairs independently.

In conclusion, the results presented for the first IC implementation of 1149.6 provide proof of concept for the emerging standard. High fault coverage and backwards compatibility to 1149.1 as well as reasonable noise rejection demonstrate 1149.6’s

success. More comprehensive noise immunity testing is necessary to confirm the robustness of the standard with respect to noise.

ACKNOWLEDGMENTS

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