

# Design and Implementation of IEEE 1149.6

Ivan Duzevik, National Semiconductor, South Portland, Maine, USA

ivan.duzevik@nsc.com

## ***Abstract***

This paper describes the process of implementation of IEEE 1149.6 to an existing commercial high-speed interface device. The first part explains the circuit design decisions made during the definition phase. The insertion of the test circuitry had to be carefully implemented to co-exist with the mission mode circuitry. The second part describes the effect of the test circuit on the high-speed mission performance of the device and the trade-offs that those effects imposed. After the implementation phase, the test circuit was simulated, verified, manufactured in silicon and tested. The third part of the paper reports the findings after the verification of the functional performance of the IEEE 1149.6 device. An important part of the verification process was to determine the fault coverage of AC-coupled line tests. The specific behavior of the test circuit during detection of various faults directly governs the design of the IEEE 1149.6 TAP (Test Access Port) controller. The discussion at the end presents a summary of and comments on the results. In addition to the results of the 1149.6 implementation, a brief comparison between the features and characteristics of the 1149.4 and 1149.6 Standard is also presented.

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