

BUILDING AN RF SOURCE FOR LOW COST TESTERS USING AN ADPLL CONTROLLED BY TEXAS INSTRUMENTS DIGITAL SIGNAL PROCESSOR (DSP) TMS320C5402

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Abstract

In this paper, a new RF/Microwave source is presented. This source is able to generate a Continuous Waveform (CW) signal as well as a modulated signal like GFSK for Bluetooth and GMSK for GSM. The RF source presented here is based on a direct modulation All-Digital Phase-Locked-Loop (ADPLL) architecture that was originally designed for a Bluetooth transmitter in the 2.4GHz in industry, science, and medicine (ISM) band. By doing some modifications, we were able to extend the frequency range of the source. The ADPLL requires a controlled signal from a Digital Signal Processor (DSP). The TMS320C5402 DSP was chosen for this experiment.

1. Introduction

The increasing functional complexity of electronic components and systems has made Integrated Circuit (IC) testing very challenging, particularly under the constraints of high quality and low price. Indeed, the manufacturing cost per transistor follows Moore's Law; hence the cost per IC is reduced, even as functionality and performance increases. Test costs, however, don't scale with Moore's Law, therefore becoming a bigger factor in the total manufacturing cost of a chip.

Figure 1 shows that the average sales price of a cellular handset, which includes the IC, is dropping over time, forcing IC developers to try to minimize their test development costs, which have remained one of the most contributing parameters to the cost of IC manufacturing. In fact, the cost to test a transistor is projected to approach the fabrication cost of the transistor within a decade, due to the emergence of System-on-Chip (SOC) designs that integrate mixed signal and radio frequency (RF) design features in addition to higher pin count. In short the need of new test methodologies and test equipment has become very urgent.

Over the last decade Automatic Test Equipment (ATE) manufacturers have put lots of effort into providing equipment that addresses the different needs of the test community. While several technical issues of IC development were efficiently addressed by introducing RF and Microwave testers in addition to digital, analog and mixed signal capabilities, they still did not succeed in lowering the costs of these testers. ATE vendors argue that the quality over price ratio cannot be any lower because of the complexity of today IC's, and suggest that the test list be reduced to get test costs down.

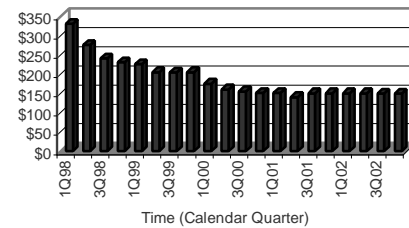


Figure 1: Average Handset Sales Price Vs Time

Another trend in the industry is the use of low cost testers by many semiconductor companies. In recent years, several IC manufacturers and ATE vendors have disclosed plans to use or develop low cost test equipment [1] [2]. However, this trend is in direct opposition with the need for speed when testing the new generations of IC's. Most of the low cost testers are very limited in their applications. While giving satisfaction for digital and low frequency analog circuits, they have not proven their capability in testing RF and Microwave devices. This is largely due to the required instrumentation. Several issues still require close attention from the RF & Microwave ATE designer: signal integrity, noise immunity, and the need to properly source and measure RF signals [3][5].

In this paper we present an RF source that is to be implemented on the Texas Instruments in house developed very low cost tester named "VLCT". Such an implementation will enhance its RF testing capabilities

while leaving the cost flat. This RF source is able to provide CW signals as well as Modulated signals. We will first discuss the general configuration of the RF tester and the importance of having an excellent RF source and then discuss our source in detail and present the data. The main focus of this paper will be the RF source, therefore we will not emphasize the tester description and other related issues.

2. RF Automatic Test Equipment (ATE)

ATE testers come in a variety of “flavors” from a variety of vendors. Unlike the personal computer (PC), testers are not all standardized in architecture. Every ATE vendor adds special features that he feels will give him a competitive advantage in the marketplace [4]. As a result testers from different vendors do not use a common software platform. A test routine implemented on one type of tester is often difficult to translate to another tester type because of subtle differences in hardware tradeoffs designed into each tester. Nevertheless most ATEs share many common characteristics. As shown on figure 2 a generic RF ATE will include system computers, RF sources, DC sources, DC meters, relay control lines, relay matrices, time measurement hardware and several other blocks that we will not be discussing in this paper.

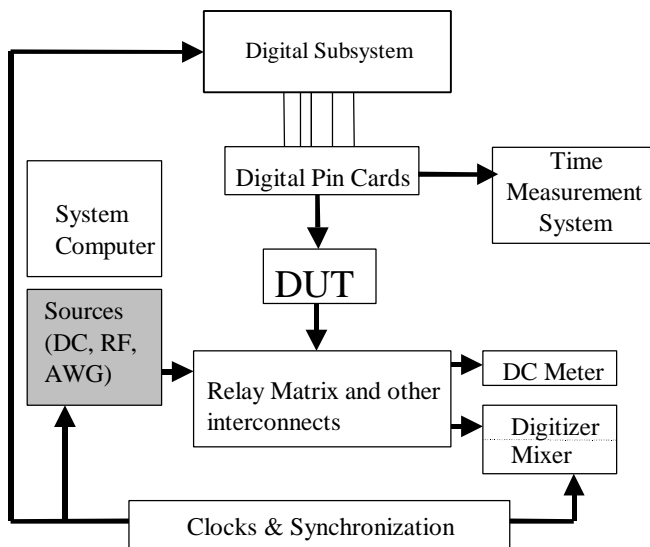


Figure 2: Configuration of a generic Mixed-Signal and RF Tester

In most RF ATEs a programmable RF source is used to provide the high frequency input needed by the DUT. Figure 3 represents the generation of the RF signal within the teradyne tester UW6000 which to some extent is similar to other ATE RF sources. The UW6000 is able to generate RF signals from 10MHz to 6000MHz. It

consists of a frequency synthesizer, a controller in the mainframe cabinet and a channel card in the test head. Using a 10 MHz crystal oscillator reference the synthesizer generates the waveform needed at a certain frequency with a fixed level. The output of the synthesizer is fed into a series of Multipliers and a multiplexer to provide the desired frequency. Then by performing a series of amplifications and attenuations within the channel card, the desired level is reached. The purpose of the quad synthesizer controller is to interface between the synthesizer and the test system for any programming of the synthesizer.

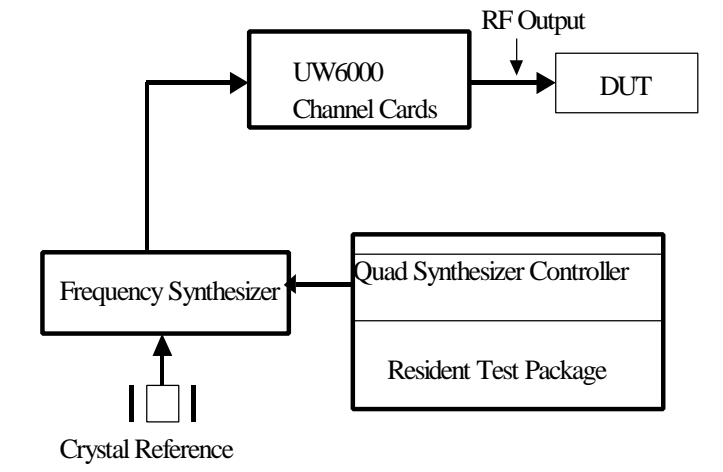


Figure 3: RF Signal generation within Teradyne Tester

3. The proposed RF Source for Low Cost Tester

Texas Instruments has developed a low cost tester, which is optimized for use with scannable and BISTed (Built-In-Self-Test) designs. This tester, while capable of handling most digital devices, is still very limited in its mixed signal and RF capabilities. One way of increasing its efficiency is to add additional instruments that will allow testing of RF devices. For that purpose a low cost RF source is being implemented. The proposed high frequency source can be divided into four major block functions as shown on figure 4:

- A control block whose main component is a DSP unit. The control block contains a ADPLL control unit (PCU) and a switch control Unit (SCU).
- A Signal Generation block represented by the ADPLL bank;
- The filtering and amplification block;

- A power level adjustment block;

The operation mode of this source is described as follows:

The user defines the desired output frequency and Power. Once the desired output frequency is known, the DSP, through the PCU and SCU, activates the switches to establish the chain from the synthesizer up to the output, while ensuring that switches in the unused chain are left open. Once the chain is established, the DSP, through its PCU will start sending the proper commands to the appropriate ADPLL, locking it at the desired frequency. The desired frequency is subsequently filtered and amplified to reach the maximum output power. It is filtered a second time to eliminate any nonlinearity that might have been introduced during the amplification. At the last stage, the signal is attenuated to the desired output power.

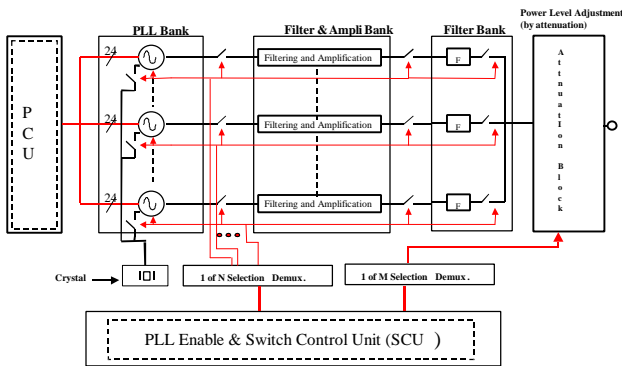


Figure 4: Proposed Configuration of the RF Source

3.1 Control Block

The control is performed by a TI DSP called the TMS320C5402 (C5402) DSP. It is an inexpensive fixed-point DSP with 16K word on-chip memory and has various on-chip peripherals. These peripherals include two multichannel buffered serial ports (McBSP's), an enhanced 8-bit parallel host port, two 16-bit timers and a six-channel direct memory access (DMA) controller. The C5402 is the industry's most powerful DSP that is specifically optimized for applications that need the best power/performance/area. It performs up to 100 million instructions per second (MIPS) at 60 mW. The control block is comprised of 2 subblocks: a PCU (ADPLL Controlled Unit) that will help select a ADPLL depending on the desired output frequency and a SCU (Switch Controlled Unit) that controls all the switches within the RF source, depending on the desired output frequency and power level.

3.2 RF Signal Generation

The signal generation block or ADPLL bank contains a certain number of ADPLLs. Each ADPLL is individually working in a specific frequency range. The ADPLL bank could be replaced by a single ADPLL if the RF source is aimed at testing a specific band. For example an ADPLL working in the 2.4 – 2.5 GHz band would be enough if the source is dedicated to testing Bluetooth or 802.11b devices only. The output frequency range of the ADPLL is fixed to 150MHz in our case. This value depends on the ADPLL design. Theoretically we can have N number of ADPLLs. The more ADPLLs we have the wider the frequency bandwidth of the RF source.

The signal generation itself is based on the use of a direct modulation All-Digital (ADPLL) configuration already experimented in the Island Project Transmitter as the RF frequency source. The ADPLL with a Digitally Controlled Oscillator (DCO) at 2.4 GHz as the RF frequency source is the cornerstone of this solution. The frequency setting is done through the fixed-point Frequency Command Word (FCW), which is the normalized frequency to the reference FREF provided by a high performance external crystal oscillator. In another view, the LSB bit of the integer part of the FCW corresponds to the 13 MHz FREF frequency coming from the external crystal.

The proposed RF source can be used as modulated source, provided a proper programming of the DSP. For example to generate GFSK modulation scheme, the modulation is done using a two-point modulation scheme to create the GFSK modulated transmit digital signal. The input NRZ data is oversampled and then passed through a digital Gaussian shaping filter DTX. The shaped data is then fed to two points of the PLL. One point is added to the FCW channel select word to realize the desired frequency deviation. The other is fed-forward directly to the oscillator through the loop filter.

3.3 Filtering and Amplification

The purpose of this block is to provide filtering and amplification of the ADPLL output signal. Two main parameters that are affected by this block are the phase noise and the maximum output power of the source. This block contains different band pass Filter cells and amplifiers. The band pass filters are used to cut all the undesired frequencies and also to reduce the far end phase noise to the thermal noise floor level or the system noise floor. Concerning the close in phase noise it depends on the design of the ADPLL. Figure 5 illustrates the phase noise of the source before the filtering and after the filtering. As one can notice the far end phase noise

presents some improvement. The choice of the band pass filters is very critical for the phase noise performance of this RF source. It requires specific characteristics (Sharp cut-off frequency and flat gain within the desired bandwidth).

After the pass band filter, a serie of amplification is performed to reach the maximum output power possible. These amplifiers are LNAs (low noise amplifier) used in their very linear region, in order to ensure the strict linearity during the amplification. One extra precaution to ensure linearity during the amplification is to use a balanced configuration[8], as illustrated by figure 6. The signal at the output of the band pass filter is divided in two similar pathes that include several amplifier cells with small gain. The use of small gain is will make the amplifiers operate in their linear area. Once the amplication is performed the signals are recombined in quadrature to reach the maximum output power. An additional pass band filtering is then performed again to ensure that no harmonic have been introduced during the amplification. Figure 7 shows the measured output signal after filtering and amplification using 9dB attenuation at the output. It can be noticed that a maximum of output power of 28dBm is achievable with this source.

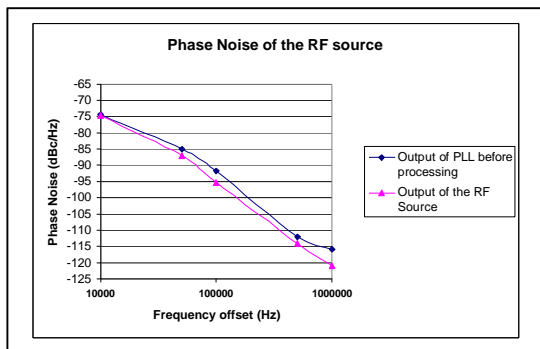


Figure 5: Measured phase noise of the RF source before and after processing

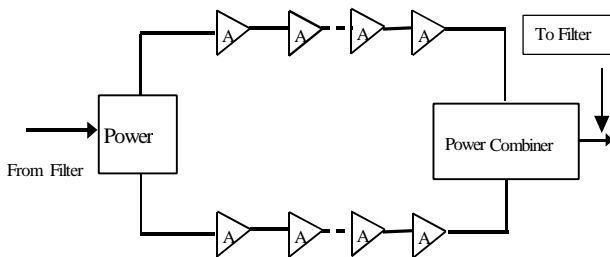


Figure 6: Amplification Stage using a balanced configuration

3.4 Power Level Adjustment (PLA)

The last block of this RF/Microwave is the Power Level Adjustment block. The purpose of the PLA is to perform the required attenuation in order to deliver the desired output power level. Figure 8 shows how that goal is achieved by using an attenuator bank. The attenuators present different attenuation level and are activated by the DSP through SCU depending on the output level requested by the user within the source program. Figure 7 shows the output power requested of 19dBm which means an required attenuation at the PLA of 9dB for a 28dBm maximum output power.

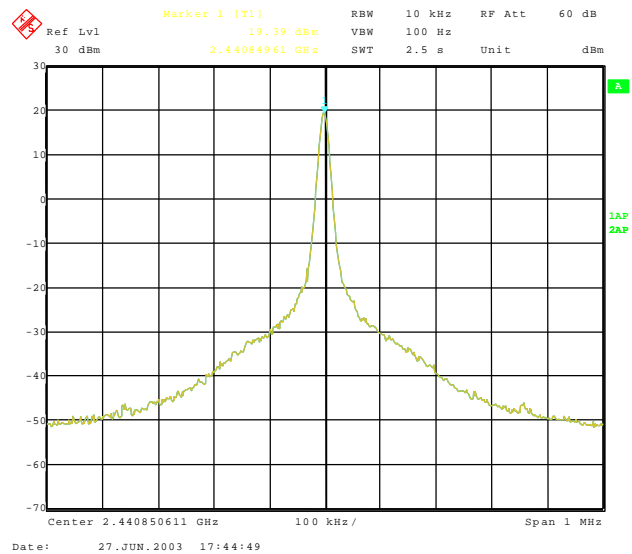


Figure 7: Measured output of the RF source after amplification and Filtering, using 9dB attenuation.

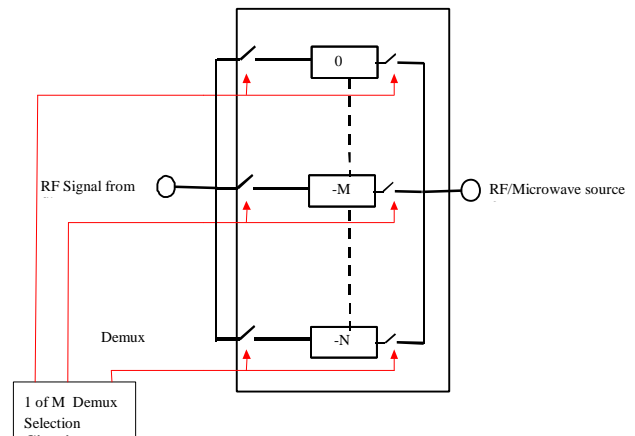


Figure 8: Power Level Adjustment (PLA) block

4. Experimental results and Discussion

The experimental results obtained show that the concept is very interesting while very easy to implement. Figure 5 and 7 shows respectively a very interesting phase noise and output power obtained from the RF source. We proved that the RF source is able to provide beside cw signals, some RF type of modulated signals. Figure 9, 10 and 11 show respectively a cw signal, a GMSK modulated signal and a bluetooth signal obtained from the RF source.

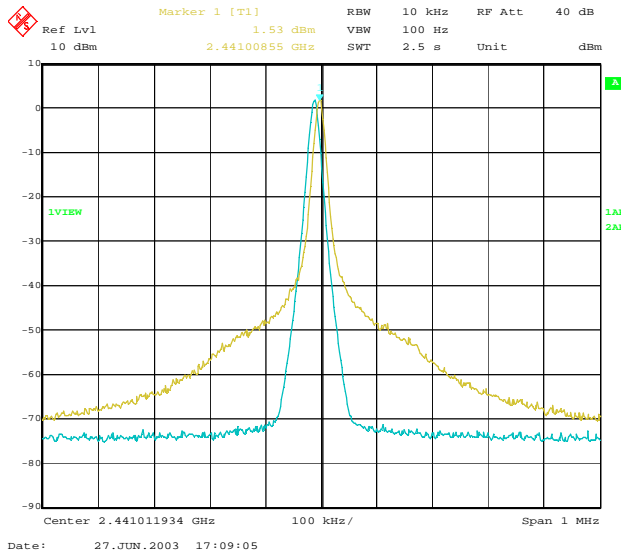


Figure 9: CW signal of the RF/Microwave source compared to the cw signal of an Rhode and Schwartz signal generator.

The analysis of the experimental result present the phase noise as the fundamental challenge that can limit the use of this RF/Microwave source for high end type of devices. The comparison with the Rhodes & Schwartz shows that for phase noise obtained from our proposed source , the far end is high compared to the one obtained from the Rhode & Schwartz. Therefore effort needs to be put on the type of filter used. As stated earlier, the performance of the filter is very critical to reduce the phase noise. Meanwhile an investigation of the ADPLL design could help in improving the phase noise.

Another critical issue that will be the focus of future works is the calibration of the source.

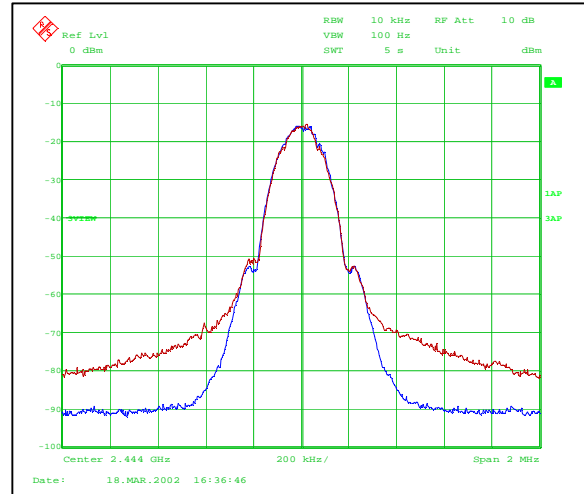


Figure 10: GMSK modulated signal from the RF/Microwave source compared to the GMSK modulated signal of an Rhode and Schwartz signal generator.

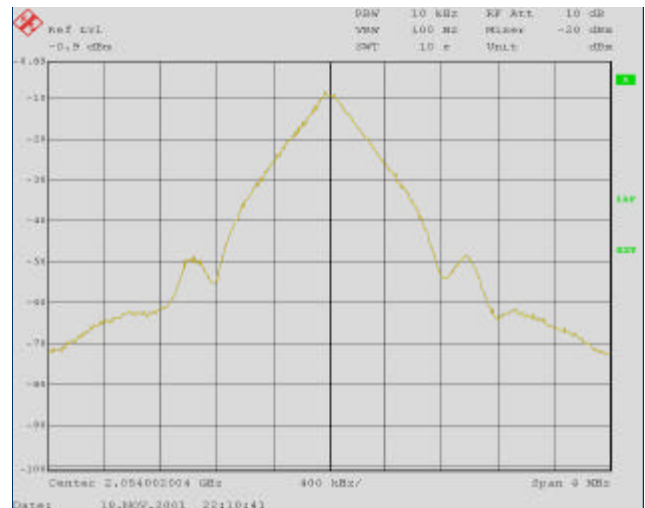


Figure 11: Bluetooth modulated signal from the RF/Microwave source.

5. Conclusion

All along this paper we presented a configuration of a RF/Microwave source that can be used in low cost tester. The Source presented in this paper is based on the use of ADPLL along with a DSP to control it. The experimental results obtained show that the source is actually very practical for low end type of device and can be used to test high type of device provide certain improvement that have been underlined. Future works

will be focus in those improvements as well as the definition of the calibration technique for the RF source.

6. Acknowledgements

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7. References

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