

# Effectiveness Improvement of ECR Tests

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## Abstract

*Energy Consumption Ratio (ECR) test, a current-based test, has shown its ability to reduce the impact of process variations and detect hard-to-detect faults. The effectiveness of ECR tests may be degraded by a large number of normal transitions in a circuit, which may bury the fault impact on the overall current. For deterministic ECRs, the fault-oriented ECR tests are generated with an algorithm to minimize the number of normal transitions not related with the sensitizable path of the target faults. For generalized ECRs, however, the test patterns are generic without targeting any specific faults and therefore may cause a significant amount of transient activities in a CUT. This issue is addressed in this paper by utilizing a DFT technique, multiple scan chain design. This technique virtually partitions the circuit into several sections, so that the transitions in each section can be much less compared with those in the whole circuit. The fault impact can be more significant with fewer transitions in the circuit, which hence increases the ECR test effectiveness. The anti-process-variation property of the ECR metric is also demonstrated through a negligible lot-to-lot shift. Finally, the effectiveness of ECR tests with different thresholds is compared with existing traditional tests.*

## 1 Introduction

Extremely high quality IC products are demanded for implantable biomedical devices. Almost all known traditional test methods in the industry are applied in the process of testing these ICs. However, traditional test methods may not provide sufficient fault coverage for high quality ICs. For example, regions with missing materials may cause resistive contacts, vias, and resistive opens. These defects may not cause logic failures and cannot be modeled well for traditional tests [1]. Many test methods have been proposed to provide additional fault coverage beyond that of traditional tests. Very-Low-Voltage (VLV) test is applied at a much lower voltage than the normal opera-

tion voltage and has been shown to be able to detect defects that escape tests applied at normal voltages [2][3][4]. Minimum-Voltage (MinVdd) test is recently recommended to detect the defects similar to that identified by VLV tests by searching for the minimal operation voltage of a chip and then comparing it against the characterized threshold [5]. In contrast to those new voltage-based tests, current-based tests that measure power supply transients of circuits have been researched for providing additional coverage. Recent methods include current waveform analysis [6], frequency domain analysis of the current [7], individual current pulse comparison [8], transient current measurement and charge calculation [9], and the Energy Consumption Ratio (ECR), which uses ratios of component dynamic currents [10]-[16]. The ECR has been shown to be tolerant of process variations, which dramatically limit most other current-based test methods. It has been shown that the ECR test can detect faults that may escape traditional tests, such as redundant faults, bridging faults, and open faults [13]. Practical data have verified that the ECR technique can provide additional coverage to our existing tests [15].

However, the effectiveness of ECR tests may be degraded by a large number of normal transitions in a circuit, because a fault impact on the energy consumed by a faulty circuit may be masked by the normal non-faulty activities. This will make it difficult for ECR tests to distinguish the faulty circuit from the good ones. This limitation is not an issue for deterministic ECRs, which are fault-oriented utilizing patterns generated with an algorithm to minimize the number of normal transitions not related with the sensitizable path of the target faults. Therefore, the fault effect is usually significant enough to be captured by the corresponding ECR. However, the test patterns created for generalized ECRs are simply some generic vector sequences that do not target any specific faults and therefore may cause a significant amount of transient activities in a circuit. The reality is such that there is a stronger motivation to adopt the generalized ECRs due to their simplicity and ease of implementation. In this paper, we will address the transition issue for generic ECRs by utilizing a virtual circuit partition tech-

nique, multiple scan chain design. The concept is based on the fact that multiple scan chain design virtually partitions the circuit into several chain-based blocks. If only one pattern is shifted through a chain at a certain period of time while all other chains are kept quiet, the number of transitions caused by the active chain can be greatly reduced compared to activation of the whole circuit. The fault impact may be more significant with fewer transitions in the circuit, which hence increases the ECR test effectiveness. We will also demonstrate the process variation immune feature of the ECR by investigating the lot-to-lot ECR shift against dynamic current shift. To further investigate the effectiveness of ECR tests, different test thresholds are characterized to form different set of ECR tests. We then compare the effectiveness of these ECR tests based on different thresholds with those of major traditional tests. All the tests are applied to a biomedical IC product with the multiple scan chain DFT feature.

The remainder of this paper is organized as follows. A brief review of ECR concept and a discussion of ECR issues and solutions are presented in Section 2. Test methods and experimental process are described in Section 3. Test results and various comparisons among different types of ECR tests as well as between ECR and traditional test methods are discussed in Section 4. Section 5 concludes this paper.

## 2 Practical ECR Test and Issues

In this section, we briefly review some key points of ECR test related with its application in this paper.

The dynamic energy consumption of a circuit can be monitored to detect the presence of faults. The Energy Consumption Ratio (ECR) has been validated through extensive simulation [10] and through IC applications [12]. Consider a stuck-at fault in a circuit that affects steady-state internal signal values. The fault also alters the way internal signals transition in response to inputs in that it changes the number and location of signal transitions that occur. This causes the energy consumed by the circuit to decrease or increase. Due to process variations, the power dissipated for a certain amount of transitions may be different from the expected value. Using the ECR may reduce the impact of process variations.

Given two pairs of transitions  $P_1$  and  $P_2$ , let  $I_{P_1}$  ( $I_{P_2}$ ) be the average currents when the vectors in  $P_1$  ( $P_2$ ) are alternated at the inputs. The Energy Consumption Ratio is the ratio of the currents (or energies)  $\frac{I_{P_1}}{I_{P_2}}$  consumed on each of the two transitions.

The primary source of dynamic energy consumption is load capacitances. The average current is proportional to the number of signal transitions and load capacitances. Due to process variations, assume that the unit capacitance is al-

tered by a factor of  $k_1$  from its nominal value across the IC. The average current on a single transition is altered by this variation. However, because the variations in the numerator and denominator cancel each other, the ECR is immune to process variations of the first order. It has been shown that *the ECR reduces the impact of process variations without reducing the impact of the fault*. The ECR is able to detect redundant and hard-to-detect faults. Defects, such as opens, can be detected with the ECR test. Relative to other dynamic  $I_{dd}$  test methods, the ECR offers significant measurement advantages. Detailed ECR concepts and test results can be found in [10][12][13].

### 2.1 Issues and Solutions

Note that the greater the number of transitions that are common to the good and faulty circuits the lower the relative impact of the fault on the energy consumption. In the fault-oriented approach, a fault is targeted and the ECR test generation algorithm minimizes the transitions that are common to the good and faulty circuits. The algorithm attempts to maximize the percentage transition difference between fault-free and faulty circuit for the test pair.

The most significant practical limitation of ECR test is the increase in test generation and application time against traditional ATPG test. An ECR test involves the application of two pairs of transitions, with each applied several times. This leads to a significant test time per fault. Since ECR test detects faults not detected by other techniques, such test times may be appropriate for applications which demand very high reliability levels such as ICs for biomedical applications. On the other hand, one may use the concept of generalizing the ECR [12] to save test time. Basically, a generalized ECR test will consist of any two test vector sequences. In other words, one does not specifically generate tests to target the faults in the circuit to maximize the effectiveness of the ECR. A generalized ECR is still more tolerant to process variations than its component currents [15][16]. A generalized ECR is fault-independent, and thus reduces dramatically both test generation and application time. However, a fault-independent ECR may not reduce the number of signal transitions that are common to the good and faulty circuits. Therefore, the effectiveness of a generalized ECR may be lowered by a large number transitions caused by the general vector sequences, especially for large circuits. Generally, the larger the circuit is, the more transitions it may have, and the lower relative fault impact on the dynamic current. In order to make generalized ECR tests applicable to larger circuits, this issue has to be addressed.

One solution to reduce the overall transitions is circuit partition. Instead of consuming the power through one supply, circuit partition technique can divide the total cir-

cuit power onto multiple power supplies. A fault impact may now have a greater chance to be observed on at least one of those power supplies. IDDQ measured at multiple power pins has been proposed as a means of localizing defects [18]. However, adding more power supplies is simply not the preferred method for our strictly controlled low-power biomedical ICs. Another solution is to take the advantage of “virtual circuit partition”. A virtually partitioned circuit still has one power supply, but with the capability to access certain blocks of a circuit at a time. The blocks can be functional or non-functional. An example of non-functional blocks is a multiple scan chain design with individually controllable chains.

In this paper, we take the non-invasive approach, the virtual circuit partition method, by utilizing the multiple scan chain design technique. Specifically, we have implemented multiple-scan-chain test methods on our new products to save test time consumed by ATPG-based tests, such as stuck-at, transition delay, and IDDQ tests. This DFT feature provides a great opportunity to enhance the effectiveness of generalized ECR tests. We may just shift-in a scan pattern through one scan chain at a time and keep the rest of the scan chains constant at the same time. In this way, we can measure the dynamic current consumed only by the portion affected by that scan chain. In general, the dynamic current consists of two components, the current from pattern shift and the current from clocks. Because of its transition activities during the shift of any scan chain, the clocking current will dilute the effectiveness of ECR test, except for defective clock trees. Ideally, for a better ECR performance, the clocking current should be isolated from the shifting current. In reality, however, it is not easy to have a clean separation between the two components. One could estimate the clocking current by shifting all 1’s or 0’s through the scan chains, and subtract this estimated component later from the total current measured while shifting the real pattern. However, preliminary results show that the error introduced by this subtraction process decreases the ECR effectiveness also. Hence, the dynamic currents used in this experiment will be the total currents including the clocking components. Scan patterns are chosen as the vector sequences for generalized ECRs, because they are simple to generate and implement. With a sufficient number of scan chains, we would expect the ECRs based on the currents from individual scan chains (portions of the circuit) are more effective than those based on the currents from all scan chains (the circuit). Due to the generality of scan patterns, all of them may not produce effective ECRs. We will also compare the effectiveness among different scan patterns over multiple scan chains.

Note that virtual partition may involve switching in different partitions due to primary input switching. For our design, the primary inputs are associated with the bound-

ary scan chain and this chain is a part of the internal scan chains. Therefore, no primary input switching is necessary to exercise the logic and each virtual partition involves only the switching caused by the shift of the pattern through the subject chain. For other designs, especially for designs with more combinational logic than flops, virtual circuit partition based on functional blocks may be considered together with the partition based on non-functional blocks such as scan chains. Switching certain primary inputs may exercise certain functional block and therefore reduce the transition activities involved with a test.

### 3 Experimental Methods

In this section, we first describe briefly the circuit under test and various test methods applied to the circuit, and then set up the experimental process for collecting various ECRs and comparing their performances against each other and versus major traditional tests.

#### 3.1 Circuit and Tests

The circuit used for this experiment is a low-power biomedical IC, which consists of a microprocessor, core logic, TAP controller, test controller, multiple on chip memories, and peripheral. The circuit contains approximately 125K gates, not including the memory. The nominal supply voltage is 1.3 volts. The feature size of the device is 0.5  $\mu\text{m}$ . The circuit is implemented with 8 scan chains. Thirty three wafers from five lots were tested. Each wafer contains 229 die and the total number of die tested is 7557.

Because the circuit is designed for an implantable medical device, a very high level of test coverage is desired. Various test methods are applied to ensure high quality devices. Some major traditional tests implemented before the burn-in process are briefly described as follows. Continuity tests verify continuity between tester and pads of the device. Static current tests check the steady state of the circuit. Dynamic current tests monitor the dynamic operation of the circuit. Both tests monitor the power supplies of the digital logic and oscillators. Functional tests examine portions of the digital logic run at speed to provide additional fault coverage. Stuck-at and transition delay tests target the stuck-at and transition delay faults of the core logic. IDDQ tests check the quiescent current of the core logic. Memory tests target two 16K-by-8 RAMs, one 32K-by-8 RAMs, and five 16K-by-8 ROMs. No other tests target the memory logic and no IDDQ is measured during memory tests.

It can be expected that some hard-to-model defects may not be detected with this existing test suite. The high quality requirements of implantable devices lead us to investigate additional test methods, such as ECR tests.

## 3.2 Experiment Setup

Recall that an ECR test is based on two current measurements from two vector sequences. In addition to the traditional/functional dynamic current, the scan currents used in this experimental process are obtained by applying five scan patterns to the multiple scan chain circuit in various ways. The ECR is applied to the test process as follows:

- Generate five scan patterns (vector sequences) that will be shifted through the scan chains of the design. Pattern 1 consists of repeated pattern “010”, and pattern 2 “01100”. Pattern 3 is a pseudo-random pattern based on a 4-bit register with a generation function  $f(x) = x^4 + x^1 + 1$ . Patterns 4 and 5 are random patterns with 10% and 70% of 1’s, respectively.

Recall that we choose generalized ECRs rather than deterministic ECRs to save test time, with the sacrifice of fault coverage, and we choose scan patterns for the generalized ECRs because of their simplicity to generate and implement. Refer to [15] for details about the selection of scan patterns.

- Set up the test condition for scan dynamic current measurements. The power supply is set to 1.3 volts, and the circuit is set to operate with a period of 500 ns for five scan patterns.
- Apply the five patterns discussed above in various ways and measure the corresponding dynamic currents. Assume a product has both multiple scan chain design and single scan chain design. Thus, shifting all the chains of the multiple scan chain design at the same time would be equivalent to shifting the only chain of the single scan chain design of the same product. In order to quantize the improvement of ECR effectiveness of multiple scan chain design over single chain design, we will mimic the single chain design by shifting a pattern through all eight chains of this multiple scan chain design together at the same time. For convenience, results associated with these simultaneously activated chains will be marked with “ssc”, representing the equivalent Single Scan Chain design. We then shift the same pattern through each of the eight chains, one at a time, and measure the dynamic current. Results associated with individually activated chains will be marked with “msc” or chain IDs, representing the Multiple Scan Chain design. For five patterns, a total of 45 currents will be collected. Table 1 shows the current names related with patterns and chains for an easy understanding of the full picture of available currents used as components of various groups of ECR tests.

- Define the ECRs as a ratio between two specified currents measured. In order to compare the ECR performance between ssc and msc designs, for each current group described above, ECRs are defined into two groups. The first group is based on the currents from “Chain ssc” over five patterns. There will be 10 ECRs from 5 currents listed in the second row of Table 1. The ECRs obtained from this approach are grouped as ECR<sub>ssc</sub>, which represents the ECRs based on the single scan chain design. The second group is based on the currents from each chain over five patterns. For example, chain 1 (third row) will give us 10 ECRs over 5 patterns. We will get a total of 80 ECRs from 8 chains. This group represents the ECRs based on each individual portion of the circuit and is called ECR<sub>msc</sub>. To compare the ECR effectiveness between different patterns, ECRs are also calculated based on the currents from each pattern over eight individual chains, and then grouped for that pattern. This will give us 28 ECRs for each pattern and a total of 140 ECRs for 5 patterns, with the groups named as ECR<sub>pat1</sub> through ECR<sub>pat5</sub>. Note that any ECR is simply a calculation based on two measured currents and itself does not require extra measurements. The cost of ECR tests mainly depends on the number of currents to be measured, since the calculation time of ECRs is negligible compared to the measurement time. The ECR groups are also listed in Table 1 associated with the corresponding current groups. The rest of ECRs are calculated between each scan current and the functional dynamic current, and results will be lumped into the final all ECR group comparing against major traditional tests.
- Apply all the original existing tests in the test set to each die to collect the pass or fail status for each test.
- The quality of a die is defined by the existing original tests. A defective die fails at least one of the original tests. A good die passes all the original tests.
- All the ECR tests are then applied to each die. A pass range is set for each ECR test, so that a die passes an ECR test if its computed ECRs fall within the pass range, else it fails that ECR test.

One approach to set the test threshold for an ECR is characterizing the statistical distribution of the ECR. Outliers from the good die may be identified using this approach. ECR tests implemented in this approach can be considered to be aggressive tests. We will use the  $\pm n\sigma$  ( $n=4, 5, 6$ ) values of each ECR as the test threshold for that ECR in this experiment. The corresponding ECR tests will be called ECR <sub>$n\sigma$</sub>  tests in the following context. Another approach is to use an ECR’s minimum and maximum values over the

**Table 1. Current Associations and ECR Groups**

Chains	Pat 1	Pat 2	Pat 3	Pat 4	Pat 5	ECR Group
Chain ssc	I1ssc	I2ssc	I3ssc	I4ssc	I5ssc	ECRssc
Chain 1	I11	I21	I31	I41	I51	ECRmsc
Chain 2	I12	I22	I32	I42	I52	
Chain 3	I13	I23	I33	I43	I53	
Chain 4	I14	I24	I34	I44	I54	
Chain 5	I15	I25	I35	I45	I55	
Chain 6	I16	I26	I36	I46	I56	
Chain 7	I17	I27	I37	I47	I57	
Chain 8	I18	I28	I38	I48	I58	
ECR Group	ECRpat1	ECRpat2	ECRpat3	ECRpat4	ECRpat5	–

good die directly as the test threshold, which means all the good die identified by existing traditional tests will be guaranteed to pass the ECR test. ECR tests implemented in this approach can be considered to be conservative tests, since it is not intended to exclude any outliers, or in other words, declare any new failures. ECRmm will be used to represent the ECR tests using the minimum to maximum range as their limits.

Note that all tests except continuity are applied to each IC in a continue-on-fail mode. Continuity tests are always applied first on a stop-on-first-fail mode to ensure the tests followed are conducted without connection problems between the tester and the device under tests. Thus, the devices that fail continuity tests will be excluded from the test performance evaluation process in this experiment, since no other tests are applied to these devices. The above procedure is applied to all 7557 ICs over 5 lots. Out of the 7557 ICs, 1175 are continuity failures, 1743 are defective detected by the rest of original tests, and 4639 are identified as good die by all the original tests. All ECR test thresholds are characterized based on these good die. We will analyze the performances of ECR tests versus other major tests in the next section.

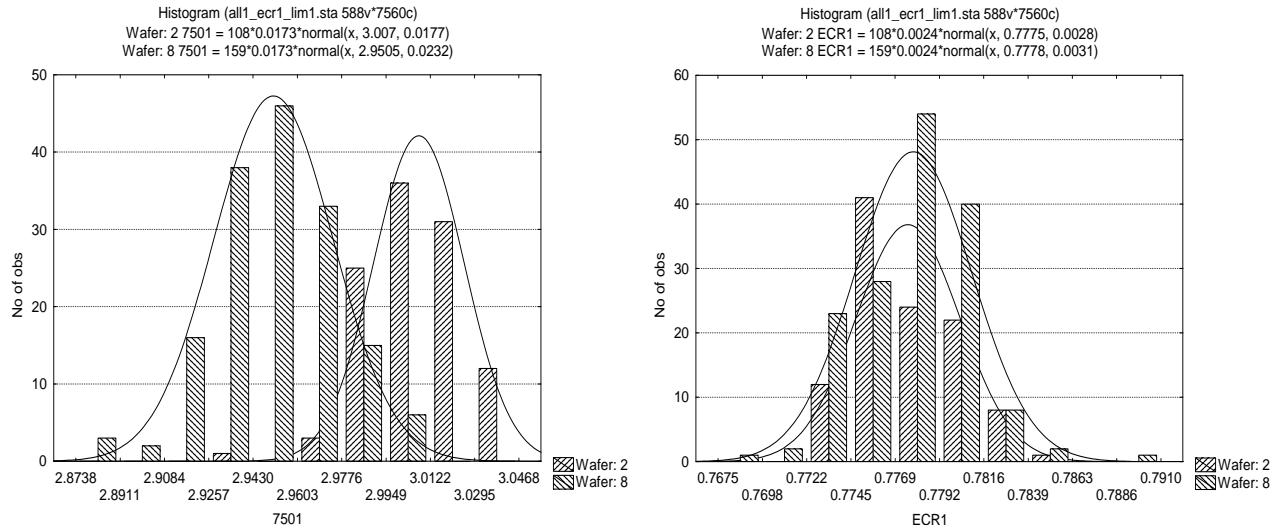
## 4 Results and Comparisons

We analyze and compare the results obtained from the above experiments. Since this is the first time for us to present ECR results from multiple wafer lots, we would like to examine the distributions of ECRs against those of dynamic currents to verify that the ECRs can provide the capability to reduce process variations over the dynamic currents across different lots.

### 4.1 Distributions of Currents and ECRs

It has been shown that the variation in the ECRs is much less than that in the current measurements [12][16]. However, the variations presented before were based on only one manufacturing lot because of limited wafers. For this investigation, we have collected five lots of wafer results. Now we can picture the lot-to-lot as well as wafer-to-wafer variations for currents and ECRs. The results are collected on the good die only for this purpose.

Figure 1 shows the distributions for one dynamic current (in mA's) and its associated ECR from two wafers of the same lot, respectively. Note this lot has four wafers, however, to show a clean figure, we do not plot all of them. Only the two wafers that show the greatest difference on their current distributions are plotted. Obviously, there exists a significant shift of the dynamic current and two well overlapped distributions of the ECR between the two wafers. In order to characterize the total variation for a subject with several distribution clusters, we will distinguish the variation based on one cluster distribution from the variation caused by the shift between clusters. In the following context, a cluster may consist of a set of data either from one wafer or from one lot. For a cluster distribution, the variation is defined as the ratio of the difference either between the minimum and mean values or between the maximum and mean values, whichever is larger, to the mean value. Thus, the variation of a cluster is the maximum variation. Between any two cluster distributions, the shift is defined as the ratio of the difference between the two mean values of the two clusters to the average of the two mean values. Thus, the total variation of a subject over two clusters can be simplified as the summation of the variation of a cluster and half of the shift between the clusters. In this way, the contribution of the shift to the overall variation can be easily characterized. Using Figure 1 as an example, the cluster (wafer) variation is 2.60%, the shift between the clusters



**Figure 1. Distributions of (a) dynamic currents (b) ECRs from 2 wafers of the same lot**

is 1.90%, and the total variations over the two clusters is 3.55%. To verify the accuracy of the total variation, we mixed the above two wafer results into one cluster and then calculate the overall variation. The result is 3.56%, which is very close to that based on the above two clusters. Similarly, we can calculate the variations for the associated ECR. The results are listed in Table 2.

**Table 2. Wafer variations and shifts**

Variations	current (%)	ECR (%)
Wafer variation	2.60	1.70
Wafer-to-wafer shift	1.90	0.04
Total variation	3.55	1.72

Usually, it is more interesting to examine the variations based on a lot and between lots, because a larger variation is expected over different lots. Figure 2 shows the distributions for the same dynamic current and its associated ECR from two lots over five lots. We only plot the two lots that present the greatest difference on their current distributions. A similar pattern to that demonstrated by wafers is observed for lot-to-lot variations. Lot variations and shifts are listed in Table 3. It can be seen that the lot-to-lot shift of the current is about 2% and the shift of the ECR is negligible. This observation indicates that the ECR has a stronger ability to overcome lot-to-lot variations than the current. The fact that process variations have significant impact on currents makes it harder to set up tight test limits for current tests. On the other hand, tighter thresholds can be set up for ECR tests to achieve better test effectiveness.

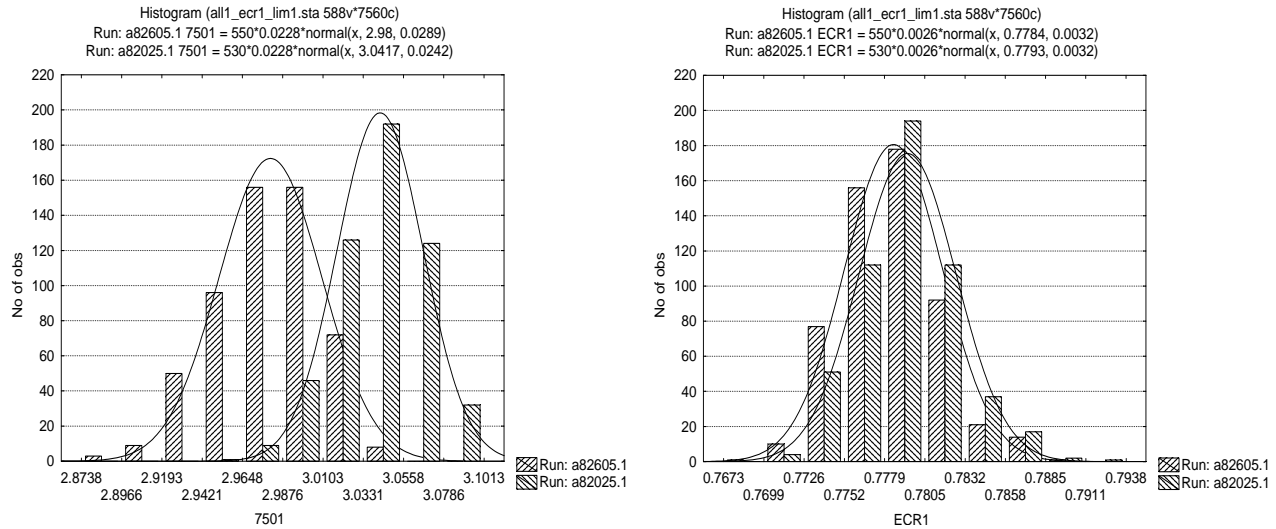
**Table 3. Lot variations and shifts**

Variations	current (%)	ECR (%)
Lot variation	3.56	1.62
Lot-to-lot shift	2.05	0.12
Total variation	4.59	1.68

## 4.2 Improving ECR Effectiveness

As mentioned before, ECR tests implemented in this product are mainly based on scan chain shift currents, which are not generated to target any specific faults. A critical issue of this type of ECR is that there may be a huge amount of signal transitions in the circuit while applying those generic ECR patterns that are not optimized to reduce unnecessary transitions. A large amount of unnecessary transitions certainly reduces or even eliminates the impact of a fault on the overall transitions. Fortunately, the device under test is implemented with multiple scan chains with the intention to improve test efficiency. We take the advantage of this DFT feature of this device for ECR tests. There are eight scan chains in this design, which virtually divide the circuit into eight blocks. Note that there may still be some logic interactions between these blocks, but the transitions associated with one chain should be greatly reduced when compared with the overall transitions caused by shifting all the chains.

In this section, we compare the ECR effectiveness between the multiple scan chain design and its equivalent single scan chain design of the same product. Recall that four types of thresholds have been defined for various ECR tests



**Figure 2. Distributions of (a) dynamic currents (b) ECRs from 2 lots**

in Section 3.2. To make a baseline performance comparison between ECR<sub>ssc</sub> and ECR<sub>msc</sub> tests, we use the minimum to maximum range of ECRs from good devices as test thresholds, which is also classified as conservative ECR or ECR<sub>mm</sub> test. The results are listed in Table 4. It can be seen that the number of defective devices detected by multiple-scan-chain-based ECR<sub>msc</sub> are increased by 57%. The increased number of detections suggests that multiple scan chain or other virtual circuit partition techniques can be used to improve ECR test effectiveness. This conclusion can be extended to physical circuit partition techniques. Therefore, circuit partition techniques, virtual or actual, can be used to address the potential low ECR defect coverage caused by a large amount of transitions in the whole circuit.

**Table 4. Effectiveness Improvements of ECR<sub>msc</sub>**

	ECR <sub>ssc</sub>	ECR <sub>msc</sub>	Improvement
Faulty	526	826	57%

Now let us examine the effectiveness of ECRs based on different patterns. Recall we have five ECR groups defined for five available patterns in this experiment. The number of faulty devices detected by each group is listed in Table 5. It can be seen that patterns 5 (70% of 1's) and 3 (pseudo random) provide better performance than others. Another observation is that ECR performance of patterns 1 (010) and 2 (01100) are very close. The cause could be the similarities on the transitions activated by these two similar patterns. Both patterns also produce a much larger amount of transitions than patterns 3 and 5, which explains their inferior per-

formance to those of patterns 3 and 5. Note that each number shown in Table 4 involves all the scan patterns, while each number in Table 5 involves only one pattern. Each pattern contributes to the total number of ECR detections. For each pattern in Table 5, the ECRs are calculated between the currents from individual chains, not between the currents from different patterns (see Table 1). Due to the intra-die process variations, the ECRs based on one pattern over different chains may show a lower effectiveness than those based on one chain at a time over different patterns.

**Table 5. Effectiveness Comparison of pattern-based ECRs**

	ECRpat1	ECRpat2	ECRpat3	ECRpat4	ECRpat5
Faulty	636	635	668	609	679

### 4.3 Overall ECR Effectiveness vs Traditional Tests

In this section we compare the effectiveness of all ECR tests based on different thresholds, against traditional tests. Recall that ECR tests with different thresholds have been identified by ECR<sub>mm</sub>, ECR<sub>4σ</sub>, ECR<sub>5σ</sub>, and ECR<sub>6σ</sub>. The types of test effectiveness was classified in [16] as Type-A (Absolute) effectiveness, Type-R (Relative) effectiveness, and Type-U (Unique) effectiveness. Table 6 shows the comparison results of the major tests applied to the available wafers. All the numbers except those in Column 2 are in percentage.

**Table 6. Effectiveness of ECR vs Traditional Tests**

Tests	Fail	Cov	memo	func	stuc	tran	stat	IDDQ	dyna	ECRmm	ECR4 $\sigma$	ECR5 $\sigma$	ECR6 $\sigma$
memo	1370	78.6	–	13.6	13.1	13.2	63.3	68.8	65.0	73.5	73.5	71.5	70.9
func	328	18.8	56.7	–	80.2	80.2	79.0	96.3	73.2	91.2	91.2	89.6	89.6
stuc	432	24.8	41.4	60.9	–	99.5	72.9	98.6	70.4	91.7	91.7	91.2	90.7
tran	432	24.8	41.9	60.9	99.5	–	72.9	98.6	70.4	91.7	91.7	91.2	90.7
stat	1117	64.1	77.6	23.2	28.2	28.2	–	93.8	87.2	96.9	97.0	96.5	96.4
IDDQ	1250	71.7	75.4	25.3	34.1	34.1	83.8	–	81.2	93.0	93.4	92.6	92.2
dyna	1088	62.4	81.9	22.1	27.9	27.9	89.5	93.3	–	99.9	99.9	99.9	99.9
ECRmm	1310	75.2	76.9	22.8	30.2	30.2	82.6	88.8	83.0	–	–	–	–
ECR4 $\sigma$	1512	77.8	66.6	19.8	26.2	26.2	71.6	77.2	71.9	–	–	–	–
ECR5 $\sigma$	1327	74.1	73.9	22.2	29.7	29.7	81.2	87.3	81.9	–	–	–	–
ECR6 $\sigma$	1285	73.1	75.6	22.9	30.5	30.5	83.8	89.7	84.6	–	–	–	–

**Type-A Effectiveness** Test names except continuity are shown in the first column. Columns 2 and 3 list the number of faulty devices detected by each test and the corresponding defect coverage relative to the total number of faulty devices, 1743, detected by all traditional tests excluding continuity tests. The exceptions are the results of row ECR4 $\sigma$ , ECR5 $\sigma$ , and ECR6 $\sigma$ . The total numbers of faulty devices are different for these tests, because these tests detects new outliers and these outliers are considered as faulty devices for comparison purposes. Higher coverage indicates greater effectiveness of a test. It can be seen from Column 3 that all ECR tests with different thresholds provides a defect coverage greater than 73%, which is much better than any other tests except memory test. IDDQ shows a coverage of 71.7%. Note that the IDDQ test patterns are deterministic and optimized for the highest defect coverage, while the ECR test patterns used here are simply generalized vector sequences that do not target any specific faults in the circuit. Furthermore, IDDQ tests include two parts, the normal ATPG patterns and the scan-chain-shift pattern “01100” that is same as one of the scan patterns used for ECR tests. The IDDQ coverage provided by this shift pattern is 63.3%. Dynamic current test (marked as dyna) shows a coverage of 62.4%, which is more than 10% lower than the ECR tests. Obviously, the wider the threshold of an ECR, the less the defect coverage it will claim.

**Type-R Effectiveness** Let us check the relationships of the effectiveness between these tests. To proceed the comparison, we assume the defective devices detected by any test are truly defective, even though they might be just different ones. Columns 4 through 13 list the conditional defect coverage for the named column tests respectively. Each conditional coverage is relative to the number of faulty devices detected by the test listed in the related row. It is defined as the ratio of the number of devices that fail both the tests across the corresponding row and column to the num-

ber of devices that fail the test identified by the row. Higher conditional coverage indicates larger overlap between the two tests, and therefore better relative effectiveness of the named test in the column correlated with the test in the row.

A better relative effectiveness of a test helps to improve the test efficiency. It can be seen that, in general, logic-based tests such as functional, stuck-at, and transition delay tests provide much lower conditional coverages than current-based tests such as static current, IDDQ, and ECR tests. For this experiment, current-based tests even demonstrate a better relative effectiveness between current-based tests and logic-based tests than the relative effectiveness between the logic-based tests themselves. This again indicates that current-based tests may detect more defects and more types of defects than logic-based tests [1][16][17]. Both IDDQ and ECR tests show excellent relative effectiveness with any other tests, with the difference that IDDQ shows better performance correlated with functional, stuck-at, and transition delay tests, while ECR behaves better when correlated with memory, static current, dynamic current, and IDDQ tests. In fact, ECR tests provide the best correlation with memory tests, which is over 70% for all ECR tests. The major reason is that the memory address lines toggle for some ECR patterns. Note that other memory logic is not touched by ECR tests, which indicates that the increase of on-chip memory may have only minor impact on ECR effectiveness. Generally speaking, ECR tests are competitive to IDDQ tests. Comparing the results between row ECRmm through row ECR6 $\sigma$ , we can see that both ECR5 $\sigma$  and ECR6 $\sigma$  tests present a performance on relative effectiveness very close to that of ECRmm test, which is considered as a baseline ECR test for performance comparison. ECR4 $\sigma$  test is aggressive compared with ECRmm test.

**Type-U Effectiveness** The number of devices that failed only one test and passed all other tests was defined as Type-U (Unique) effectiveness. Unique effectiveness of a test in-

dicates the necessity of that test in the test universe. Table 7 lists the unique failure status for five different sets of tests. Column 2 shows the numbers of unique failures for the corresponding tests in the first column after applying the original existing tests. Column 3 shows the unique failure status for the original tests plus ECRmm tests, Column 4 for the original tests plus ECR4 $\sigma$  test, Column 5 for the original tests plus ECR5 $\sigma$  test, and Column 6 for the original tests plus ECR6 $\sigma$  test. An entry 0 means the corresponding test does not detect any unique failures. Over all sets of tests, the largest number (about 300) of uniquely detected defective devices is provided by memory test, which is understandable because all other tests are not designed to exercise the memory portion of the circuit. Thus, memory test is a necessary test to detect any memory failure. With the original tests applied, static current test provides the second largest number (39) of unique failures, IDDQ the third (19), and dynamic the fourth (1). None of the functional, stuck-at, and transition delay tests detected any unique failures. Further investigation reveals that there is one device that failed only stuck-at and transition delay tests. This means stuck-at and transition delay tests are mutually redundant tests, and one of the two can be removed from wafer screening tests. Similarly, functional test can be removed from the test sets. Note that to ensure the high quality of our products, these tests are retained.

**Table 7. Unique Failure Status**

Tests	Orig.	+ECRmm	+ECR4 $\sigma$	+ECR5 $\sigma$	+ECR6 $\sigma$
memo	333	297	300	319	325
func	0	0	0	0	0
stuc	0	0	0	0	0
tran	0	0	0	0	0
stat	39	17	16	19	19
IDDQ	19	13	13	14	15
dyna	1	0	0	0	0
ECRmm	-	0	-	-	-
ECR4 $\sigma$	-	-	200	-	-
ECR5 $\sigma$	-	-	-	47	-
ECR6 $\sigma$	-	-	-	-	16

The status of unique failure detections is changed if any of the four ECR tests, ECRmm, ECR4 $\sigma$ , ECR5 $\sigma$ , and ECR6 $\sigma$ , is applied. Basically, they detect about half of the static current unique failures, more than one fifth IDDQ unique failures, and one dynamic current unique failure. Recall that ECRmm test is a conservative ECR test used as a baseline comparison, which means the established thresholds guarantee all good devices identified by traditional tests will pass ECRmm tests. Hence, ECRmm will not detect any new outliers or unique failures (no yield reduction). In general practice, however, statistically character-

ized thresholds may be desired for ECR tests, such as those used for ECR4 $\sigma$ , ECR5 $\sigma$ , or ECR6 $\sigma$ . In this experiment, ECR4 $\sigma$  detects 200 new outliers (2.6% yield reduction) because of its tighter limits, and ECR5 $\sigma$  detects 47 outliers (0.6% yield reduction). ECR6 $\sigma$  detects 16 unique outliers, which is in the same order of IDDQ test (19), but different devices. Combining this fact with the observation from Type-R Effectiveness, we can make the suggestion for this product that ECR6 $\sigma$  be the accepted test with overall competitive performances. Of course, applying tighter limits will identify more outliers and applying wider limits will ease the yield reduction. It is worth mentioning that ECR6 $\sigma$  covers as high as 92.2% of IDDQ failures (Table 6). Note that 16 outliers identified by ECR6 $\sigma$  test represents a yield reduction of 0.2% based on the original tests. This yield reduction is more acceptable to industry with high quality requirements, such as biomedical engineering. However, general product manufacturer may need to justify this reduction together with the costs associated with a potentially low quality product.

**Efficiency** We presented data to show that ECR test is one of the most efficient tests for one of our single-scan-chain designs [15]. For reference, the test time of some major tests for this multiple-scan-chain design is listed in Table 8. The total test time of a good device is 72 seconds. ECR test takes about 0.8 seconds. It can be seen that ECR test is more efficient than any other major tests. If ECR test is executed early in the test suite when using a stop-on-fail method, the extra ECR cost will actually reduce the overall test time [19].

**Table 8. Test time of ECR vs other tests**

Test	memo	func	stuc	tran	Iddq	ECR
Time (s)	19.4	2.4	1.2	2.1	3.9	0.8

**Summary** We have made comprehensive comparisons on the effectiveness of various ECR tests with different limits and major traditional tests. Based on this set of experimental results,

- Type-U test effectiveness analyses suggest that statistical threshold based ECR test may be effective in further enhancing product quality. The threshold needs to be characterized and justified for a product by post-processing its data. Some major traditional tests may be redundant and can be removed from the test sets during device screening tests to save test time.
- Type-A and Type-R test effectiveness analysis indicates that current-based tests may detect more defects and more types of defects than logic-based tests.

- The limitation of ECR tests is that their effectiveness may be affected by measurement error. More accurate measurement is required for higher ECR resolution.

## 5 Conclusion

In this paper, we demonstrated the capability of anti-process-variation of the test metric ECR by comparing the lot-to-lot shifts between ECRs and their component dynamic currents. The shift of currents is significant, while the shift of ECRs is negligible. This property makes tighter test limits possible for dynamic current-based tests over different processes, and therefore forms a higher quality test. We then compared the effectiveness of ECR tests based on a multiple scan chain design with that of ECR tests based on an equivalent single scan chain design of the same product. The results prove that circuit partition techniques can be utilized to address the issue of large numbers of transitions for large designs, should generic ECR tests be applied. Multiple scan chains virtually partition the circuit into several blocks, so that the total amount of transitions of the circuit can be greatly reduced by shifting only one chain at a time while measuring the dynamic current. Reducing the total amount of transitions magnifies the fault effect and therefore increases the ECR test effectiveness. Also, patterns creating less transient activities in a circuit may generate ECR tests with better performance. Another focus of this paper was comparing different threshold-based ECR tests with major traditional tests. The test process was conducted by setting different statistical thresholds for ECR tests. Each type of ECR test was applied in addition to our existing traditional tests to the biomedical IC product with multiple scan chains. The experimental results show that ECR tests based on statistical limits identified new outliers from the good die of the tested wafers, which may enhance our IC quality.

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