Testability Features of the Alpha 21364 Microprocessor

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Abstract

The custom testability strategy of the Alpha 21364, Hewlett-Packard's most recent Alpha microprocessor, builds upon its Alpha 21264 embedded core. Several additional DFT features integrate to meet the testing challenges of the new generation.

1. Introduction

The Alpha 21364 [1] is the fourth generation Alpha microprocessor. This 139 million transistor 1443-pin chip, originally a 0.18 μm bulk CMOS device, has been recently implemented using 0.13 μm SOI technology [2].

The chip design combines the previous generation Alpha microprocessor (Alpha 21264 [3]) as an embedded core with a 1.75 MB second-level cache, two high-performance memory controllers and an on-chip interprocessor router. Figure 1 shows the chip photomicrograph.

Like its predecessors [4], the Alpha 21364 microprocessor follows a custom testability strategy. That is, the total test solution consists of a blend of custom design for test (DFT) techniques, handcrafted test patterns, and test engineering tools and procedures. Each aspect of the test methodology specifically targets a unique testability goal.

The implementation of this strategy on the Alpha 21364 faced several interesting challenges. First, since the chip embeds the previous generation microprocessor as its core, new DFT solutions needed to seamlessly integrate with the inherited DFT and testability access infrastructure. Second, the chip's high performance interfaces and large number of pins required special attention to ensure that the chip is testable on affordable testers. Third, aggressive time-to-market goals necessitated the need for rapid prototype debug capabilities. Finally, unlike previous generations, the Alpha 21364 relies entirely on external foundries in its production. This created additional test requirements including the need for significantly enhanced debug and diagnosis, increased production test pattern suite stability, and chip testability on automated test equipment (ATE) available at the foundry.

This paper focuses on the testability features of the Alpha 21364 microprocessor. A companion paper [5] details the chip's debug features. The paper is organized as follows: Section 2 describes the testability features, Section 3 briefly describes the testability access architecture, Section 4 summarizes some key results, and Section 5 concludes the paper.

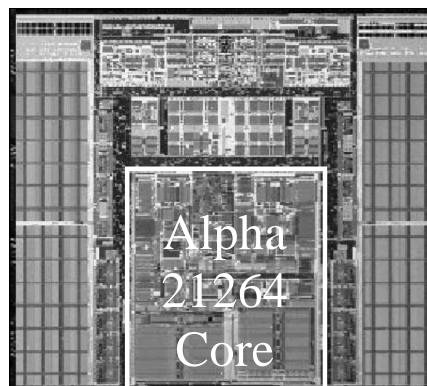

Figure 1: Alpha 21364 Microprocessor

[*] The work for this paper was performed while the authors were with Compaq Computer Corporation/Hewlett-Packard Company.

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2. Testability Features

The Alpha 21364 employs a two-level hierarchical test organization. In this scheme, similar test targets collectively form a test target group. The test targets within a group employ similar, but dedicated testability resources. Members of a group are daisy-chained and transport data and results serially. A single central controller interfaces with the test features using a small number of wires. External access to the test features is provided via an IEEE 1149.1 test access port (TAP) [6] interface.

Figure 2 shows the top-level view of the Alpha 21364 testability feature organization. The features located in the Alpha 21264 core are shaded in black.

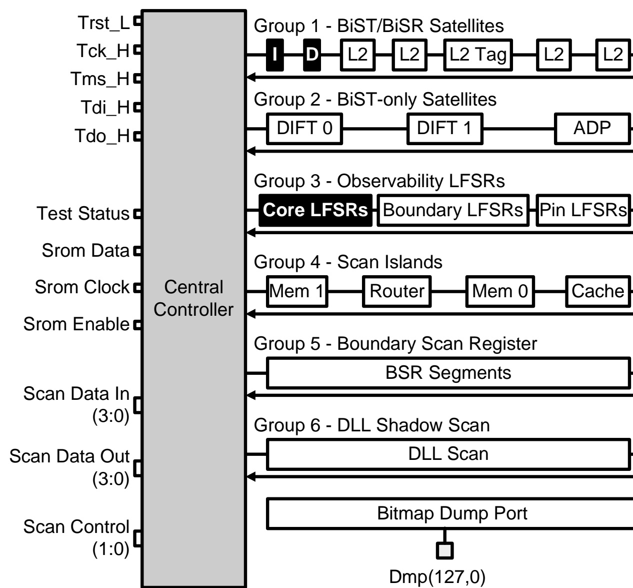

Figure 2: Alpha 21364 Testability Features

Group 1 - BiST/BiSR Satellites

This group includes seven test satellites that control the testability features of all major RAM arrays. These arrays include: the L2 cache and tags, L1 instruction cache and tags, and L1 data cache, tags and ECC. Due to its size and location on the die, the L2 cache contains four quadrants, each accessed by its own test satellite.

The Group 1 satellites support the following test operations:

- Automatic power-on self-test
- Quick-initialization upon special reset
- Freeze and dump for system debug on certain arrays
- Manufacturing self-test and self-repair
- Retention self-test
- Bitmap

Each of the Group 1 arrays performs self-repair using redundant state elements. To further improve yield, the larger arrays employ two-dimensional self-repair [7]. The self-repair allows a one-pass wafer probe, streamlining chip production. The Alpha 21364 supports permanent cache repair through the use of laser-blown fuses.

The Group 1 arrays allow the bitmap operation to be performed while performing BiST at full speed. Throughout the BiST operation, the bitmap data is serially transported to the pins and outputted via a 128-bit bitmap dump port. The bitmap dump port shares its pins with the chip's functional interface.

Group 2 - BiST-only Satellites

This group is comprised of three satellites targeting two small RAM arrays located in the memory controller unit and a RAM/CAM combined array in the L2 cache controller data path. These arrays are an order of magnitude smaller than the Group 1 arrays. Consequently, they include no repair overhead.

The Group 2 satellites support a wide assortment of features to achieve their test goals as well as aid in the debug process including:

- Automatic power-on self-test
- Freeze and dump for system debug

- Manufacturing initiated self-test, which allows viewing of pass/fail status of individual satellites
- Address map

Group 3 - Observability Registers

The Alpha 21364 includes observability registers [8] based on linear feedback shift registers (LFSRs). They serve three objectives: enhance the fault coverage of the hand-crafted functional tests, support reduced-pin count testing, and provide internal observability for chip and system debug. The chip contains observability register nodes at the boundary of and throughout the Alpha 21264 core as well as at the system bus interfaces. In total, the Alpha 21364 has 86 LFSR chains observing approximately 6000 chip nodes.

The Alpha 21364 partitions the observability registers into several independent LFSR segments, which are daisy-chained together for serial access. This organization provides several benefits. It confines and contains the impact of non-deterministic data resulting from the capture of uninitialized state. It increases failure isolation. Finally, it facilitates debug by allowing the bypass of all LFSR segments except those of interest.

The observability registers support two primary modes of operations single-cycle snapshot mode used for debug and multi-cycle signature mode used for production test. In both cases, the observability registers operate at full CPU speed, allowing data capture at any CPU cycle. The IEEE 1149.1 TAP and the LFSR control logic located inside the central controller control the oberservability register operation.

Group 4 - Scan Islands

The Alpha 21364 implements partial scan in the new logic outside of the Alpha 21264 core. While the primary goal was to facilitate rapid debug and diagnosis, the implementation also allows leveraging scan for a variety of production test purposes, including ATPG-based patterns.

The Alpha 21364 supports the following scan test modes:

- Traditional scan testing from tester
- At-speed manufacturing scan-BiST from on-chip random pattern source
- Manufacturing scan with patterns supplied from tester via the scan wheel [9]
- Quick-initialization of the scannable state upon powering up
- A dump of scannable state for system debug

To increase the effectiveness of ATPG and test operation, the partial scan implementation employs a partitioning scheme called scan islands [10]. This architecture allows ATPG to be performed on partitions independently. During production test, islands may be tested separately and simultaneously or chained together to form an archipelago, which permits the testing of interfaces between islands.

The IEEE 1149.1 TAP and the central scan controller located inside the central controller control the scan operations. A scan interface port called an isle scan port provides local control to each island and its scan chains.

The Alpha 21364 has four scan islands, each with four parallel scan chains. The penetration of scan in the islands is in the range of 25-40%. The total number of scan-flops is approximately 13,000.

Group 5 - Boundary Scan Register

The Alpha 21364 incorporates a boundary scan register (BSR) architecture to facilitate testing of its high performance interfaces. It supports three main objectives:

- Traditional board-level interconnect testing using IEEE 1149.1 EXTEST and SAMPLE instructions
- AC-parametric testing for characterization and production screen of high performance interface pins on a limited-capability tester
- Observability of unconnected output pins during functional testing in a reduced-pin tester environment

AC-parametric testing of high performance pin interfaces is a challenge that is new for this generation of Alpha. Three features play together to meet this challenge. First, all high performance interface pins incorporate on-chip loop-back capability [11]. To facilitate this, all pins are implemented as bidirectional. This required adding test receivers to output-only pins and test drivers to all input-only pins. Second, the pin interface and internal registers provide control of the skew of the driver and receiver clocking. This allows margining data loopback across a range of driver and receiver clock frequencies. Finally, the BSR structures allow an on-chip method for test stimuli generation and response evaluation.

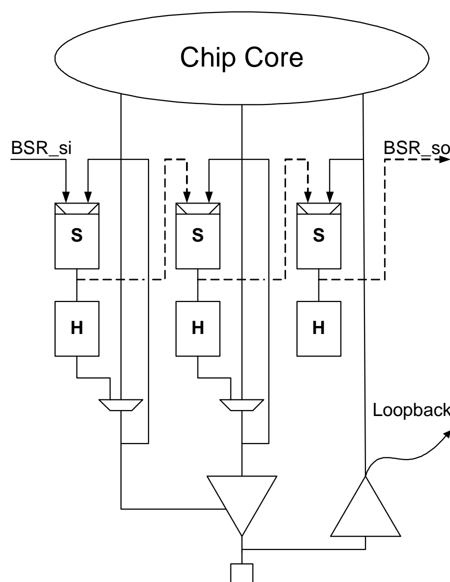

Figure 3: Alpha 21364 BSR Structure

Figure 3 shows the BSR structure at each pin. It consists of three BSR cells, one each for incoming data, output data and the pin direction control. Each BSR cell has a shift flip-flop and a hold flip-flop. The six flip-flops present in the BSR cell may be reconfigured to form a 6-bit LFSR.

This configuration is known as pin-LFSR mode. The LFSR of the pin under test generates the test stimulus data while the LFSR of an adjacent pin captures a signature using the loopback data. Switching the compressor and generator roles allows testing of the full interface in two passes. The generation and receiving of data is entirely contained on-chip and performed at the full speed of the pin interface. AC-parametric testing of the pins is thus achieved with reduced dependency upon the ATE timing accuracy.

Another mode of operation, called chip-LFSR mode, concatenates all pin-LFSRs of a high-speed interface to form a very wide LFSR. This mode captures and compresses the data driven to the output pins, allowing functional testing on a reduced-pin tester environment. The chip-LFSR mode comprises an integral part of the Group 3 observability LFSRs described earlier.

The per pin tristate control provides the ability to perform DC-parametric testing in a reduced-pin tester environment by ganging several unconnected pins together on a single tester channel. Each pin is enabled one at a time, while all of the other pins sharing the tester channel are tristated. This allows the serial DC-parametric testing of all outputs using a reduced number of tester channels.

Included within the boundary scan shift path are special control registers that configure the pins under test. This includes features such as driver strength selection, driver enabling, and pin termination control. Although this is a deviation from the IEEE 1149.1 standard, the boundary scan offers a convenient access mechanism to these controls and greatly improves the testability

of the pin interface both during chip manufacturing and board-level testing.

Group 6 - DLL Shadow Scan

The Alpha 21364 possesses several delay-locked loops (DLLs) in its high-speed pin interfaces and in the new logic outside of the 21264 core. The DLL shadow scan architecture allows access to all DLLs operating in different clock domains via a single scan-path. This technique provides a basic functionality to characterize and test the digital logic and the digital/analog (D/A) interfaces present in these DLLs. Specifically, DLL shadow scan facilitates three test objectives:

- Testing of the DLL digital logic via ATPG-generated test patterns
- Providing direct access to digital DLL control logic to facilitate testing of the analog logic
- Observability of DLL digital state during normal chip operation

The architecture implements special DLL shadow scan-flops at the D/A interfaces and throughout the digital logic of the DLL. Figure 4 shows the DLL shadow scan-flop. It consists of two flip-flops: a system flop from the normal DLL interface and a shadow flop that is part of the DLL scan path. The shadow flops provide the serial scan path to load and unload data to and from the DLL logic under test. The system flops receive test data from the scan path and also load the scan path with the circuit response.

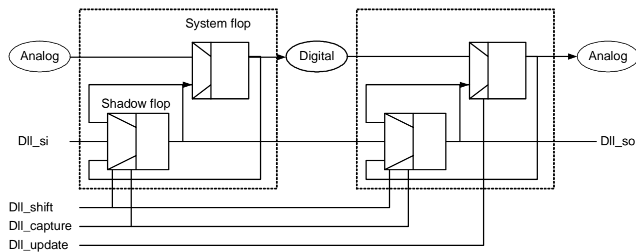

Figure 4: DLL Shadow Scan

The IEEE 1149.1 TAP controls the operation of the DLL shadow scan architecture. The TAP controller initiates all data transfers between the system and shadow flops. The system flops receive data from the shadow flops upon leaving the Update-DR state. The system flops transfer data back into the scan path upon entering the Capture-DR state.

The Alpha 21364 has ten high performance ports, each with multiple DLLs operating in their independent clock domains. This offered the unique challenge of stringing shadow scan-flops in different ports into a single chain.

The DLL shadow scan architecture mitigates this challenge by synchronizing the test control signals locally in each port with the clock domain of the DLL under test (DCLK). The test data crosses clock domains when loading from the shadow flops into the system flops. Likewise, the response data crosses back into the scan path clock domain (NCLK) when captured by the shadow flops. The entire shadow scan path shifts within the NCLK domain. Internally to the chip, the TCK pin is synchronized with NCLK. From the standpoint of the user, the DLL shadow scan appears to operate entirely using TCK even though it actually accesses several clock domains.

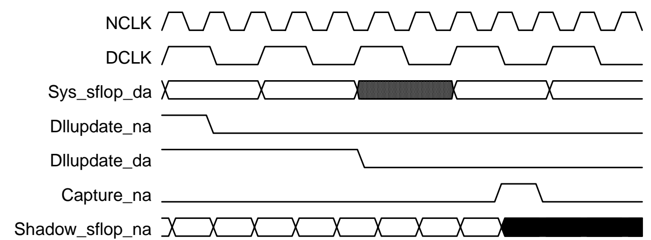

Figure 5: DLL Digital Test Timing Diagram

Figure 5 illustrates an example of the DLL digital logic test operation. The deassertion of the update signal from the central controller (Dllupdate_na) in the NCLK domain begins the operation. Synchronization logic crosses this signal into the DCLK domain (Dllupdate_da).

Shadow scan data is transferred to the system flip-flops upon the falling edge of this signal.

Once the digital logic under test reaches a stable state, the shadow scan may capture the response. The capture command from the central controller begins the response sample operation. The assertion of the Capture_na signal transfers the response data from the system flops into the shadow flops that will shift the data to the pins.

In addition to testing the digital logic, the DLL shadow scan also provides test access to the reference loop clock generators and the phase mixing logic. Access to these circuits provides the ability to manually force the generation of different clock waveforms and provides observability into the internal DLL state.

3. Testability Access Architecture

To address the challenge of accessing test features scattered widely across the chip using a minimum number of wiring channels, the Alpha 21364 employs a two-tier hierarchical access scheme.

At the top-level is the central controller, which broadcasts global control the test target groups. All targets within a group respond identically to global broadcasts. The global broadcasts transfer test data and results and initiates test actions.

At the bottom-level are the local controllers located at each test target. One or more test control registers in a local controller provide customized test target-specific control as well as any parameters for test operation.

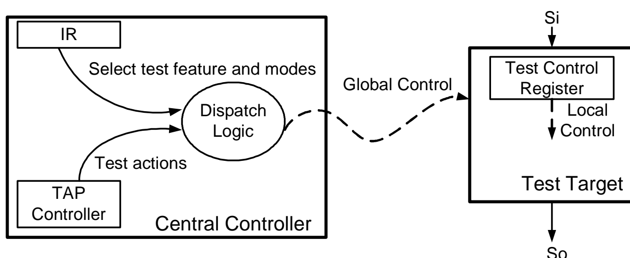

Figure 6: Testability Access Architecture

Figure 6 illustrates the control organization. A single IEEE 1149.1 TAP provides the interface to the outside world. The TAP instruction-register selects testability features and test modes. The TAP controller initiates all test operations as well as controls the shifting of data and results to and from the test satellites. The central controller broadcasts the instruction register and TAP controller state to the testability features using a small number of wires. As mentioned earlier, the testability features themselves are daisy-chained to transport test data and results via a serial shift register path.

The testability access architecture faced a unique challenge in interfacing the internal scan chains with external testers. All scan-flops on the Alpha 21364 use a data-mux implementation. Consequently, the scan chains shift at full speed with the normal CPU clock. Ordinarily, a tester cannot source or sink data such a high rate.

The Alpha 21364 solves this problem with the innovative scan wheel interface [9] that allows a slower speed ATE to load/unload scan chains operating at full CPU speed. Connecting the last scan-flop to the first scan-flop in a chain forms a scan wheel. This circulates the captured data to keep it alive in a closed loop. A sampling mechanism unloads and injects new data into the scan wheel periodically until all scan-flops have been read and written.

In addition to interfacing the scan chains with a slow speed tester, scan wheel provides a more general-use mode of viewing data generated at the full CPU speed using a slow ATE interface. The dumping of arrays and observability registers use the scan wheel interface.

4. Results

In all, the testability features of the Alpha 21364 use approximately 150K transistors (not including scan overhead) and occupy approximately 2% of the total die area. The testability access architecture uses eight

dedicated pins and shares the remainder with the normal functional pins. Synthesis and automatic place and route tools implemented the majority of the testability logic.

All of the testability features are operational and have been fulfilling the Alpha 21364 testing and debugging needs since first silicon.

The Group 1 and Group 2 satellites have been useful from both a test and debug standpoint. Together, they successfully self-test over 116 million of the 139 million devices on the chip. The self-repair has allowed a one-pass wafer probe, eliminating an extra testing step and reducing test costs.

The ability to freeze and dump the contents of the L2 cache and tag arrays and the Group 2 arrays has been extremely valuable in both chip and system debug. The Alpha 21364 also contains an on-chip logic analyzer that writes information related to program execution and memory accesses to the L2 cache. When used in combination with the array dump, this ability has provided essential information for the debug of the chip.

The array bitmap and address map have also been used for debug and yield engineering. In particular, the Group 2 address map helped in tracking down CAM-cell voltage sensitivity.

The observability registers at the high performance pin interfaces allow the 1443-pin Alpha 21364 to be thoroughly tested at wafer-probe using a 512-pin tester, thus weeding out the defective parts early and saving the cost of expensive packages. The fault coverage gains from the other internal observability registers is not explicitly measured, but based on previous experience, is speculated to be in the range of 1-3%.

The implementation of partial scan and the scan island architecture yielded mixed results. The scan island architecture itself has proven to be an extremely effective mechanism for the generation and delivery of ATPG patterns. Commercial ATPG tools generated the ATPG patterns using scan island-level wirelists. The ability to partition the chip into smaller sections greatly eased the burden on the ATPG tools and sped up the pattern generation process. Adding a simple pattern header easily converted the scan island ATPG patterns to chip-level patterns. All ATPG patterns generated for each scan island ran successfully at first silicon.

Despite the success of the scan architecture itself, the ATPG coverage is not at all impressive. The 15-40% penetration of scan in the islands proved to be too little to obtain any meaningful coverage. However, this has no consequence on the Alpha 21364 coverage levels as the overall test strategy relies on at-speed functional tests for production screens. The design and test teams learned several valuable lessons in implementing and using scan.

Similar to scan, the scan-BiST feature yielded mixed results. The grossly partial scan did not yield meaningful coverage. However, scan-BiST turned out to be extremely useful for burn-in testing. Its pseudo-random patterns generate toggle activity on 50-60% of the nodes throughout the scan islands.

The scan wheel mechanism paid off in two ways. First, it allowed ATPG patterns to be run using a slow ATE interface. Second, the ability to dump the scannable state to the pins was vital in tracking down several bugs.

The Alpha 21364 is the first Alpha microprocessor to extensively exploit many test features for the purpose of system debug. A simple notebook PC-based IEEE 1149.1 master controller provides access to the test features in system environment. This gives a direct method to validate and debug chip functionality without relying on system firmware. This access mechanism found and resolved many production-related problems early in the prototype debug process. This backdoor test access also provides a higher degree of precision and easier bug

diagnosis when compared to software-based approaches.

Both ATE and system-based testing utilize the boundary scan logic heavily for testing the chip interfaces. ATE and system board-level test use the BSR structures for their AC-parametric and DC-parametric test capabilities as well as characterizing signal integrity.

The DLL shadow scan has been used extensively for both circuit characterization and debug. The DLL state observability provided invaluable insight used to validate the DLL operation. The ability to drive the analog DLL circuitry with test data was also used for characterizing the frequency response of the chip DLLs. This insight into the actual operation of the DLLs allowed refinement of the circuit simulation models and helped to understand the impact of manufacturing process upon the DLL performance.

5. Concluding Remarks

The paper presented the testability strategy and the testability features of the Alpha 21364 microprocessor. This strategy builds upon the custom testability strategy of its embedded Alpha 21264 core and adds several new features to solve the testability problems of the new generation. The features of the two generations seamlessly integrate to present one unified testability solution for the entire chip. All features are operational in manufacturing and delivering their promised functions. Furthermore, the design and test teams learned several valuable lessons that they will carry forward to future generations of microprocessors.

The Alpha 21364 testability architecture boasts several innovations. The two-level hierarchical organization of daisy-chained test targets provides uniform testability access over a minimal number of global wires. The two-dimensional row-column self-repair, observability register architecture, scan island partitioning, scan wheel interface, and comprehensive BSR and DLL shadow scan architecture are all innovations that play together on the Alpha 21364 to solve a variety of test and debug challenges.

The Alpha 21364 testability features represent a stage in the continuous evolution of the Alpha microprocessor test strategy. Although this is the last Alpha microprocessor, we hope the techniques developed and lessons learned will find their way into future microprocessor designs.

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