

TRIBuTE™ Board and Platform Test Methodology: Intel's Next-Generation Test and Validation Methodology for Platforms

Jay J. Nejedlo, Intel Corporation, Hillsboro, OR, USA

jay.nejedlo@intel.com

Abstract

Built-in self-test (BIST) has been historically silicon-centric in its application. This paper offers an overview of Intel's next-generation platform test methodology, TRIBuTE™. TRIBuTE™ is an Intel-coined acronym for Three-Reuseable-Integrated-Bist-u-TEchnologies. The TRIBuTE™ approach targets the replacement of today's standard platform testing process and exploits BIST in a novel way.... comprehensive board and platform testing.

This paper was submitted under the ITC Special Board and System Test Call-for-Papers that had an extended due-date. As such, the full text of the paper was not available in time for inclusion in the general volume of the 2003 ITC Proceedings. The full text is available in *2003 ITC Proceedings—Board and System Test Track*.