

Detection of Resistive Shorts in Deep Sub-micron Technologies

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Abstract

Current-based tests are the most effective methods available to detect resistive shorts. Delta I_{DDQ} testing is the most sensitive variant and can handle off-state currents of 10-100 mA of a single core. Nevertheless this is not sufficient to handle the next generations of very deep sub-micron technologies. Moreover delay-fault testing and very-low voltage testing are not a real alternative for the detection of resistive shorts. The main limitation of ΔI_{DDQ} testing is the intra-die variation of the threshold voltage which results in variations in the off-state current. Two methods are investigated that improve the detection capabilities of ΔI_{DDQ} testing. The first method reduces the impact of intra-die variation by reducing the amount of logic that switches states. This method can handle very large off-state currents although at the cost of a substantial increase in test time. The second method investigates the correct scaling of the intra-die variations as a function of temperature. We show that both methods improve the detection capabilities of ΔI_{DDQ} testing.

1 Introduction

Shorts are one of the main defect mechanisms in deep sub-micron technologies. The adequate detection of these defects is important to achieve the required quality levels of modern ICs. How easy it is to detect this category of defects strongly depends on the resistance of the defect. Shorts with resistances of less than 1 k Ω can be detected with a Boolean test based on the (single) stuck-at fault model. Shorts with higher resistances, however, are almost undetectable with a Boolean test [1][2]. They form a reliability risk [3]-[5] although their impact on circuit performance is usually low. A much more effective method to detect shorts is quiescent current testing (I_{DDQ}). In an I_{DDQ} test one observes the (leakage) current of the power supply when no clock activity is present. This test method can detect resistive shorts as well as a wide variety of other defects and is a commonly applied test method to achieve high quality levels.

In deep sub-micron technologies conventional I_{DDQ} testing has become obsolete because of the strong increase in off-state current and due to the wide variation in

leakage currents for defect-free devices [6][7]. Therefore applying a single pass/fail I_{DDQ} limit is not effective anymore to distinguish between defective and defect-free devices. This threat was recognised in the mid 90s and technological solutions as well as more advanced test methods have been proposed. One of the most promising advanced test methods is ΔI_{DDQ} [8][9]. In ΔI_{DDQ} testing one performs relative measurements instead of absolute ones. This method allows one to detect small anomalies on top of large off-state currents. We showed that anomalies of 1% of I_{OFF} can be detected [7]. This is far better than any of the other advanced current-based test methods that have been proposed. Nevertheless, also ΔI_{DDQ} testing has its limitations. For off-state currents of more than 100 mA a detection capability of 1% is equivalent to anomalies of 1mA while for the detection of resistive shorts one needs a capability to detect anomalies of 5 to 100 μ A. Therefore the capability to detect these defects in deep sub-micron technologies is threatened. Especially since also alternative methods such as very-low-voltage testing and delay fault testing are not well suited to detect resistive shorts. In this paper two methods are investigated that improve the capabilities of ΔI_{DDQ} testing.

The remainder of this paper is organised as follows. In section 2 the limitations of ΔI_{DDQ} testing in deep sub-micron technologies are described. It turns out that the main limitation is intra-die variation. The device-under test is described in Section 3. Section 4 investigates two methods to improve the capabilities of ΔI_{DDQ} testing. Two other test methods are very-low voltage testing and delay-fault testing. Their capabilities are investigated in section 5. The paper is concluded in section 6.

2 Limitations of ΔI_{DDQ} testing

2.1 Introduction

The detectability of defects that short logic nodes strongly depends on the defect's resistance. Figure 1 shows typical voltage and current behaviour as a function of this resistance. Shorts with a resistance below 1 k Ω result in stuck-at behaviour of the affected node. For resistances above the critical resistance (R_{crit}) [1][2], however, the impact on the logical performance of the circuit be-

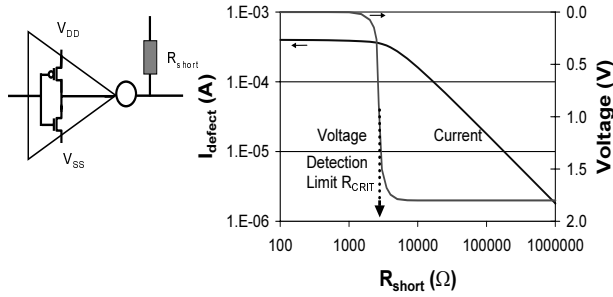


Fig. 1: Inverter with a short to V_{DD} and the resulting voltage and current impact as a function of resistance.

comes very small.

Besides observing the voltage behaviour one can also investigate the current behaviour. Due to the defect an additional current is flowing between V_{DD} and V_{SS} . This additional current is what is detected in current-based tests. For a purely resistive defect this additional current scales linearly with the resistance and a $100\text{ k}\Omega$ short will therefore result in an I_{DDQ} anomaly of about $10\text{ }\mu\text{A}$, while a $10\text{ k}\Omega$ results in an I_{DDQ} anomaly of $100\text{ }\mu\text{A}$. As long as one can detect these anomalies, a current-based test is more sensitive than a voltage-based test. This small additional current, however, is obscured by a large off-state current in deep sub-micron technologies and the method starts to lose sensitivity. This led to the introduction of ΔI_{DDQ} . Instead of performing absolute measurements one performs differential or delta measurements. The basic assumption is that for a good IC the off-state current of a circuit is (almost) independent of the applied test pattern. If one applies different test patterns they should all result in nearly identical I_{DDQ} values. This is not the case for an IC with a short. Some patterns result in a voltage difference across the shorted nodes and an additional current will flow. If this happens one observes a high I_{DDQ} state and the defect is “active”. If the defect is not activated one observes the normal off-state current. Figure 2 shows examples of these two kinds of behaviour. The defect-free device shows no major changes in leakage current as a function of test pattern while for the defective IC one can recognise high and low I_{DDQ} states. This delta between the I_{DDQ} currents is the rejection criterion in a ΔI_{DDQ} test. If the measured delta is above a certain limit the device is rejected. Typical limits are in the range of 10 to $100\text{ }\mu\text{A}$. Note that the absolute off-state current is not relevant in ΔI_{DDQ} testing since this usually indicates just a faster type of processing and is not related to defects anymore [6][7].

The detection capabilities of a ΔI_{DDQ} testing are determined by the expected variations between test patterns for a good device. These variations are usually small but not completely negligible and determine what the minimum rejection limit is. The variations stem from three

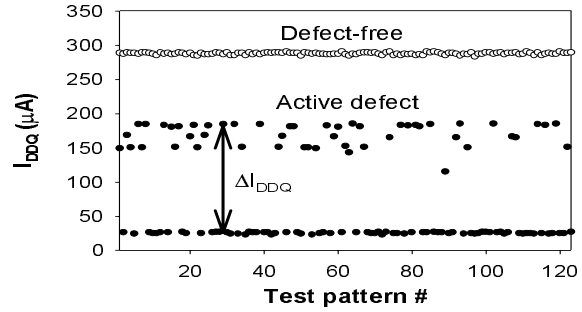


Fig. 2: I_{DDQ} as a function of test pattern for a good (open symbols) and a bad IC (solid symbols).

sources, viz. :

- measurement inaccuracies
- state dependencies
- intra-die variations.

The impact of these three sources and how they affect the capabilities are summarised in the next paragraphs; more details can be found in ref. [7].

2.2 Measurement inaccuracy

Measurement inaccuracies are not a real limitations of ΔI_{DDQ} testing. In principle the required accuracy can always be achieved with (more expensive) measurement equipment. Especially the fact that we do not need an absolute measurement but only a relative one, makes this possible. One option is a differential I_{DDQ} monitor, which only determines delta currents with respect to a reference current. For all data that is shown in this paper as normalised I_{DDQ} , the contribution due to measurement inaccuracies is much smaller than due to the other sources described in the next two sections.

2.3 State dependency

The second source of variation is state dependency and is caused by the fact that the off-state current depends on the state of a circuit. For example, the leakage current of a 3-input NOR with input vector (111) is 10-100 times lower than for (000) [10]. In circuits with 10,000 or more gates, however, these state-dependent effects start to level out. The remaining variance as a function of test pattern is quite small. Typically the difference between the minimum and the maximum leakage state is a few percent for a defect-free device [7][11].

Figure 3 shows an example how the state of a circuit affects the leakage current. In this example the I_{DDQ} values for two devices were measured. The leakage currents are normalised to the average leakage current of the IC and to highlight the state dependency the results for IC-B are sorted for increasing leakage currents. The results for IC-A are plotted in the same order as those of IC-B. Figure 3 shows that both ICs have the same behaviour as a

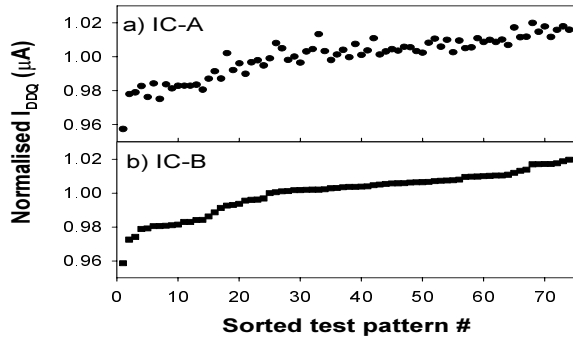


Fig. 3: State dependency. I_{DDQ} as a function of test pattern for two good ICs. The patterns are sorted in order of increasing leakage currents for IC-B

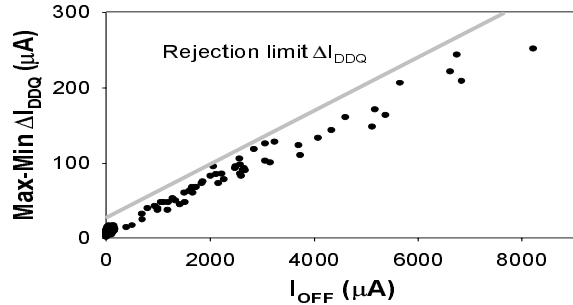


Fig. 4: Relation between the off-state current and the expected delta due to state dependencies for good devices. The grey line denotes an example of a rejection limit

function of test pattern. Both have the lowest I_{DDQ} value for the first pattern and the highest I_{DDQ} values for the last ten patterns. The correlation between these measurements is 0.96, which indicates that the test pattern dependency of IC-A is reasonably well predicted by IC-B.

In the example of Figure 3 the difference between the lowest and highest observed leakage state is 6%. This hampers ΔI_{DDQ} testing because the expected delta increases as a function of off-state current. Figure 4 shows an example from [7] which shows that for this design off-state currents of 8 mA already result in expected delta currents of 300 μA . On first sight this seems to make the detection of anomalies of 100 μA impossible. However, this state dependency is not a big limitation in practice since the state dependent component is a known contribution and it is therefore relatively easy to compensate for. Three possible solutions are:

- 1) Only use test patterns which result in “average” leakage currents. For example, the expected delta is reduced with a factor of 3 by applying only patterns 25 through 60 of Figure 3. This considerably improves the detection capabilities. However, additional patterns should be created to cover the loss of fault coverage.

- 2) Determine the delta between successive sorted test patterns instead of determining it on bases of minimum and the maximum I_{DDQ} value across all patterns. If

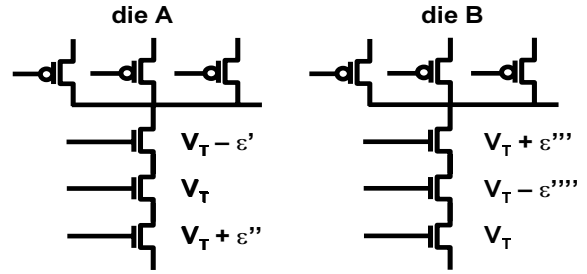


Fig. 5: An example of two 3-input NORs and how small variations affect the threshold voltage of the n-transistors.

the patterns are sorted the expected difference between two patterns is considerably smaller. For example in Figure 3 the largest jump is expected between pattern 1 and 2 but this jump is only a fifth of the difference between the maximum and the minimum.

- 3) Compare the measured values with expected values. The expected values or golden signature can be determined by measuring a large set of samples and apply statistical methods to remove outliers. For example based on Figure 3 we know that the first pattern should yield a normalised I_{DDQ} of 0.96. If we measure a normalised I_{DDQ} of 1.00 for that pattern we know that something is wrong. Also with this method a strong improvement in detection capabilities is obtained.

These three correction methods for the state-dependency can be applied individually or as a combination. So also state-dependencies are not a real limitation for ΔI_{DDQ} testing. It is furthermore important to notice that the state dependency is only determined by the part of the circuit that switches states. For a chip with a small random logic core and a large memory core the off-state current is determined by the memory but as long as the memory remains in the same state it will not cause additional variations in the ΔI_{DDQ} measurements. This is a big difference compared to current-based test methods, which try to predict the expected off-state current, e.g. based on speed [12] or neighbourhoods [13]. With these methods it becomes harder to detect small anomalies if the total off-state current increases since their capabilities are determined by the total off-state current. This severely hampers the sensitivity of these methods.

2.4 Intra-die variation

The third and last source of variation is intra-die variation. The off-state current strongly depends on the threshold voltage and (for very-deep sub-micron technologies) on the gate leakage. Intra-die variations cause small shifts in the threshold voltages of the transistors. As a result the state-dependencies are not completely reproducible. Figure 5 shows two three-input NORs as an example. The ϵ terms indicate small shifts in the threshold

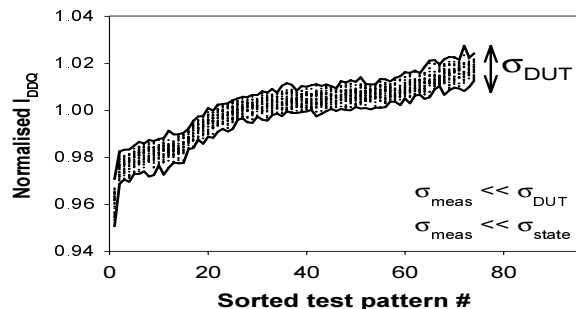


Fig. 6: Normalised I_{DDQ} results for 30 cores ($0.18 \mu\text{m}$ technology) as a function of sorted test pattern. The black lines denote the minimum and maximum observed values and the interval between them represents variations due to the intra-die component.

voltage, for example caused by stochastic dopant fluctuations. These small differences cause small deviations in the state-dependent contribution. So it is impossible to precisely predict the expected leakage current for an IC, even if the measurement inaccuracies can be neglected. The impact of these intra-die variations is shown in Figure 6. This figure shows the I_{DDQ} results for 30 identical cores as small dots. The minimum and maximum observed values per test pattern are marked with black lines. The spread per test patterns is much wider than what is expected on basis of the measurement inaccuracy (expected is less than a quarter). The best we can achieve for this design is a 1% I_{OFF} rejection limit. These intra-die variations are the main limitation of ΔI_{DDQ} testing (and any other current-based test method) since they scale with the off-state current.

Although 1% of I_{OFF} detection capability seems very good it is certainly not good enough for very deep sub-micron technologies. These new technologies have typical leakage currents of 10-100 nA/ μm and standard gate transistor W of about 1 μm . A core with a few million of these transistors already results in off-state currents of 10 to 100 mA. Delta I_{DDQ} testing becomes useless for off-state currents (of that specific core) of 100 mA since only anomalies with an impact of 1 mA can be detected. These kind of additional currents can occur for (stuck-at) test escapes, e.g. due to insufficient coverage, but are rarely associated with resistive shorts. Within Philips typical stuck-at coverage is high. Therefore one of our main interests for applying current-based tests is to screen for potential reliability fails. The capability of ΔI_{DDQ} to screen for these resistive shorts is already deteriorating at off-state currents of 10 mA. It is therefore important to search for improvements and/or alternative methods.

3 Device Under Test

The device under test (DUT) is a DSP-like core of a

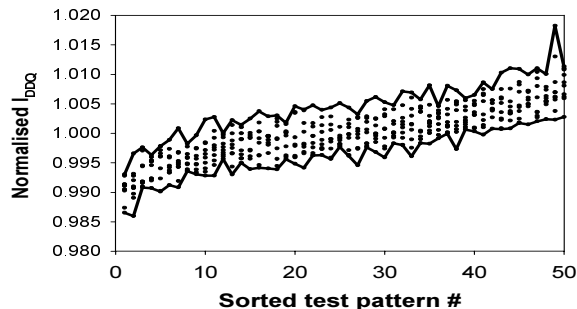


Fig. 7: Normalised I_{DDQ} results as a function of sorted test pattern for ten cores ($0.13 \mu\text{m}$ technology).

test chip. The core is made in a $0.13 \mu\text{m}$ technology with a standard gate library. No dynamic logic is used and the circuit contains more than 1 million transistors. The nominal supply voltage is 1.2 V. The typical off-state current is low enough to perform ΔI_{DDQ} testing and is therefore not yet representative for the problems we face in very deep sub-micron technologies. However, skewing the process to the fast corner results in several ICs with off-state currents in the 10 mA range for this single core. The disadvantage of using corner lots is that they are less representative for the normal processing. For example, the intra-die variation can be worse than for typical processing. In this case this is not a major objection since the purpose is not really to compare the effectiveness of different test methods but to investigate how we can improve them. If an improvement is successful for a fast corner lot in this technology it is most likely also applicable for typical processing in the next technology node.

I_{DDQ} measurements were performed for 50 patterns. The delta was determined by calculating the difference between the maximum and the minimum. The observed state dependency is 3%. This is in line with the 6% as observed for a $0.18 \mu\text{m}$ technology shown in Figure 6 because of the following. The impact of the state of a circuit roughly scales with the square root of the number of transistors. Therefore the larger the core the less one will observe variations due to state dependencies. The $0.13 \mu\text{m}$ DUT core is more than four times bigger than the one used in Figure 6 and therefore about half the effect due to state dependencies is expected. This is indeed the case.

To determine the intra-die variations ten “good” devices with off-state currents of more than 5 mA were measured. Figure 7 shows the normalised I_{DDQ} values plotted as a function of increasing average off-state current per pattern. The black lines denote the minimum and maximum observed values. The impact of the intra-die variation is about 1% of I_{OFF} . For real production settings a wider margin is required since Figure 7 is based on a very limited number of devices. For example for pattern 49 the variation is larger than for any other pattern. One could assume that this is due to a defect. However, closer

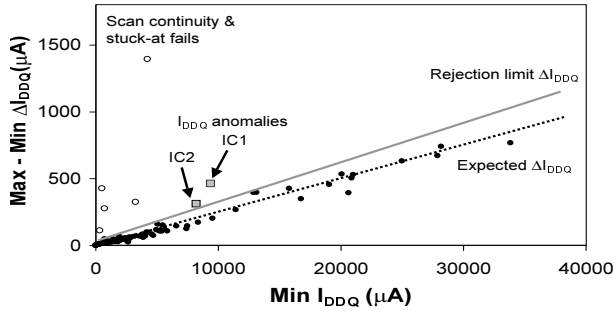


Fig. 8: Relation between the measured off-state current and the delta for good and bad devices. The dotted line denotes the expected delta and the grey line the rejection limit. IC1 and IC2 are two devices that pass stuck-at testing but fail the ΔI_{DDQ} test.

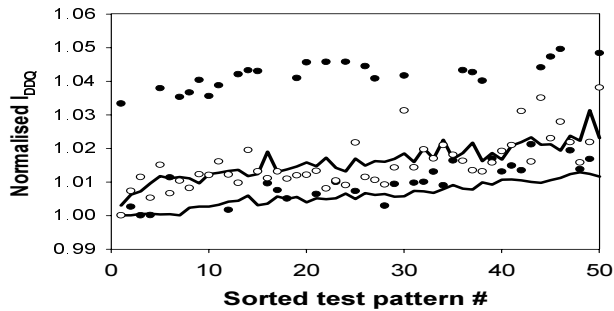


Fig. 9: Minimum I_{DDQ} normalised results for IC1 (solid circles) and IC2 (open circles). The black lines denote the range of expected values.

investigation revealed that this is not the case and just the effect of state dependencies, intra-die variations and measurement inaccuracies. Therefore the spread as observed for pattern 49 is probably a better indication of the kind of margins required during production testing.

Figure 8 shows the expected delta as a function of I_{OFF} . This behaviour is very similar to the observations in Figure 4 for a 0.18 μm technology. The black dotted line denotes the expected delta. The grey line marks the ΔI_{DDQ} rejection limit and includes a margin for intra-die variations. Several devices with off-state currents below 5 mA show ΔI_{DDQ} anomalies. These devices either fail scan continuity or stuck-at testing. The two devices marked as IC1 and IC2 pass the stuck-at test but show abnormal ΔI_{DDQ} behaviour. If one plots the observed I_{DDQ} values as a function of sorted test patterns these two ICs indeed show a different behaviour (see Figure 9). Note that in this case the I_{DDQ} values were normalised with respect to the minimum value instead of the average value. Also the minimum and maximum lines of Figure 7 were redetermined for this condition. The reason is merely for the visualisation. The advantage is that all low leakage states of an IC with a defect fall in the same zone as the defect-free ICs' data points. This zone is roughly indicated by the two black lines in Figure 9. If the normalisation

was performed on the average current the low leakage states are below the minimum. IC1 contains an anomaly of 290 μA or 3% of I_{OFF} while IC2 shows signs of a much smaller anomaly. Low temperature measurements, which improve the sensitivity, confirmed that these ICs indeed contain ΔI_{DDQ} anomalies and that IC2 has two high current states of +70 and +150 μA .

In conclusion: for two ICs with off-state currents of 9 mA, ΔI_{DDQ} testing could detect anomalies of 290 and 150 μA . So ΔI_{DDQ} testing is capable of detecting “gross” anomalies, but to detect small anomalies the ΔI_{DDQ} test has to be improved.

4 Delta I_{DDQ} improvements

4.1 Introduction

Both ICs with an anomaly could be detected with ΔI_{DDQ} testing, however, they contained gross anomalies. It is a much harder task to detect smaller anomalies. Improvements are required to achieve this for off-state currents of 10 mA or more. Several improvements are still possible. For example reducing the temperature strongly reduces the sub-threshold current. Sato *et al.* [14] showed this approach to perform ΔI_{DDQ} measurements on a chip that had 1 Ampere of leakage current. But cooling is expensive and even with cooling one will encounter the described problems at a certain moment in time. Therefore it assumed that the ΔI_{DDQ} measurements were performed at the lowest temperature which is at default available during the test. In our case it means that all the improvements are based on measurements made at room temperature or above. (Some low temperature measurements were used in Section 3 but only to confirm the pass/fail limit; this needs to be done only once for a design in a specific process.)

Another option is to increase the number of observation points either by using several on-chip monitors [15] or by using multiple-observation points [16]. Both methods are feasible, however, at the cost of either silicon area or complex measurement equipment and loadboards. Furthermore, more advanced data analysis programs can also improve the detectability. Industry and academia are investigating all these improvements. In this paper two other enhancements for ΔI_{DDQ} testing are investigated and applied to IC1 and IC2.

4.2 Reduction of activity

The first improvement is related to virtual partitioning. In virtual partitioning one does not separate the power domains physically but only activates the cores one by one. As already noted before, ΔI_{DDQ} testing is only hampered by parts of a circuit that switch state. So by reducing the “activity” we can improve the detection capabilities of the ΔI_{DDQ} test. We applied this approach

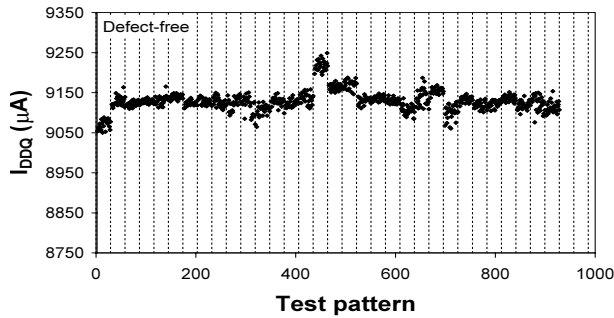


Fig. 10: I_{DDQ} results of a good device for 32 sets of patterns. Vertical lines mark the individual sets

already in ref. [7] were we investigated 6 cores with a joined power supply network. By applying only patterns to one core at a time we improved the detection capabilities. This concept is very easy to use in a core based design. If this is not sufficient one can extend this approach to sub-core level in full scan designs. In deep sub-micron technologies, lay-out tools have to place logic functions physically together to meet timing requirements because the interconnect delay starts to dominate the transistor delay. Furthermore, smart scan-chain routing tools group scan flip flops together [17]. The result is a design in which the logic is controlled on a local scale by a subset of the flip flops. One can therefore test a part of the core while keeping the rest of the core in the same state. The best way to achieve this is with a dedicated ATPG tool that, based on a bridging fault list, can group test patterns for a region “together” and keep the rest of the circuit quiet.

To prove the concept a much simpler approach was used in which the scan chains were “activated” one at a time. To achieve this all 32 scan chains of the core are filled with a fixed pattern except for one for which the original patterns are used. The fill pattern can be any pattern as long as it is kept constant within one set. It is relatively simple to selectively fill scan chains with zeros or ones and in our experiments zeros were used. By doing this the state of a large part of the core remains the same during the I_{DDQ} measurement. In our experiments the 27 first patterns of the original test were used as basic set. The result is 27 times 32 (roughly 1000) measurements. For real usage these modified patterns should be resimulated to determine the expected response and the fault coverage. In our case this was not done since we already know that the two devices contain anomalies which are undetectable with stuck-at testing.

A typical result of a good device is shown in Figure 10. The result should be handled as 32 independent sets of ΔI_{DDQ} measurements. The vertical lines mark these sets. Jumps of up to 200 μA occur between sets but this is not relevant anymore since we handle each set independ-

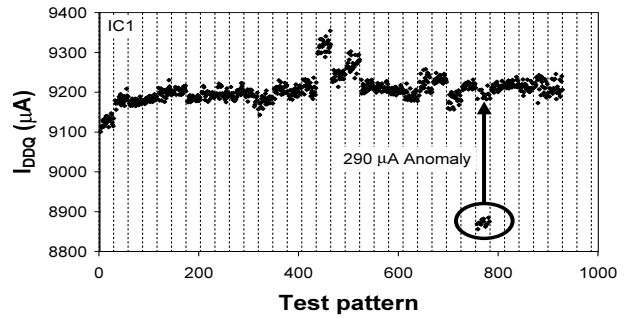


Fig. 11: Results for IC1. The ellipse marks the low leakage state present in set 27.

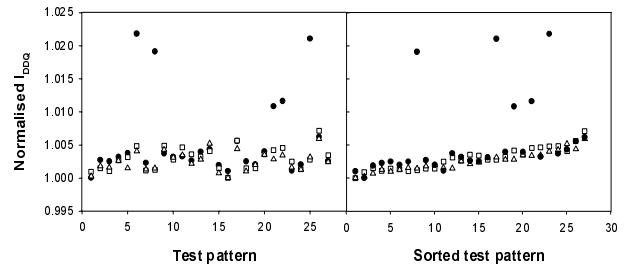


Fig. 12: Normalised I_{DDQ} results for set 15 for IC2 (solid circles) and two reference devices (open symbols). The left-hand side shows the original order, the right-hand side the sorted order.

ently. The typical variations in off-state current per set are now 50 μA or less and consist again of a state dependent part and an intra-die part. The spread is much smaller than when all scan chains are activated (typical spread 250 μA). The improvement with a factor 5 is in surprisingly good agreement with the expected factor of $\sqrt{32}$.

Figure 11 shows the result for IC1. Set 27 is the only one which affects the anomaly. Apparently the defect is activated if we fill scan chain 27 with zeros and therefore all sets show elevated I_{DDQ} values except for set 27 which also deactivates the defect. The separation between good and bad behaviour is much better than what one observed in Figure 9.

Also for IC2 we only have one set in which the defect is activated/deactivated. In this case the fill pattern results in a deactivation of the defect except for set 15. Figure 12 shows the normalised results for this set for IC2 and two reference ICs. The impact of the defect is the same as for the original patterns, i.e. 2% of I_{OFF} . The big difference is now that the variation as function of the test pattern is reduced to 0.5% instead of 2% (compare Figures 9 and 12). Therefore, it is much easier to distinguish the high leakage states.

The nice thing about this approach is that all tricks that one can use to improve ΔI_{DDQ} testing in general can also be applied to sub-core testing. For example, one can reduce the impact of state dependencies as described in Section 2. The improvement one can achieve is shown in

the right-hand side of Figure 12. This data is the same as the left-hand side but now the patterns are sorted. This figure also shows that not only the state-dependent component is reduced with a factor of 5 but also the intra-die component. This reduction makes it indeed possible to detect 5 times smaller anomalies.

This example shows that the method works in practice. The approach of using only one scan chain at a time does of course cost test coverage. How much depends on the organisation of the flip flops and the logic controlled by these flip flops. If a part of the core is only controlled by one scan-chain the impact on the fault-coverage is the smallest and the reduction in intra-die variation the best. The worst situation is a core where each scan-chain is routed randomly all over the core. The reduction in intra-die variation is smaller and the fault coverage for defects can be strongly reduced.

In principle this divide-and-conquer approach can be continued for even smaller units. For example by blanking sections of the scan chain. In the extreme case one can even target one fault at a time to reduce the impact of other parts of a circuit completely. This last approach would make ΔI_{DDQ} testing possible even if transistors leak up to $10 \mu A$ a piece. However, this approach is not feasible for a production test due to the huge increase in test time. Even the present approach with 1000 measurements is only acceptable with a fast ΔI_{DDQ} monitor.

4.3 Scaling of the intra-die component

The problem one faces in ΔI_{DDQ} testing is that the intra-die component in the off-state current is a priori unpredictable. The method described in the previous paragraph is based on the *reduction* of the impact of intra-die variation on the I_{DDQ} measurements. Another way to handle intra-die variations is to *predict* their impact. One option would be to try to correlate variations in one pattern with other patterns. If this is possible then one can predict the impact of intra-die variations for all test patterns on basis of the first patterns. A similar approach was already applied to the state dependency of the Sematech S-121 data [18]. The successfulness of such an attempt strongly depends on the sources of the intra-die variation. If this is only determined by sochastical variation then it is unlikely that such a method will succeed because the variation consists of a million independent components. However, the intra-die component can also depend on slow variations in process parameters across the die, e.g. L_{EFF} , $V_{T,N}$, $V_{T,P}$. It could be possible that methods as described by Bergman *et al.* [18] are suited to predict the impact of these variations on the basis of a small sub-set of measurements.

Another alternative is not to directly predict the variations but to check if the off-state current correctly scales as a function of voltage or temperature. This method is

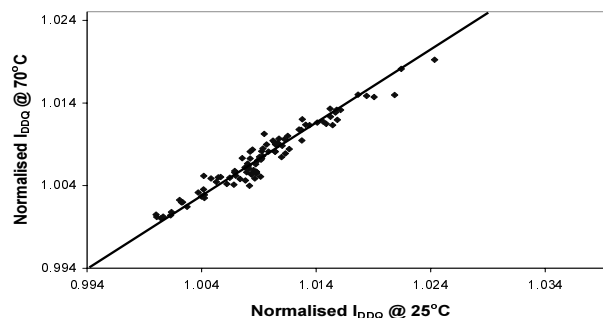


Fig. 13: Normalised off-state current at 25°C versus 70°C for a defect-free device. The line is a guide to the eye.

based on the assumption that one cannot predict exactly the expected leakage current for a specific pattern due to the intra-die variation but that one is capable of predicting its temperature or voltage scaling. This only works if the additional current due to a defect scales differently compared to the off-state current. Luckily, subthreshold currents strongly depend on the temperature while additional currents due to defects are almost independent of the temperature (they scale like I_{ON}). Voltage scaling, however, strongly affects both the off-state current as well as the additional defect current. Therefore temperature scaling is better suited than voltage scaling. Although this method has some similarities with the one proposed in ref. [19] and ref. [12] it is in reality quite different. Their proposal is to determine deviations in temperature scaling for a *group of ICs*. Since the temperature scaling depends on the processing this scaling is not very uniform. In our experience one is at best capable to detect anomalies of about 10% of I_{OFF} and in the experiments in ref. [12] one even uses an anomaly of more than 1000% of the off-state current at low temperatures. Conventional ΔI_{DDQ} testing, with a capability of 1% of I_{OFF} is therefore at least 10 and usually 100 times more sensitive than their approach.

Our approach is an enhancement of ΔI_{DDQ} testing. Instead of using only the normal (low-) temperature measurements one also uses I_{DDQ} measurements at an elevated temperature. These measurements at the elevated temperature are on their own not very helpful since the larger off-state currents make it harder to detect anomalies. In combination with the normal temperature measurement, however, one can detect deviations in the I_{DDQ} behaviour between test patterns applied to a single IC.

The measurements were performed at 25°C and 70°C for 95 test patterns. Figure 13 shows an example of the results for a good device; the data points for this device lay on one line indicating the same scaling as a function of temperature for all test patterns. Figure 14 shows the behaviour for IC2. In this figure we can distinguish three groups of data points. These groups have an offset due to the additional current of the defect. This method

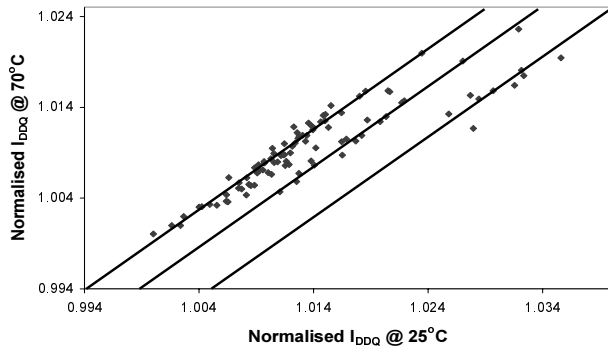


Fig. 14: Off-state current at 25°C versus 70°C for IC2. The three lines denote the three leakage states.

helps to separate the active and the inactive defect states and thereby improves the detectability of anomalies. Although this method helps a bit, e.g. the intermediate state of 70 μ A of IC2 can be distinguished, it is clearly not a very big improvement and typically only a factor of 2 is achieved.

Figure 13 already shows that small deviations from the expected behaviour are present for the good device. The correlation between the 25°C and 70°C measurements is only 0.97. These deviations are small with respect to the off-state current but not to the additional currents we want to detect. One reason the improvement is less than expected is due to our measurement accuracy of 8 μ A above off-state currents of 10mA. This is considerable less than the 1 μ A we have below 10 mA. In principle higher accuracy measurements can overcome this limitation. However, there are two other limitations which are much harder to correct. First, n- and p-transistors scale differently as a function of temperature. Second, the gate-oxide leakage is in a first approximation independent of the temperature and scales therefore differently compared to sub-threshold leakage. In particular gate-oxide leakage can make this method worthless in very deep sub-micron technologies in which this component becomes more dominant. These two factors make the scaling with temperature not completely uniform for all test patterns. To determine their impact we also performed dual temperature measurements for typical ICs. The off-state current of these devices stays below 10 mA at 70°C. Different measurements made at the same temperature are almost identical (correlation coefficients of 0.999) while the correlation coefficient between 25°C and 70°C measurement is comparable to the results for fast processing. This difference is attributed to the non-uniform scaling as a function of test pattern. It might be possible to correct for these two components on basis of leakage current estimators or measurements at multiple temperatures. Future experiments should prove this.

4.4 Summary

Two advanced versions of ΔI_{DDQ} testing were described that cope with the intra-die component in different ways. The first method limits the activity to one sub-core and thereby reduces the intra-die variations in leakage current. This method can be used to detect very small anomalies on top of large off-state currents at the cost of a strong increase in test time. The second method compares the scaling of the off-state current for different test patterns applied to one IC. This method gives a small improvement with respect to conventional ΔI_{DDQ} testing as described in Section 3.

5 Delay fault testing and very-low voltage testing

5.1 Introduction

In section 2 we showed that a current-based test is the most sensitive class of tests for detecting resistive shorts. Although current-based testing is hampered by the increase in off-state current it is also clear that many improvements are still possible. In section 4 two of these improvements were described. These and other improvements extend the life of current-based testing but it is also clear that it becomes more complicated. All solutions require a combination of sophisticated equipment, complex data analysis and more test time. It is therefore fair to investigate the capabilities of alternative methods such as delay-fault testing and very-low voltage testing (VLV) and determine if these methods could have been able to detect the defects in the two ICs with an I_{DDQ} anomaly.

5.2 Delay-fault testing

Delay-fault testing is not a very attractive method for the detection of resistive shorts as was shown in Figure 1. Only for a narrow resistance range of 1 to 3 $\times R_{crit}$ one expects to observe delays and even in this narrow range the additional delays are typically less than 100 ps in static CMOS designs. Therefore it is unlikely that the two I_{DDQ} anomalies of Section 3 can be detected with delay-fault testing. However, delay-fault measurements are required anyway so no additional test time is needed.

The DUT contains paths with a long logic depth, and therefore a per-path delay-fault measurement was performed. This prevents masking of small additional delays in short paths. This method allows us to detect additional delays of 200 ps or more. None of the paths showed these kinds of additional delay at the nominal supply voltage of 1.2 V. This confirms the simulations that predict that in general one cannot detect resistive shorts with delay-fault testing. Although delay-fault testing may perform better for circuits with short logic depth and speeds in the GHz

range or which use dynamic logic.

5.3 Very low voltage testing

Very low voltage testing is a much more attractive method to detect resistive shorts. The group of McCluskey showed [21]-[23] that by reducing the supply voltage one becomes more sensitive for a wide variety of defect classes. One of those classes is resistive shorts. The sensitivity of VLV testing strongly depends on the reduction in supply voltage. In previous experiments [20] we showed that at a supply voltage of 0.65 V ($1.5 \times V_T$) a Boolean test became more than 5 times as sensitive. However, even with this setting VLV testing could only detect 15% of the ΔI_{DDQ} anomalies. Especially anomalies in the 10-100 μ A range are hard to detect with VLV testing and typically VLV testing has not the sensitivity of ΔI_{DDQ} testing.

Figure 15 gives an schematic view of test conditions and the performance of a device. On one hand one can recognise test conditions *A* (relaxed timing conditions often used for “stuck-at” testing) and *B* (delay-fault testing) which are performed at the nominal supply voltage and on the other hand test conditions that are applied at a strongly reduced supply voltage, i.e. *C* and *D*. In ref. [20] we distinguished two kinds of VLV testing: VLV testing with critical timing and VLV testing with non-critical timing. These conditions are denoted with *C* and *D*, respectively. At condition *D* one is more sensitive for shorts than for condition *C* at the cost of a reduced sensitivity for delay-faults.

5.4 VLV testing with critical timing

The delay-fault test was applied at supply voltages of 1.0, 0.8 and 0.6 V. Only at 0.6 V additional delays were detected for IC1. IC2 did not show any additional delay at either 1.0, 0.8 or 0.6 V supply voltage. This matches the expected behaviour for shorts. The impact of a short is negligible until the supply voltage drops below an IC-specific value which is determined by the resistance of the defect and the driver strengths of the involved transistors. Although one IC could be detected it is not very convincing especially since the conditions are very close to those applied in VLV testing with non-critical timing (see below).

5.5 VLV testing with non-critical timing

Very low voltage testing can also be performed with non-critical timing. Non-critical timing indicates that an IC is likely to pass the same test if the cycle time is reduced with say 50%. Typical conditions for VLV testing with non-critical timing are marked with *D* in Figure 15. These conditions are typically determined by using a fixed cycle time and then measure for a large sample set at which supply voltage each device fails. The thus obtained

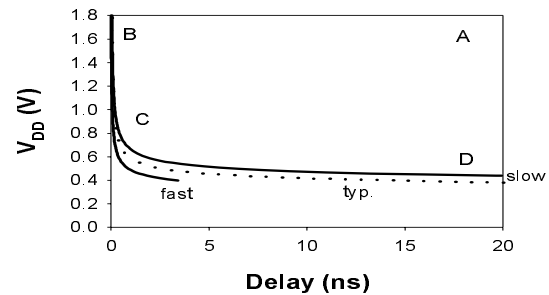


Fig. 15: Simulations of delay versus V_{DD} of a short inverter line for three types of processing. *A*, *B*, *C*, and *D* mark different test conditions.

minimum required supply voltage is increased with a safety margin to cope with process variations and is subsequently used in the actual test. Since the speed is less important one can use both delay-fault patterns and stuck-at patterns.

As a reference set, ICs with off-state currents of 5 mA are used. All these ICs fail between 0.49 and 0.50 V at a cycle time of 250 ns except for our two ICs with a ΔI_{DDQ} anomaly. Those ICs fail at 0.56 V and 0.53 V. A VLV test at a supply voltage of 0.52 V can distinguish both groups. Therefore, VLV testing is in principle capable of detecting the anomalies. However, the test conditions to achieve this are very specific for this set of devices with fast processing and a low V_T . The proposed test voltage of 0.52 V includes a very small safety margin for fast processing but no margin for typical or slow processing. Moreover, ICs with slow processing will always fail the test. Although this makes VLV testing a bit harder, it certainly does not make it impossible. One can adjust pass/fail limits on basis of performance or neighbourhood [13]. Furthermore, the detectability can be improved by using even lower supply voltages (and longer cycle times). Whether such a reduction in supply voltage for a specific design is really feasible strongly depends on which cells or cores determine the minimum operational speed. If other parts already start to fail at 0.6 V, both I_{DDQ} anomalies would have been undetectable with VLV testing. Furthermore, certain parts can require minimum clock speed, e.g. dynamic logic. Another disadvantage of VLV testing is that the technology scaling is not favourable for this method (although it is even worse for I_{DDQ} testing). The improvement in detection capabilities depends on the reduction in supply voltage in relation to the threshold voltage and the nominal supply voltage. The nominal supply voltage, expressed in units of threshold voltage, reduces with advancing technology nodes. For example some low power technologies already use a nominal supply close to $2 \times V_T$. This leaves very little room for exploiting VLV testing. Although there are no objections to perform VLV testing, it is certainly not a

easy task to outperform ΔI_{DDQ} testing. VLV testing is therefore not a real replacement for ΔI_{DDQ} testing.

6 Conclusions

Delta I_{DDQ} testing is hampered by intra-die variations. These variations scale with the off-state current and make ΔI_{DDQ} testing senseless for single cores with an off-state current of 100 mA or more. The capabilities to detect resistive shorts start to deteriorate even sooner. Two enhancements for ΔI_{DDQ} testing are presented in this paper. The first modification confines the activity to a localised part of the DUT and therefore reduces the impact of intra-die variations. In principle this modification allows one to effectively test cores with huge off-state currents although at the cost of a substantial increase in test time. The second modification predicts the scaling of intra-die variations as a function of temperature. This modification only gave a modest improvement of a factor of 2 in detection capabilities in our experiments. It is expected that more sophisticated data analysis will improve the capabilities of this method. However, there are some doubts how well this method can cope with gate-oxide leakage.

The investigated enhancements allow one to detect anomalies of less than 20 μA on top of 10 mA off-state currents. These kind of anomalies are undetectable with delay-fault testing and very hard to detect with VLV testing. For example, the gross anomalies in our test chip of 290 and 150 μA are barely detectable with VLV testing. It is therefore doubtful if smaller anomalies could have been detected.

Although it is clear that the detection of resistive shorts with a current-based test becomes harder and more costly in very deep sub-micron technologies, it is also clear that a current-based test still has the highest sensitivity of the available test methods. The described enhancements and others will allow us to continue to use current-based tests in very deep sub-micron technologies.

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