

# Circular BIST testing the digital logic within a high speed Serdes

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## **Abstract**

*High Speed Serializer Deserializers (serdes) are traditionally tested using functional BIST. This paper presents an improved BIST for testing the digital part of a serdes using circular BIST.*

## **I. Introduction**

The purpose of this paper is to address the manufacturing test of the digital part of an ASIC high speed Serializer Deserializer. This serdes contains both analog and digital cmos circuits which run with data rates up to 3.2 Gbps and clock frequencies up to 1.6 GHz. Combined with these high frequencies is the high integration levels with up to 128 receiver/transmitter pairs found on some designs.

The manufacturing test of such designs is performed with digital testers whose capacity falls short of the required data rates by some 2 to 3x. This can be overcome by connecting receiver and transmitter pairs together externally on the test fixture and running short functional at-speed data streams from the transmitter to the receiver. This is commonly called external loopback test [1].

On the present serdes the external loopback test is a functional BIST test whereby pseudo-random bit streams are internally generated and transmitted by the transmitter. The receiver processes the

incoming data and compares it with that expected for the particular fixed sequence of pseudo random bits. Being a BIST test it is straightforward to run. Also it is practical to run this test simultaneously on the many serdes receiver/transmitter pairs of an ASIC.

Whilst external loopback test provides an at-speed manufacturing test of the serdes it is a functional test. It is well known that the fault coverage of functional tests is not high unless much effort is expended in fault grading and the laborious hand generation of many targeted functional tests. The low grade of the current serdes external loopback test was confirmed and that led to the need to improve the test coverage of the digital part of the serdes.

The digital part of the serdes has several key characteristics that determine any approach to test. Firstly there are only several thousand nand gate equivalents. Secondly the logic is running at clock frequencies of 1.6Ghz and 400Mhz. The 1.6GHz frequency is pushing the limit of the currently used ASIC silicon technology. Thirdly, combined with these high clock frequencies is the fact that the low frequency clock is a derived clock. Finally the logic is bound on one side by pure analog circuitry, which severely curtails observability. These characteristics led to the decision to use a circular BIST approach for testing the digital logic.

In section II the serdes architecture is described together with the external loopback test and its effectiveness. Section III describes the requirements for testing the digital logic and discusses the options available providing the reasons for using circular BIST. Section IV describes the serdes circular BIST implementation and results. Finally, conclusions are presented in section V.

## II. The Serdes and its loopback test.

The serdes are a set of 0.13 micron silicon Serializer Deserializer ASIC IO macros that run at up to 3.2Gbps data rates. There are five macros:

- bi-directional pair comprising one transmitter and one receiver.
- 4 transmitter macro.
- 4 receiver macro.
- 8 transmitter macro.
- 8 receiver macro.

For simplicity only the bi-directional macro will be addressed in this paper. The other macros have identical architectures.

Figure 1 shows the overall architecture of the macro. The shaded blocks are analog circuits, all others are digital logic.

8 or 10 bit parallel transmit data comes from the ASIC core via bus Td, it is serialized in the Parallel2Serial block utilizing the 1.6GHz PLL clock via the Tx phase interpolator. Finally it is transmitted out of the chip via the differential output Tx.

Differential serial input comes into the chip at Rx. The receiver function must sample the high-speed incoming serial data and align with its variable rate. It does this using the 1.6GHz PLL clock and the feedback loop comprising the following blocks:

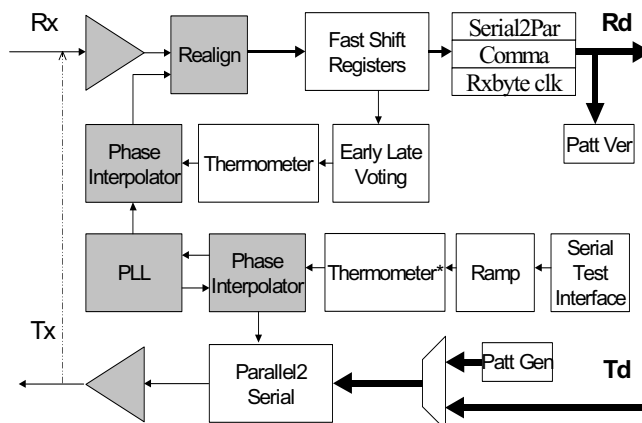


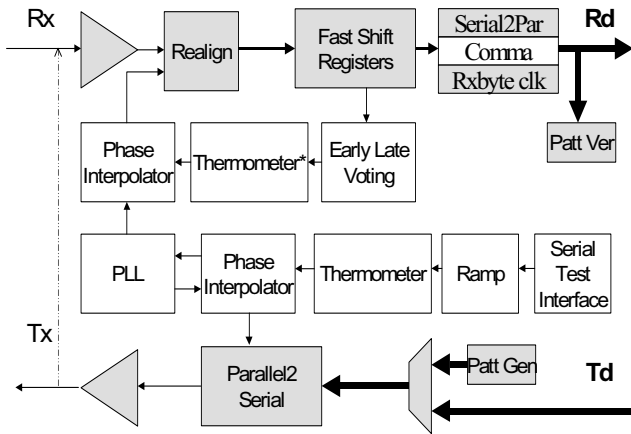
Figure 1: Serdes Architecture

- Realign
- Fast Shift Registers
- Early Late Voting
- Thermometer
- Phase Interpolator

Once aligned the data is essentially captured together with an aligned 1.6Ghz recovered clock. The data is finally parallelized and sent to the ASIC core via bus Rd together with the corresponding divided down 400Mhz recovered clock. In 10-bit mode, a comma detect function is available to aid with byte alignment. These latter functions are performed in the Serial2parallel, comma and Rxbyte clk blocks.

The serial test interface block is a test access port which is used for applying manufacturing tests, for utilizing a bounding scan chain for ATPG purposes and for debug, either directly, or utilizing 1149.1 jtag control of the test scan path.

The serial test interface block is shown controlling the two blocks, Ramp and Thermometer\*. These are used in conjunction with the PattGen and PattVer blocks to perform loopback testing.



**Figure 2:** Loopback Test Data-Path

Loopback testing uses the data-path shown highlighted in Figure 2. The source data is generated by the PattGen block, it can generate three different kinds of data streams;

1. a 400MHz clock pattern.
2. a  $2^7 - 1$  pseudo random pattern.
3. a  $2^{23} - 1$  pseudo random pattern.

This pattern is sent out through the transmitter and back into the receiver. Once sampled and aligned the PattVer block has pattern detecting logic which confirms receipt or not of the correct pattern.

A major functionality of the receiver logic is its ability to align and track with the incoming data. This functionality is partly tested during the loopback test via the Ramp and thermometer\* blocks. These apply a constant frequency offset to the PLL whilst keeping the transmitter path clock frequency at its nominal 1.6GHz value. The result is that the loopback receive data arrives at a constant frequency offset from the PLL clock. This forces the receive logic to use its feedback path to adjust to the offset hence providing some functional test of the feedback path. Various offset values are available from the Ramp block.

Loopback test has a number of benefits,

- Both the analog and digital paths through the serdes are tested.
- The testing is at-speed.
- There is some testing of the alignment and clock recovery logic.

This test is however essentially a functional test and can therefore be expected to have low stuckat coverage of the digital logic.

The serdes macro  $2^7 - 1$  10 bit mode loopback test without ramp was fault graded using Verifault™. Digital logic was modeled as gates and fault graded, Analog logic was modelled with behavioral verilog models and was therefore not gradeable. The fault grades for the mission digital logic blocks are shown in Table 1 together with the relative areas of these blocks.

Block	Relative area	Fault Grade
Fast Shift Registers	6	42.2%
Serial2Par	2	93.5%
Comma	5	14.7%
RxByte clk	3	53.1%
Thermometer	20	17.4%
Early Late Voting	15	15.4%
Parallel2Serial	1	33.4%

**Table 1:** Loopback test grades

Table 1 shows that most of the subblocks have low fault grades, in particular the large blocks Thermometer and Early Late Voting, have very low grades. Whilst these fault grades are for just one of several available loopback tests it is unlikely that the cumulated grades for all loopback tests would provide a high fault coverage.

Actually computing the cumulative grade was not practical due to tool limitations.

### III Improving serdes digital logic test

The main object of this work was to improve the test coverage of the digital parts of the serdes macro. Fault coverage analysis of a typical loopback test highlighted low grades on the two largest blocks Early Late Voting and Thermometer. Since these two blocks data is sourced from the Fast Shift Registers then these three sub-blocks were targeted for improvement. The goals for an improved test are given in Table2.

Goal	Description
G1	Stuckat Fault cover >=90%
G2	Area overhead <= 10%
G3	Test to run at-speed
G4	Test to be easily run
G5	Run on many Serdes in parallel

**Table 2.** Goals of test

The following options were considered:

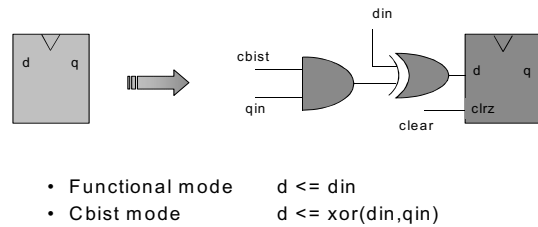
- Functional Test.
- Functional BIST.
- Scan ATPG.
- STUMPS Logic BIST.
- Circular BIST.

Functional Test would require development of customized tests which would be different for every design and would likely attain similar fault coverage's as Functional BIST. Functional BIST has inadequate fault coverage. Scan ATPG has the advantage that a high grade would be attained however some of the logic runs at 1.6GHz and would be difficult to scan insert, the derived 400Mhz clock would need gating and provision of scan access would complicate deployment of the serdes macro. That leaves the two structural BIST options, STUMPS BIST[2] and circular

BIST[3,4]. STUMPS BIST was ruled out because the BIST controller itself would rival the size of the logic to be tested. Also, as with scan ATPG, the clocks would need gating. Therefore, although the authors had not previously used circular bist, it was the obvious choice to try.

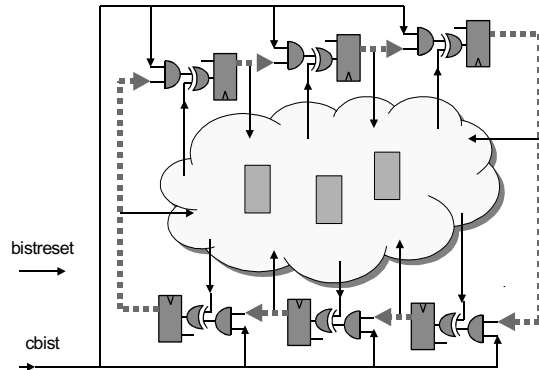
### IV. Circular BIST Implementation

Circular BIST is a structural self test method whereby some of the flip-flops of a design are upgraded with an enabled xor on the D input, see figure 3.



**Figure 3:** Circular BIST flip-flop

When the BIST enable signal is inactive the flip-flop sees the normal functional din input. When the BIST enable signal is active the flip-flop reads the xor of the functional din input together with, typically, the Q output of another circular BISTED flip-flop. The subset of flip-flops that are converted to circular BIST flip-flops are connected to form a circular path as in figure 4.



**Figure 4.** Circular BIST Path

This BIST is then operated by the sequence

1. Reset all flip-flops.
2. Enable circular BIST mode.
3. Clock for N cycles.
4. Compare values in subset of flip-flops with expected value.

We should mention here that the original cbist implementation in [3] had a slightly more elaborate cbisted dff that allowed for two additional modes other than functional and cbist. These were an initialisation mode and scan shift mode. In the present work a general circuit reset was already available. Also, as already mentioned, scan access was not practical. Finally no facility for diagnosis was considered for the present work.

The main advantages of circular BIST are;

1. It generates one pattern per clock, unlike scan based BIST which generates one pattern per scan.
2. Clocks can be used as-is. Derived clocks are used as if in functional mode and no clock gating is required.
3. BIST control is simple to implement and small in overhead.
4. The BIST test can be run at-speed.
5. Full conversion of functional flip-flops to BIST flip-flops is not required [5].

The main disadvantages of circular BIST are;

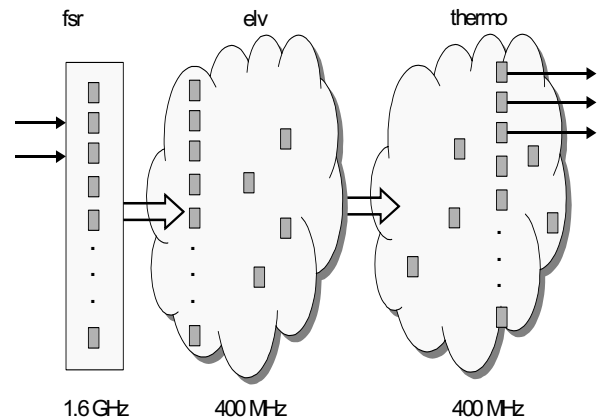
1. Fault grades can be low due to limit cycling [3]. This is where an inappropriate starting state for the circular BIST path leads to the BIST path repeatedly cycling through a limited number of states.
2. Fault grades can be low due to the register adjacency problem [6]. This is where adjacent cells in the BIST path have the property that the output of the first cell is in the functional input cone of the second. The result is that the xor

gate of the second cell can always output zero and hence block fault propagation.

3. Despite several university and proprietary automations of BIST insertion [3,7,8] a commercially available tool does not exist. This means a manual implementation is required.
4. Fault grades must be obtained using slow sequential fault simulation.

Along with these specific disadvantages, circular BIST shares the requirement of all embedded BIST that inputs be bound for controllability and outputs bound for observability.

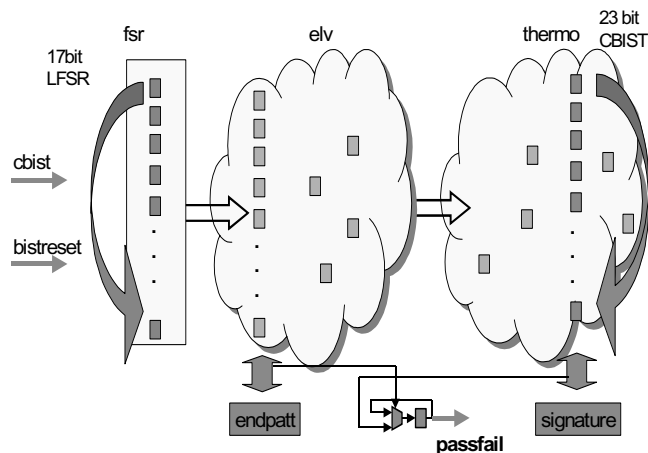
The small size of the serdes digital logic and certain of its features mitigated the disadvantages of circular BIST making it a practical option.



**Figure 5.** Target blocks for BIST

The three blocks to be BISTed are shown in figure 5. Certain properties of these blocks lead naturally to some of the BIST implementation details. The main data-flow is from the Fast Shift Register, through Early Late Voting to the Thermometer block. This led naturally to a BIST approach where the Fast Shift Registers provide the source of the pattern data and the

thermometer block is the pattern destination. The actual BIST implementation is shown in figure 6.



**Figure 6.** Circular BIST Implementation

The Fast Shift Register block is mainly composed of a shift register, and whilst it runs at the high speed of 1.6GHz, there is enough timing slack to enable it to be configured as a 17bit Linear Feedback Shift Register during circular BIST mode. This LSFR sourced the pattern data.

None of the 20 early late voting logic flip-flops were touched.

All 23 of the Thermometer flip-flops were converted to a circular BIST loop providing both pattern source and pattern destination. This loop of circular BIST registers was used to accumulate the BIST result signature.

Finally two comparators were added. One comparator monitors a register within Early Late Voting triggering on a unique signature. The signature chosen was that attained by the register at the last cycle of the BIST test. The other comparator monitors the values of the BIST registers for the ending signature.

BIST operation then comprised of resetting the flip-flops, putting the logic into circular BIST mode and running for a fixed number of clock cycles. At the end of operation the outputs of the two comparators set the sticky bit of a test register to pass or fail.

The whole implementation was performed manually on the Verilog RTL design description. Both RTL and gate level simulation were performed to validate the circular BIST operation, then Verifault™ fault simulation was performed to assess the achieved fault grade. The normal operation of the BIST allows monitoring of only the sticky bit and fault grading under this constraint took approximately 3 hrs. However during BIST development the whole loop of circular BIST flip-flops could be monitored to provide a good estimate of the overall grade and reducing the fault simulation time to a more practical one minute.

The number of cycles for the BIST operation was selected by observing the knee in the fault grade verses clock cycle curve, 1200 of the 400MHz clock cycles were optimum.

Initial fault grades were in the mid 80% range. Here design knowledge and experimentation were used to increase the grade. Low BIST grades are often caused by controllability and observability problems.[9] Observability experiments could be made by simply adding probe points during fault simulation. Controllability experiments required changes at the RTL level and re-synthesis prior to re-simulation. Control points were inserted by xor'ing in pre-existing non static signals into a static signal. Observe points by xor'ing the required signal into a pre-existing flip-flop. Two control points and one observe point were added to the logic producing a fault grade above 90%.

Goal	Description	Result
G1	Stuckat Fault cover >= 90%	93%
G2	Area overhead <= 10%	7%
G3	Test to run at-speed	Yes
G4	Test to be easily run	Yes
G5	Run on many Serdes in parallel	Yes
N/A	Implementation time	1 Person Month
N/A	Silicon runtime	4 $\mu$ sec

**Table 3.** Results

The results of this work are given in table 3 and indicate that the goals set out in table 2 were met.

The implementation was successful despite being performed manually. This is ascribed to the following;

- The blocks were naturally bound by registers. The input registers became the LFSR and the output registers part of the circular BIST loop.
- Control inputs were few and only one required bounding to avoid grade loss due to a stuck value.
- Configuring the input register as an LFSR rather than a circular BIST loop reduced the problem of limit cycling.
- Register adjacency was avoided by both the nature of the logic inserted and by manual selection of the circular BIST path order.
- A reasonable grade was obtained through test point insertion.

## V. Conclusions

Circular BIST has been used successfully to test the digital logic of a high-speed serdes macro at speed. Circular BIST provided an at speed structural test with a

fault coverage of 93% and a gate overhead of 7%. Whilst implementation was fully manual and required sequential fault simulation the small size of a few thousand gates made this a practical proposition.

## ACKNOWLEDGEMENTS

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