

AC IO Loopback Design for High Speed uProcessor IO Test

Benoit Provost*, Tiffany Huang**, Chee How Lim*, Kathy Tian**,
Mo Bashir*, Mubeen Atha**, Ali Muhtaroglu*, Cangsang Zhao**, Harry Muljono**

Intel Corporation. Hillsboro, OR, USA *
Intel Corporation. Santa Clara, CA, USA **

Abstract

This paper presents the next generation AC IO Loopback design for two Intel processor architectures. Both designs detect I/O defects with 20 ps resolution and 50 ps jitter for up to 800 MHz bus speed. Even though the implementations differ in some aspects to accommodate two different bus architectures, the same prudent considerations for high speed operation, minimum test inaccuracy, and low implementation costs apply to both.

1. Introduction

Microprocessor bus speeds have increased significantly in the recent years to fulfill large bandwidth demanded by applications. This presents a growing challenge to the AC I/O parametric testing. Traditional AC I/O tests use an Automatic Test Equipment (ATE) with a standalone processor as the device-under-test (DUT). The test precision is limited by tester's Edge Placement Accuracy (EPA), which varies from tester to tester, resulting in test limits which are much tighter than the timing specifications. Consequently, the DUT cannot be tested any tighter without the risk of significant yield loss. Higher speed and lower EPA testers recently developed by tester vendors do not provide a viable solution due to unacceptable manufacturing costs associated with them.

Defect based I/O screens using AC IO Loopback (ACIOLB) [1] Design for Test (DFT) feature have been embraced at Intel as an alternative to traditional functional test methods. In this paper, we will introduce the next generation ACIOLB designs implemented in Itanium® 2 [2] processor on a 130nm process and Pentium® 4 [3] processor on a 90nm process. Both designs use an on-die Delay Lock Loop (DLL) for maximum timing accuracy. Cost effective design considerations, simulation and characterization data are also presented.

2. AC IO Loopback Methodology and Architecture

ACIOLB tests the pad timing by measuring the loop time from the output flop to the input flop through the pad. Figure 1 illustrates a simplified block-diagram of ACIOLB implementation for source synchronous (SS) bus. ACIOLB uses a Pattern Generator, Error Checker and Delay Cell. The data captured by the strobe edges at the receiving latches are compared against expected values and the pass/fail result is generated. The loop time can be stressed by adjusting the strobe timing. In addition, each pad circuit is equipped with its own multi-bit pattern generator to exercise Single-Bit-Switching (SBS), Simultaneous-Switching-Output (SSO), Inter-Symbol-Interference (ISI) and crosstalk conditions.

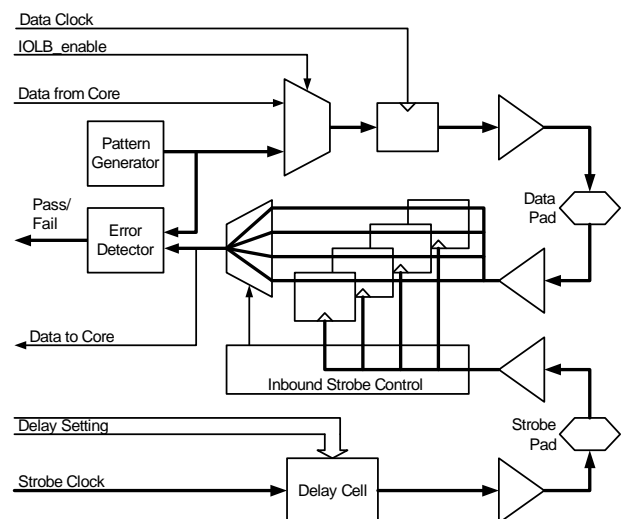


Figure 1 AC IOLB general approach for source synchronous (SS) pads. Bold lines indicate IOLB signal paths.

The I/O loop is exercised with “First Fail” (FF) and “All Fail” (AF) searches in order to capture signal jitter and

pad-to-pad variation. The FF search is used to capture T_{va} (data out valid time after strobe) and AF is used to capture T_{vb} (data out valid time before strobe). Data clock remains unchanged during both searches, and drives data from the pattern generator to the output buffer. Data comparison is preset to pass in the FF search (Figure 2). I/O loop is stressed by gradually pushing the strobe timing using the programmable Delay Cell from its nominal centered position to the point where one of the pads latches the wrong data. For example, one pad will latch data “c” instead of “b” like all other pads in the first cycle depicted in Figure 2. This first failing occurrence is recorded as FF.

Two approaches are possible for the AF search. One approach, shown in Figure 3, is to start the search with the same strobe position as in the FF case, then pull the strobe toward the previous data edge. First failing occurrence is defined as AF. The other approach, shown in Figure 4, is to start the search with strobe centered in the next data cycle, then reduce the strobe delay toward the current data edge. The comparison is made between the current data from pad and the next data from pattern generator. First failing occurrence is defined as AF. The delta between FF and AF determines data timing variation due to clock jitter, repeatability errors and delay cell inaccuracy.

Besides test cost reduction resulting from moving the test from a functional tester to a lower cost structural tester, the test cost is further by decreasing the test time. For the Pentium® 4 microprocessor, ACIOLB test time on a structural tester is 40% shorter than the traditional pad timing test method on a functional tester.

For both Pentium® 4 and Itanium® 2 microprocessors, the silicon area overhead due to additional circuits required specifically by ACIOLB represent approximately 3.5% of the entire pads area.

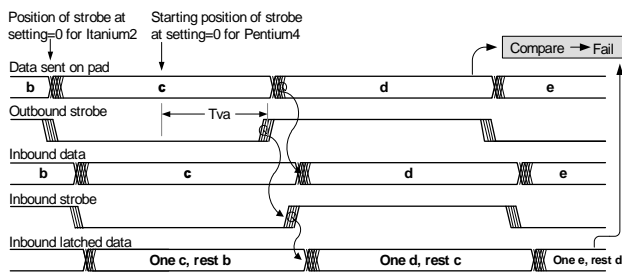


Figure 2 First Fail (FF) Search.

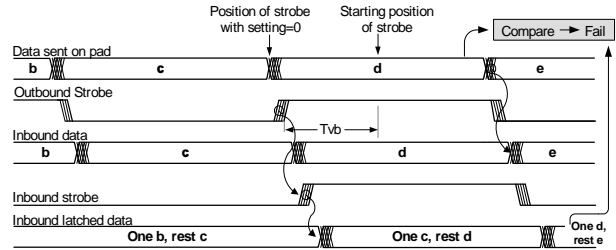


Figure 3 All Fail (AF) Search for Itanium® 2 Processor.

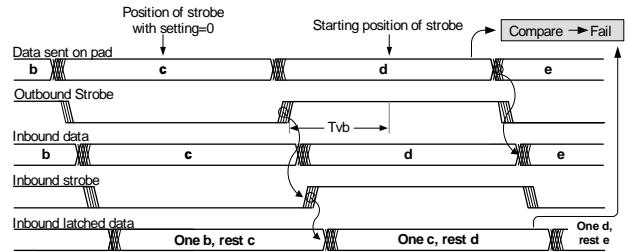


Figure 4 All Fail (AF) Search for Pentium® 4 Processor.

3. Delay Locked Loop Designs

A precise on-chip delay mechanism is necessary to implement the strobe timing adjustments (Delay Cell in Figure 1). The test mode configuration should encompass low complexity with minimal impact to area and schedule. Yet it has to deliver high resolution to meet high speed AC screening requirements. Early implementations of ACIOLB using delay lines made of programmable inverter chains suffered from large process, voltage, and temperature (PVT) variation effects (typically ~2-3X). ACIOLB implementation in both the latest Pentium® 4 and Itanium® 2 Processors’ ACIOLB use self-calibrated delay mechanisms with a centralized DLL circuit.

In this section, two different self-calibrated delay implementations will be described. A central Analog DLL and central delay approach (Figure 5) is used in Itanium® 2 Processor. The central Analog DLL (ADLL) locks to a Phase Locked Loop (PLL)-derived clock and distributes the delayed clock to all pads. The ADLL provides compensation of coarse delay steps and is supplemented by a digital interpolator for fine delay adjustments. Compensation of the coarse delay adjustment against process, temperature and supply variations ensure a reliable and predictable offset between strobe and data. A central Digital DLL (DDLL) and distributed delay architecture (Figure 6) is selected in Pentium® 4 Processor. The central DDLL also locks to a PLL-derived clock, but only a copy of the digital compensation settings is distributed to the pads instead of modified clocks. Each strobe pad contains a Strobe Adjustment Circuit (SAC), which contains a delay line built from the exact copy of

the delay buffers used in the DDLL. The SACs therefore act as slaves to delay the local clock according to the coarse delay control bits. Each SAC also includes a digitally controlled analog interpolator for fine tuning.

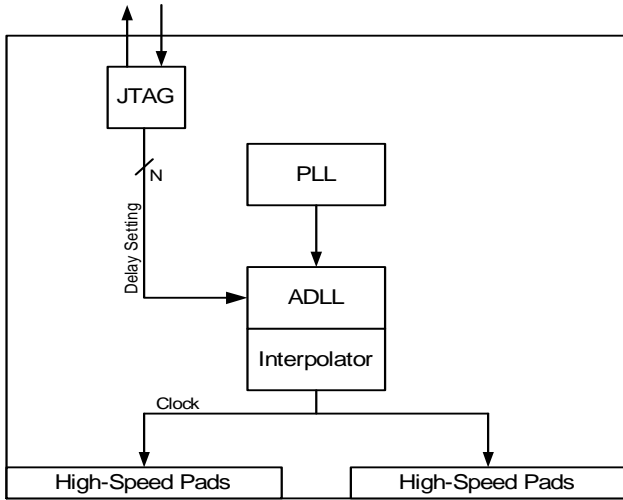


Figure 5 Central ADLL and central delay approach used on Itanium® 2 Processor.

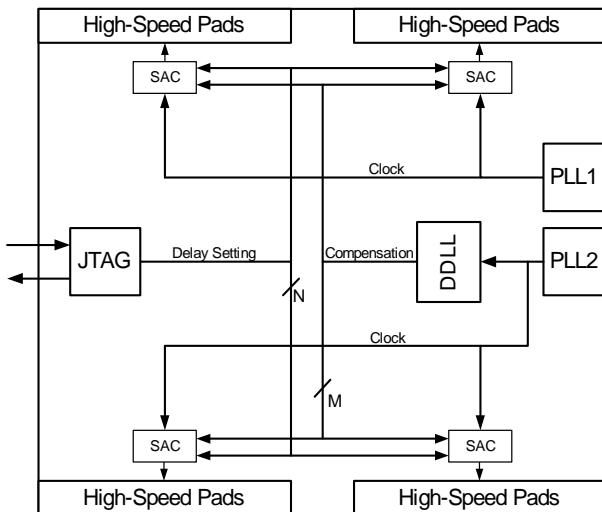


Figure 6 Central DDLL and distributed delay approach on Pentium® 4 Processor.

The fact that local clocks in pads are not all from the same PLL in Pentium® 4 Processor is the main reason for using a master-slave approach. Since Itanium® 2 Processor uses a single clock for all pads, a central delay mechanism is more appropriate. The Itanium® 2 Processor’s approach also allows the use of an ADLL (which benefits from very high resolution) since the compensation settings

do not need to be distributed across the die. On the other hand, using distributed programmable delay cells at the pads in the case of Pentium® 4 Processor adds the flexibility of setting different strobe delay values (and possibly different kill limits) across different pad groups tested in parallel. The Pentium® 4 implementation does not rely on the strobe Delay Cell to center the strobe on the data. Instead, logic circuitry ensures that the strobe is centered when the delay setting on the Delay Cell is set to 0. However, inserting a Delay Cell on the strobe path would result in a mismatch between strobe and data because of the PVT-sensitive timing offset through the delay cell when setting is at 0. The solution is to add a “dummy” delay cell on the data path clock. This dummy delay cell reproduces the offset delay of the strobe delay cell. This ensures that strobes are always perfectly centered on data in normal mode (when the delay setting is at 0).

3.1 Itanium® 2 Processor ADLL and Interpolator Design

Itanium® 2 Processor implemented an analog DLL based on self-biased techniques in order to achieve low jitter operation. Self-biased DLL design eliminates PVT variation dependency and also provides tracking bandwidth over a broad frequency range [4]. The ADLL is isolated from the noisy I/O buffers and is powered by a locally decoupled and filtered power supply to ensure low jitter performance at the clock output.

Figure 7 depicts the block diagram of the ADLL. The circuit is comprised of a phase comparator, charge pump, loop filter, bias generator and voltage controlled delay line (VCDL). The ADLL uses a 400 MHz reference clock (FREF), supplied by the IO PLL. The phase comparator provides up and down signals to the charge pump to charge and discharge the loop filter (VCTRL). The bias generator utilizes the VCTRL signal to generate internal bias voltages for the VCDL.

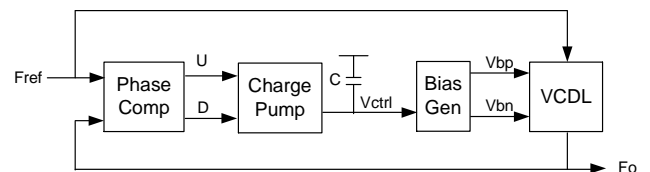


Figure 7 Analog DLL on Itanium® 2 Processor.

The VCDL consists of multiple stages of delay cells, as shown in Figure 8. The delay cell comprises of a source-coupled pair with resistor load elements (Figure 9). The internal bias voltages VBP and VBN control the load and tail current respectively. The delay through the VCDL is

controlled by the loop filter, which generates a feedback by integrating the phase error between the reference clock (FREF) and the VCDL output (FO). Once in sync, the VCDL then delays the reference clock by a fixed amount until there is no phase error detected between the reference and output clocks. By referencing internally generated bias voltages, the VCDL can be adjusted to provide accurate double-quad phases, which are then delivered to the interpolator stage. For 400 MHz operation, each phase is spaced by 312.5 ps.

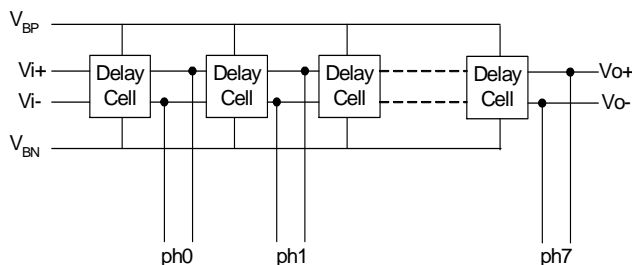


Figure 8 VCDL on Itanium® 2 Processor.

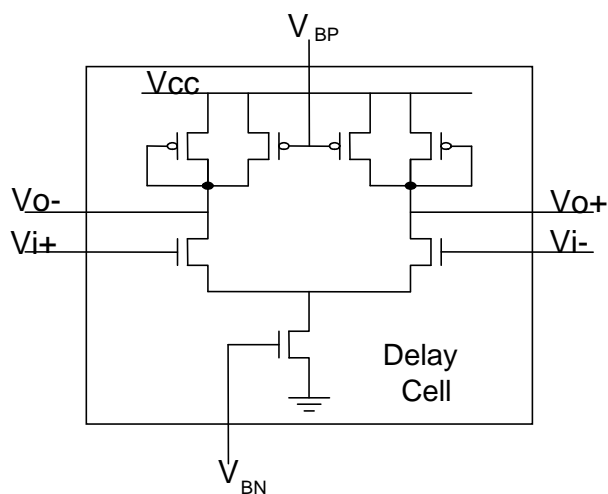


Figure 9 Differential Buffer Delay Stage on Itanium® 2 Processor.

A digital interpolator is used to further refine these clock edges to generate 16 new phases of ACIOLB clocks per ADLL phase, resulting in a 19.5 ps final step size [5]. An innovative digital interpolator, shown in Figure 10, was developed that exhibits low non-linearity characteristics, low power consumption and ease of design [6]. The interpolator is also PVT compensated and has a wide dynamic frequency range suitable for ACIOLB operation.

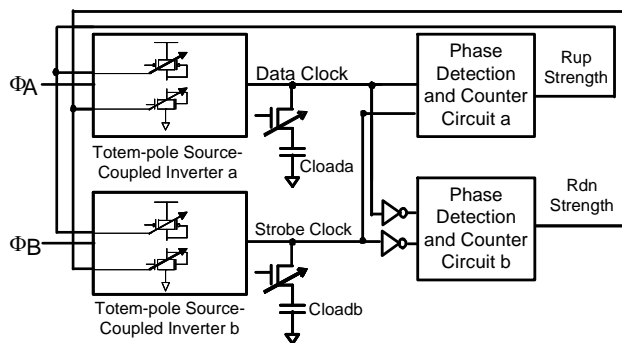


Figure 10 Digital Interpolator on Itanium® 2 Processor.

The interpolation process involves clock propagation through an RC network. The resistor is constructed from a source-coupled transistor pair that exhibits linear resistance characteristics. Each pair can be individually turned on and off by a calibration circuit using Rup and Rdn signals. The capacitors Cloda and Clodab consist of multiple legs of capacitive devices with each leg adding one additional phase step to the overall timing delay. During calibration, the upper capacitors are all selected and 0-degree clock (Φ_A) is fed in. The lower capacitors are deselected and 45-degree clock (Φ_B) is fed in. The resistor pairs are then switched on and off by the phase detection and counter circuit, until phase skew is 0. After calibration, 16 legs of capacitive devices are equivalent to 45 degrees of phase delta. During interpolation, the Cloda value always defaults to 0 and the Clodab value can be loaded to generate desired timing.

3.2 Pentium® 4 Processor DDLL and Delay Cell Design

The central DLL and distributed delay approach used in the Pentium® 4 Processor necessitates the distribution of the compensation setting bits to each of the strobe pads. A Digital DLL (DDLL) is preferred over the ADLL implementation as it bypasses the requirement of routing analog compensation bits across the die. The central DDLL uses a conventional technique [7,8], as shown in Figure 11. In this design, the reference clock is derived from an I/O PLL generating an 800 MHz, 50% duty cycle clock. As part of the effort to reduce area, a total of 4 delay buffers (DB) are used in the delay line to match the 625 ps high-phase, instead of using 8 buffers to match 1.25 ns. Thus, each DB is 156 ps. The phase detector (PD) is a D-flip-flop, tuned to have low offset for rise-fall comparisons. The digital filter and counter are used to provide a stable set of compensation bits. Finally, a digital lock detector monitors the binary output (up/dn) of the phase detector. A symmetric up/dn behavior over a series 16 cycles is the criteria for lock signal assertion.

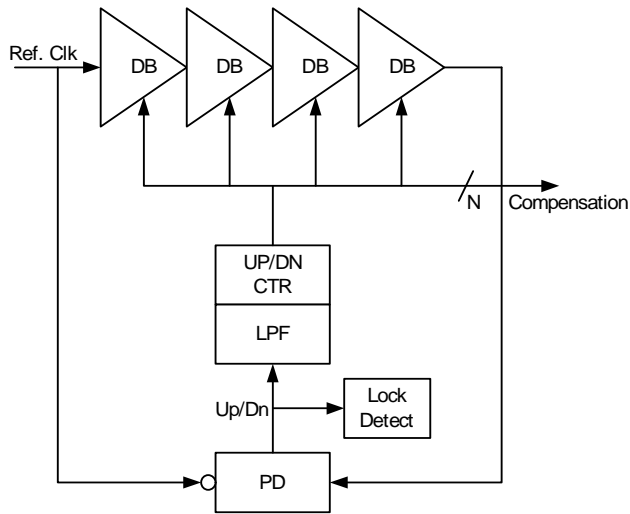


Figure 11 DLL Used in Pentium® 4 Processor.

The core of the DLL design is the delay cell. Temporal and spatial differences in supply voltages could severely degrade the master-to-slave delay matching, leading to large offsets. One approach to design a programmable delay cell would be to add a digitally-controlled capacitive load to the delay buffer. This approach allows the distribution of the digital compensation settings across the chip, but the delay variation versus compensation setting over a wide range is non-linear.

To improve delay range and resolution while enjoying the robustness and simplicity of the digital scheme, a dual-control delay buffer is proposed. Three key observations led to this design:

1. To achieve wide range and high resolution, both the drive current and the load capacitance should be adjusted.
2. If the same control bits are used for both current and capacitance adjustments, delay range can be wider for a given number of bits, compared to a typical binary-weighted capacitive load-only scheme.
3. The current and capacitance adjustments compensate each other such that the delay resolution is close to the ideal resolution for a given number of bits.

Figure 12 shows the dual-control delay buffer [9]. In this implementation, capacitor switching is replaced by an RC circuit in which the resistor is made of binary-weighted pass-gates. To meet the 800 MHz I/O test specification, a 5-bit control is used which achieves 4-4.6% resolution over the entire range. In a conventional binary scheme, the resolution would significantly degrade (>30%) at either the lower or higher values of the compensation

setting range, depending on whether it is current or capacitance based.

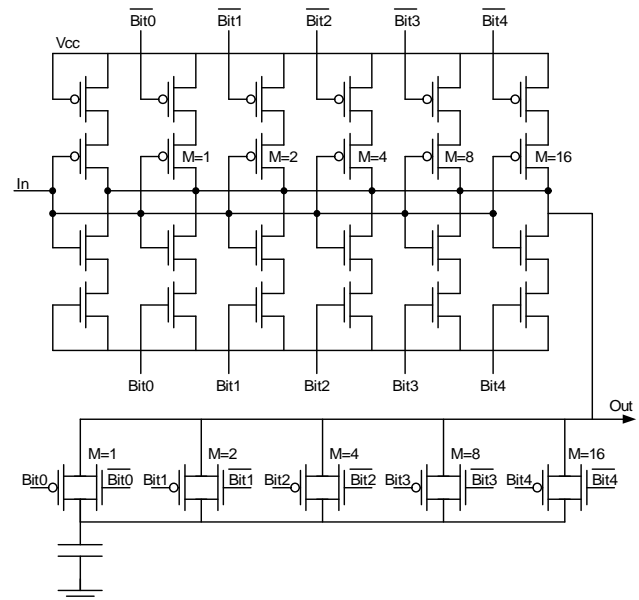


Figure 12 Delay Buffer (DB) on Pentium® 4 Processor.

The simulated delay range and resolution for the design target of 156 ps, showed appropriate delay range coverage, with a resolution of approximately 4% of the total range, across PVT.

The strobe adjustment circuit (SAC) in Figure 13 provides 2.5 ns (2 I/O clock period) range using a combination of 4-coarse and 3-fine select bits. The coarse select bits select one of the 16 buffer outputs in 156 ps steps, while the fine bits select the interpolator configuration to achieve 19.5 ps increments. This multiplexer-based interpolator blends the early and late signal timings to divide the 156 ps block into 19.5 ps increments. Figure 14 illustrates this process. Depending on the fine select bit settings, the slope of the RC discharge curve will vary and affect the time at which the “mixed” node crosses the output buffer threshold. An analog interpolator is chosen for its simple implementation and no calibration requirements.

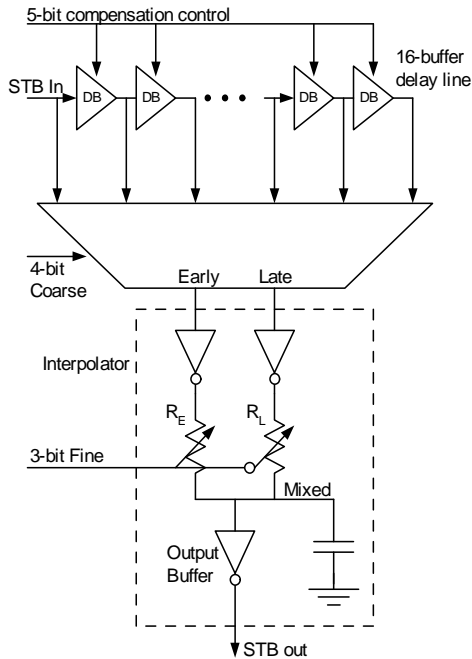


Figure 13 Srobe Adjustment Circuit (SAC) on Pentium® 4 Processor.

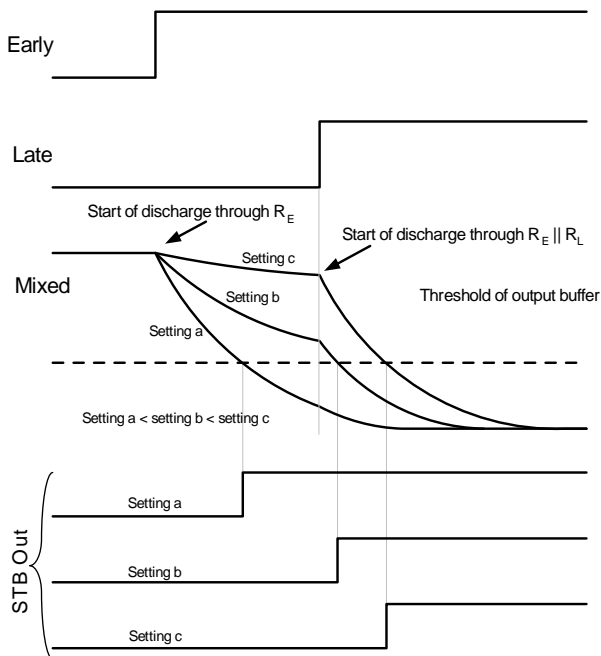


Figure 14 Pentium® 4 Processor Interpolator Timing.

The use of the master-slave approach requires delay buffers to be sized such that they are insensitive to on-die variations. Otherwise, the on-die variations between the master DLL and the slave delay lines will introduce

greater timing uncertainties in the test results. Table 1 shows the results from pre-silicon simulations on the impact of various contributors. It should be noted that the listed percentage represents the contribution of each error source to the total variation, and not the error magnitude itself.

Parameter	800 MHz (8 DB)
Random (V_t and L_{eff})	3.0%
Systematic (V_t and L_{eff})	32.2%
ΔV_{cc} between master and slave	8.5%
$\Delta Temp$ between master and slave	6.2%
LSB Error	50.2%
Total	100%

Table 1 Pareto Chart of Timing Uncertainty Contributors (DB: Delay Buffer).

4. AC IO Loopback Design Validation

System characterizations were performed on Itanium® 2 Processor ADLL and interpolator as well as on Pentium® 4 Processor DDLL and SAC to ensure linear delay steps and low jitter. Figure 15 shows the clock timing at the output of ADLL and interpolator on Itanium® 2 Processor. The graph shows linear delay step size for each programmed delay setting. The step size also did not vary with process skews. This indicates both ADLL and interpolator are able to eliminate PVT variation dependency.

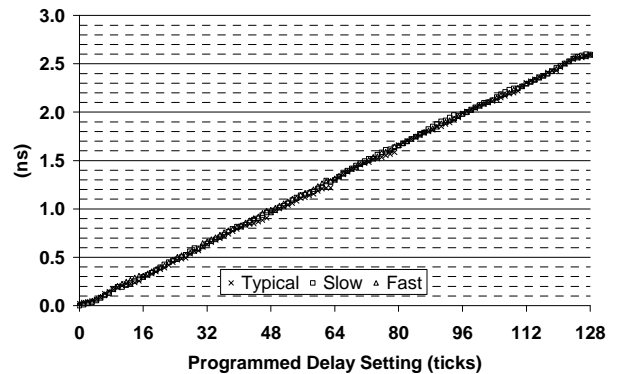


Figure 15 ADLL/Interpolator Linearity Result on Itanium® 2 Processor.

ADLL/interpolator jitter was also measured to determine the accuracy of each programmed delay size. Figure 16 shows the jitter data collected on Itanium® 2 Processor.

The jitter is very small and it spikes up every 16 DLL/interpolator ticks. This points to the interpolator as source of the jitter variation since DLL generates 8 coarse delay steps while interpolator generates 16 fine delay steps between each coarse step. 30 ps is the largest peak-to-peak jitter measured on sampled units. The jitter is not modulated by process skew, indicating robust skew tracking provided by the design. For each DLL/interpolator tick, the total accuracy, or error, is the sum of resolution and worst case jitter, which only totaled 50 ps with DLL/Interpolator running at 400 MHz. This is much smaller than the EPA of Itanium® 2 Processor's current functional ATE tester platform, which is +/- 100 ps for a given tester.

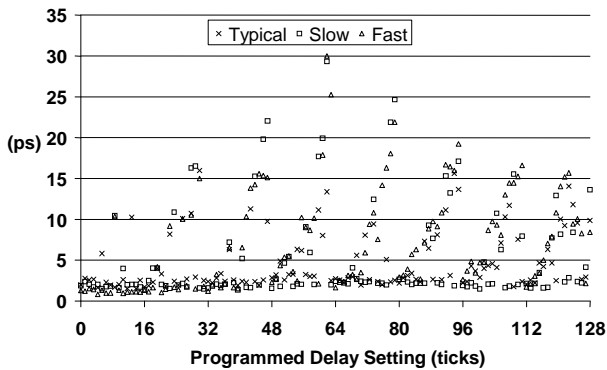


Figure 16 ADLL/Interpolator Jitter Result on Itanium® 2 Processor.

Figure 17 illustrates the delay provided by the SAC once it is compensated by the DDLL on Pentium® 4 Processor. Only a few samples of delay settings within the full range were characterized: 0 to 2, 25 to 40 and 123 to 127. The slope difference between slow and fast data is due to LSB error on the DDLL. Figure 18 shows the delay step jitter for settings 25 to 40. Largest delay step jitter is 34 ps peak-to-peak. Jitter did not vary considerably across PVT. Here again, the step delay jitter is much smaller than the EPA on ATE test platform.

As data demonstrates the DLL, Delay Cell and Interpolator designs are robust for both Itanium® 2 and Pentium® 4 Processors. The resulting delays are predictable and accurate across PVT conditions. The next step in characterization is to collect ACIOLB timing data for First Fail (FF) and All Fail (AF) parameters on all pads.

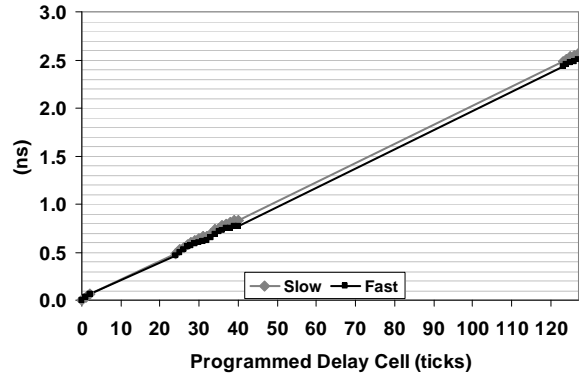


Figure 17 DLL and SAC Delay on Pentium® 4 Processor.

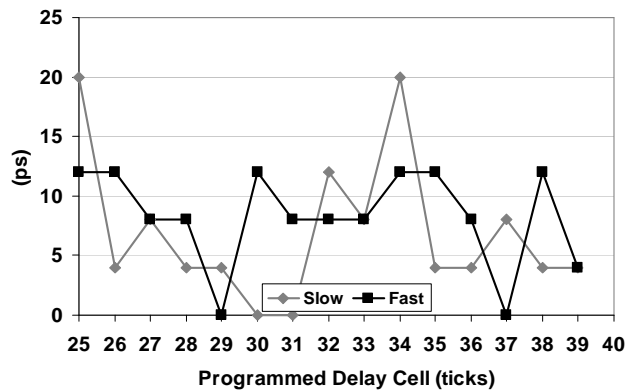


Figure 18 DLL and SAC Step Jitter on Pentium® 4 Processor.

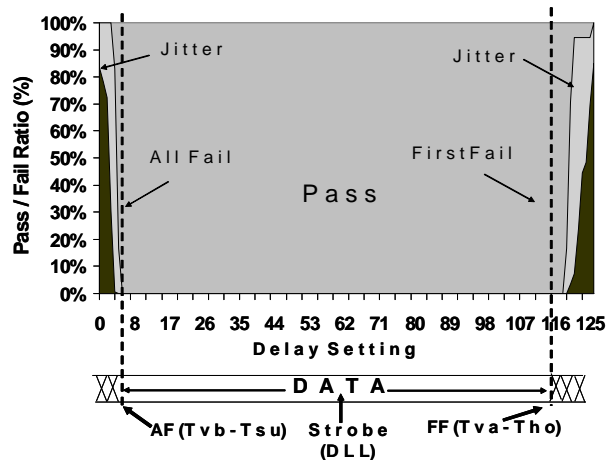


Figure 19 SS ACIOLB Result on Itanium® 2 Processor.

For SS signals on Itanium® 2 Processor, differential strobe pairs are driven by DLL/interpolator-delayed SCLK. The loop time search can also be described as linear shmoo of moving the strobe timing with respect to data, as shown in Figure 19. It also shows the cumulative per pad group search failure percentage. X-axis

represents the Strobe CLK position with respect to Data CLK, in terms of DLL/interpolator delay setting. First Fail and All Fail are achieved by moving Strobe CLK from the center of the DLL/interpolator range toward either end until failure is observed.

Figure 20 illustrates similar results for SS bus on Pentium® 4 Processor. This implementation actually performs the AF timing search by moving to the next cycle and pulling back the strobe, but the results were reformatted for clarity.

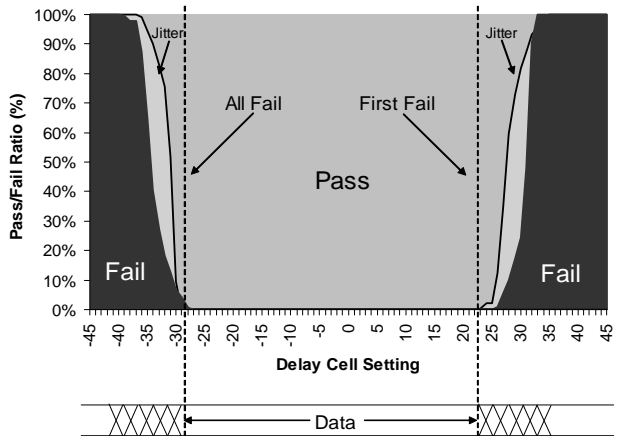


Figure 20 SS ACIOLB Result on Pentium® 4 Processor.

Correlation experiments between traditional functional DV using high speed functional ATE testers and ACIOLB data consistently indicated more margin with accurate ACIOLB DFT testing than with the tester for both Itanium® 2 and Pentium® 4 implementations across 400 MHz to 800 MHz bus speeds.

5. Conclusions

In conclusion, two design approaches for implementing on die ACIOLB were discussed. Both designs achieved better resolution and lower jitter compared to high speed ATE testers, using on-die delay compensation against PVT variations. ACIOLB greatly reduces test costs and is scalable to faster bus speeds.

6. Acknowledgements

The authors would like to acknowledge and thank the hard work and invaluable contributions of Mitsuhiro Adachi, Byron Grossnickle, Hussam Khadder, Kruti S. Pota, Lily Tran, Yanbin Eddie Wang.

The authors would like to specially acknowledge Anne Meixner, T.M. Mak and Mike Tripp for guiding us through initial design stages and providing feedback.

The authors would also like to extend deep gratitude to other members of the Itanium® 2 and Pentium® 4 Processors' design, product and validation teams for their immense support.

7. References

- [1] M. Tripp et al., "Elimination of Traditional Functional Testing of Interface Timings at Intel", ITC 2003.
- [2] S. Rusu et al., "A 1.5GHz 130nm Itanium® 2 Processor with 6MB On-die L3 Cache", IEEE J. Solid-State Circuits, vol. 38, no. 11, pp 1887-1895, Nov. 2003.
- [3] D. Delegates, J. Douglas, B. Kommandur, M. Patyra, "Designing a 3 GHz, 130 nm, Intel® Pentium® 4 processor", Proceedings, 2002 VLSI Circuits Symposium, pp 130-133.
- [4] J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE J. Solid-State Circuits, vol. 31, no.11, Nov. 1996.
- [5] H. Muljono et al., "A 400MT/s 6.4GB/s Multiprocessor Bus Interface", IEEE J. Solid-State Circuits, vol. 38, no. 11, pp 1846-1856, Nov. 2003.
- [6] US Patent 6,650,159, "Method and Apparatus for Precise Signal Interpolation", Eddie Wang and Harry Muljono, 2003.
- [7] B.W. Garlepp et al., "A Portable Digital DLL Architecture for CMOS Interface Circuits", Proceedings, 1998 VLSI Circuits Symposium, pp 214-215.
- [8] T. Matano et al., "A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer", Proceedings, 2002 VLSI Circuits Symposium, pp 112-113.
- [9] US Patent Pending, "A fully digitally controlled delay element with wide delay tuning range and small tuning error", Cangsang Zhao, Byron Grossnickle.