A Real-Time Jitter Measurement Board for High-Performance Computer and Communication Systems

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Abstract

This paper presents the design and performance results of a real-time jitter measurement board for testing high-frequency clocks and data transceivers. The board targets high-volume manufacturing test to measure sinusoidal jitter tolerance and random jitter in computer and communication systems, with a substantial reduction in test cost compared to existing equipment.

1. Introduction

Jitter testing is the key challenge in manufacturing high-speed I/O devices as well as communication devices. Jitter tolerance tests are commonly performed on receiver circuits using sinusoidal jitter [1]. On the other hand, to test intrinsic jitter of the device, random timing jitter generated by a transmitter in the absence of applied jitter must be also measured [2]. In response to these measurement needs, manufacturers have developed a wide range of test instruments, ranging from high-frequency oscilloscopes with jitter measurement capabilities (e.g. Tektronix [3], LeCroy [3], Agilent [4], etc.) to dedicated signal integrity analysis systems (SIA) or time interval analyzers (TIA) (e.g. Wavecrest [5], GuideTech, etc.). Since instruments are typically expensive both in terms of initial cost and in cost per-unit testing time, they are mainly used for characterization testing, and not in a production test environment.

We demonstrate in this paper the design of a real-time jitter measurement board that meets both jitter tolerance and random jitter measurement needs, and that is suitable for use in production testing. This board has been prototyped and its linearity and measurement accuracy are validated in this paper.

Terminology and definitions are presented in Section 2. Section 3 discusses the requirements and specifications for the board. Section 4 describes the board design and its operation principle in jitter testing. Section 5 presents experimental results using this board to test computing and communication circuits. Finally, both the advantages and disadvantages of this jitter-measurement board are discussed in Section 6.

2. Terminology

Timing Jitter [6]. Timing jitter is the uncertainty in the edge of a square wave signal, or the uncertainty in the zero-crossing point of any other signal. If the total instantaneous phase of a signal is denoted by $\phi(t)$ and the edge position or zero crossing is at a time nT, then the timing jitter is the variation of $\phi(nT)$, denoted by $\Delta\phi[n]$. $\Delta\phi[n]$ is shown in Figure 1.

Period Jitter [6]. Period jitter $J[n] = \Delta\phi[n+1] - \Delta\phi[n]$ is the variation of the instantaneous period from the constant mean period T.

Sinusoidal Jitter. Sinusoidal jitter refers to the use of a sinusoidal phase modulation provided by a sinusoidal jitter source. It is normally used in standard jitter tolerance testing [1], [7]. The

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sinusoidal jitter is described by $\frac{\Delta\theta_{PP}}{2}\cos(2\pi f_{PM}t)$ where $\frac{\Delta\theta_{PP}}{2}$ is the jitter amplitude ($\Delta\theta_{PP}$ is the peak-to-peak value of timing jitter) and f_{PM} is the jitter frequency [8].

Random Jitter. Random jitter (RJ) encompasses timing edge uncertainties introduced by random noise sources. Random jitter is assumed to have a Gaussian distribution, to be uncorrelated with other system noise sources, and to be unbounded as test time increases. Random jitter has been a focus of the design and testing of low-jitter oscillators in the past several years [9]-[11].

Jitter Tolerance [8]**.** Jitter tolerance measurement is an extension of bit error rate (BER) testing. It is a measure of the boundary across which a deserializer starts to introduce errors due to the applied data transition jitter. This boundary separates the erroneous region and the error-free region as a function of the amplitude of the jitter applied to the deserializer under test. The jitter amplitude at the boundary gives an upper limit of maximum tolerable jitter [12]. A SONET jitter tolerance test uses sinusoidal jitter at a fixed frequency and amplitude to modulate edges of a data clock [1].

3. Requirements and Specifications

3.1 Requirements

A jitter-measurement board should meet the following requirements;

R1. Timing jitter measurement is required.
R2. Jitter should be measured in real-time.
R3. Measurement of jitter should be performed without using a reference clock or any triggering signal.
R4. Measurements must be accurate and repeatable.
R5. For use in production test, the test unit or test board must be small enough to be mounted as part of the ATE test head or performance board.
R6. Unit cost should be minimized.

Timing Jitter. In the case of high-speed I/Os, the key measure is not a period fluctuation of the clock signal but a timing misalignment between the data sequence and clock signal. Therefore, the board should measure edge fluctuations (= timing jitter) in both the data sequence and the clock signal [13]. In particular, (a) sinusoidal timing jitter measurements are required for testing jitter tolerance in data communications, and (b) random timing jitter measurements are required for testing intrinsic jitter. Consequently, a measurement method and circuit implementation which provides the capability for measuring timing jitter, i.e. requirement *R1*, must be developed.

Test Time. Many conventional methods perform post-processing on captured waveforms, or measure period fluctuations using a non-zero dead time counter. Thus, it takes long test times to measure jitter using conventional methods. In order to realize short test times, the proposed board must meet both requirements *R2* and *R3*.

Size & Cost. The size of a typical oscilloscope is 18"x17"x11" and the size of a typical dedicated jitter test instrument is 23"x17"x9". Moreover, the current equipment cost is approximately $70K for high-performance oscilloscopes to $150K for dedicated jitter test instruments. Thus, *R5* and *R6* must be met by finding a new way to realize requirements *R1* to *R4*.

3.2 Specifications

The first prototype design is targeted to meet these requirements as well as the following specifications, in consideration of standards [7], [14]:

S1. Maximum frequency of clock or data signals: 2 GHz (= 4 Gbps).
S2. Maximum jitter frequency for sinusoidal jitter: 10 MHz.

Note that these maximum frequency limits could be improved in future designs.

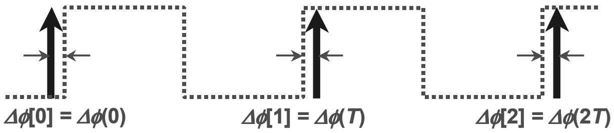

Figure 1. Illustration of timing jitter.

4. Design and Operation of Real-Time Jitter-Measurement Board

The measurement method implemented in this board focuses on timing jitter (*R1*), not period jitter. Figure 2 shows a communication system with both a transmitter and a receiver, together with the received waveforms of DATA and recovered clock RCLK. Note that, as an erroneous decoding is illustrated in Figure 2(c), the decoding of the data depends critically on the rising edge of the RCLK. Timing jitter affects the locations of these rising edges, thus the measurement should target timing jitter instead of period jitter.

The timing jitter at a rising clock edge can be measured by accumulating the period jitters in the preceding time intervals as illustrated in Figure 3. J_1 is the period jitter of the first clock period (e.g. the first period value is actually $T+J_1$). J_2 is the period jitter of the second clock period. Therefore, the edge displacement of the third rising edge of the clock is obviously given by J_1+J_2. In general, the timing jitter at the n^{th} rising edge of the clock is given by the sum of the period jitter $\{J_k\}$ over the entire preceding clock times:

$$\Delta\phi_n = \sum_{k=1}^{n} J_k \qquad (1)$$

This simple observation leads to the measurement circuit shown in Figure 4, with representative waveforms to be used in describing the operations of this circuit. The circuit accepts one input (the CLK signal in the figure), whose timing jitter is to be measured. The DELAY block provides a 1-unit delay (1-UI), thus the two inputs to the following phase-frequency detector (PFD) are the current CLK signal and the DCLK signal from the previous cycle delayed by 1 clock period.

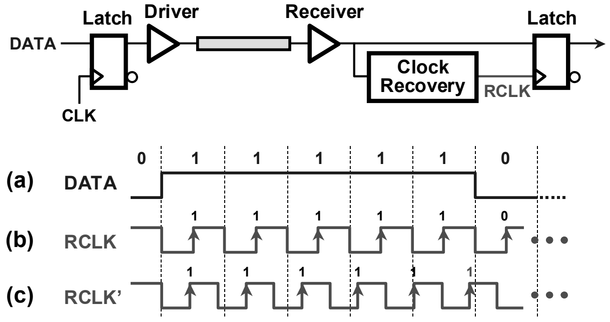

Figure 2. A communication system and received waveforms with timing jitter.

The PFD compares these two signals, which in essence means that it computes the period jitter J_k at clock time *k*. The outputs of the PFD drive the charge pump, which could be in either of two states (Figure 5):

1. If the period jitter is *negative*, e.g. the delayed clock edge precedes the current clock edge, the UP signal is generated and its pulse width is the instantaneous period jitter.
2. If the period jitter is *positive*, e.g. the delayed clock edge follows the current clock edge, the DOWN signal is generated and its pulse width is the instantaneous period jitter.

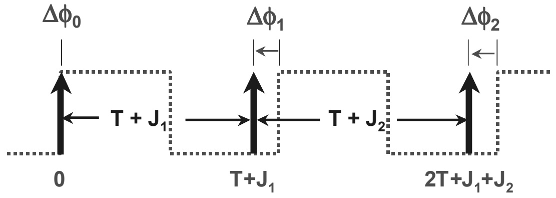

Figure 3. Timing jitter as accumulation of period jitters.

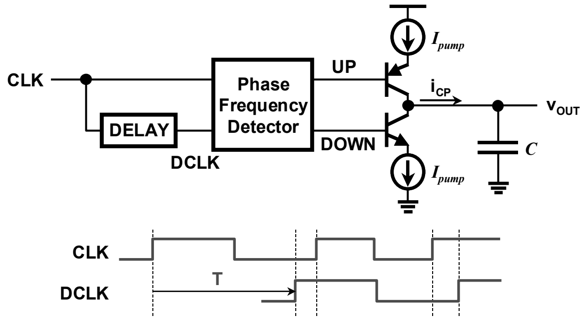

Figure 4. Measurement circuit.

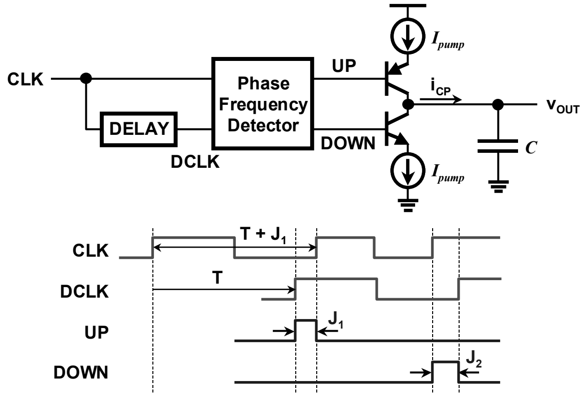

Figure 5. Generation of J_1 and J_2.

The UP and DOWN signals result in either charging or discharging the capacitor, which is equivalent to the period jitter accumulation in Equation (1). In Figure 6, the capacitor charges up during the pulse width J_1 of the UP signal and the voltage V_{out} at the end of the charging time is:

$$V_{out} = \frac{I_{pump} J_1}{C} \tag{2}$$

At the next clock cycle, the jitter J_2 results in the discharge of the capacitor and the voltage V_{out} at the end of the discharging time is:

$$V_{out} = \frac{I_{pump}}{C}(J_1 + J_2)$$

Note that J_2 is negative in this example. The operation of this circuit continues in this manner with the charge pump acting as a summer or an integrator.

$$V_{out} = \frac{I_{pump}}{C}\sum_{k=1}^{n} J_k \tag{3}$$

It is obvious that after n clock times, the voltage V_{out} is directly proportional to the timing edge jitter at time nT from Equation (1).

The discussion above relates mainly to timing jitter in clock signals, with one rising edge at each clock cycle. For data signals, an arbitrary data sequence, e.g. <10000000000>, might not contain a sufficient number of rising edges to generate the correct UP and DOWN signals. The specific clock pattern <101010...> is used to verify the performance of the board and to measure intrinsic jitter in this specific case.

If an analog-to-digital converter (ADC) is used to digitize V_{out}, the sampling frequency must be $f_{\text{sample}} > 2\ f_J$, where f_J is the jitter frequency or the offset frequency from the nominal input clock frequency f_{CLK} ($=1/T$). The voltage value of the LSB of the ADC is given by $V_{out}/2^b$. Typically the number of bits ($= b$) is 8.

In order to analyze the behavior of the circuit as a function of f_J, the period jitter is re-defined using its frequency characteristics [9]:

$$J(f_J) = 2\sin(\pi f_J T) \tag{4}$$

For the first measurement of the input rising edge, Equations (2) and (4) yield:

$$V_{out}(f_J) = 2\frac{I_{pump}}{C}\sin(\pi f_J T) \tag{5}$$

As the measurement continues with more rising edges, the final output of the circuit given by Equation (3) is equivalent to integration in the time domain, which is the same as multiplication by $1/s$ in the frequency domain. With $|s| = 2\pi f_J T$ at the jitter frequency for one period T, the overall jitter transfer function between input timing jitter and output V_{out}, in terms of the offset frequency f_J, is given by:

$$H_{JIT}(f_J) = \frac{1}{\pi}\frac{I_{pump}}{C}\frac{\sin(\pi f_J T)}{(\pi f_J T)} \tag{6}$$

The ideal transfer function of the measurement circuit is plotted in Figure 7, for an input clock

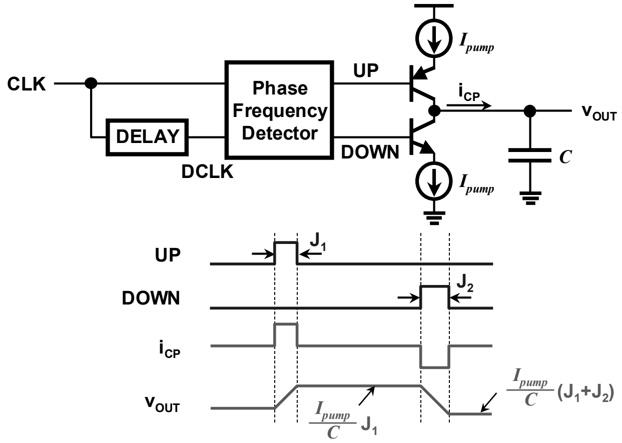

Figure 6. Circuit operation to generate output voltage.

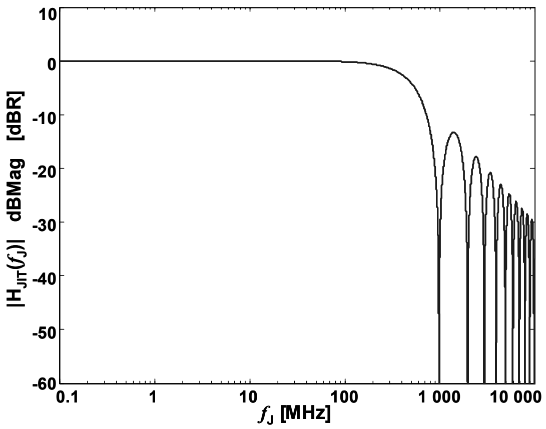

Figure 7. Timing jitter transfer function of the circuit.

frequency of 1 GHz or T=1000 ps.

At the beginning of each timing measurement test, the initial value on the capacitor C needs to be reset to 0. Note that while the final output of the circuit is proportional to timing jitter at time n, period jitter is measured at each clock time and accumulated over n periods to produce the desired timing jitter.

At this point, we have characterized the circuit operation both in the time and frequency domains. The proposed circuit clearly satisfies requirements *R1* to *R3*. The performance of the jitter measurement board is verified in the next section.

5. Performance Verification

The performance of the prototype board for measuring both sinusoidal jitter and random jitter was verified with experimental results.

5.1 Verification Test Using Sinusoidal Jitter

The test setup for sinusoidal jitter is shown in Figure 8. The transmission analyzer (Advantest D3371) generates a clock signal at 985 MHz with sinusoidal jitter. The 1-UI delay element was implemented using a semi-rigid cable with a delay time of 1015 ps. The remainder of the circuit was implemented on the prototype board. The board output was measured with a spectrum analyzer (Advantest R3273).

Figure 9 shows the performance of the jitter measurement board. The output voltage is linearly related to the input timing jitter for the 3 offset frequencies f_J used in the test. This linearity is very important since it relates the output voltage values to the input timing jitter values. Figure 7 shows that the transfer function of the board has a constant magnitude for all 3 frequencies but the slopes in Figure 9 are different due to the finite conductances of the charge pump currents in the actual tests.

The standard deviations in the output voltage measurements were 0.86 mVpp, 3.1 mVpp, and 17.3 mV pp for the 3 jitter frequencies f_J = 0.5 MHz, 1 MHz, 5 MHz, respectively. Note that the standard deviations are very small compared to the values of V_{out} plotted in Figure 9.

5.2 Verification Test Using Random Jitter

The test setup for random jitter is shown in Figure 10. The random noise is fed into the FM input of the signal generator (R&S SMT03) from an arbitrary waveform generator (Tektronix AWG2010). The signal generator generates a clock signal of frequency 985 MHz with random jitter. The 1-UI delay element is again implemented with a semi-rigid cable having a delay time 1015 ps. The board inputs and outputs were measured by using a spectrum analyzer (Advantest R3273) and an oscilloscope (Tektronix TDS7404).

Figure 11 shows good agreement between the jitter transfer function of the measurement board estimated; one estimated using random jitter and the other measured using sinusoidal jitter. Due to the lowpass characteristics of the circuit output buffer, the jitter transfer function shows gain loss at frequencies greater than 5 MHz. The roll-off at low frequencies, not predicted in Figure 7, is due to the finite conductances of the charge pumps and the

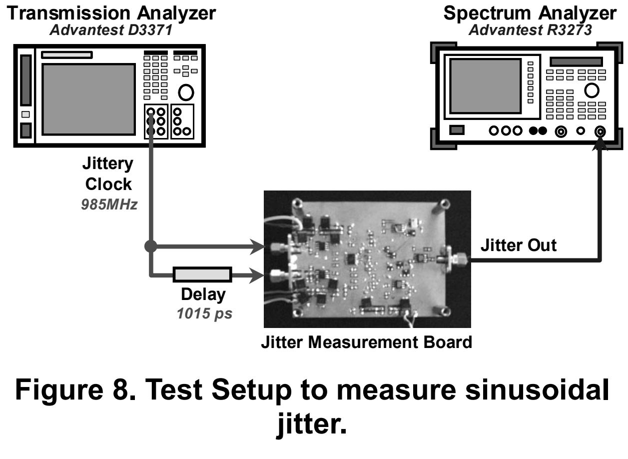

Figure 8. Test Setup to measure sinusoidal jitter.

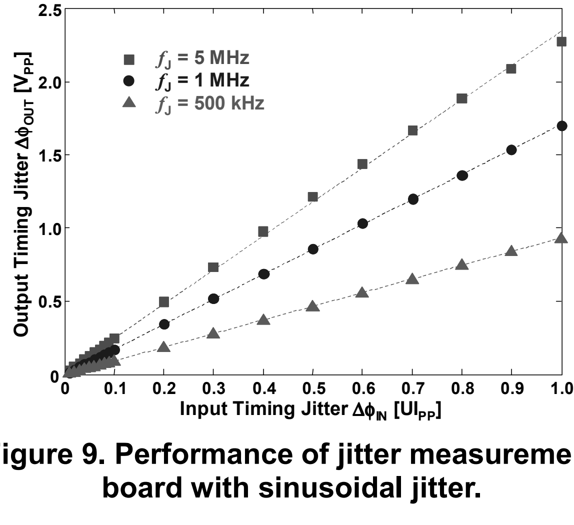

Figure 9. Performance of jitter measurement board with sinusoidal jitter.

capacitor leakage current in the actual tests.

An application of the board for sinusoidal jitter tolerance testing of high-frequency I/O, data, and communications systems is shown in Figure 12.

Figure 13 illustrates another application of the board in a jitter generation test of a communication transmitter using a <1010…> clock pattern. This specific pattern has been demonstrated [15] to be useful in measuring the intrinsic jitter of a communication transceiver.

6. Advantages and Disadvantages

The jitter measurement board described in this paper offers several key advantages in meeting the testing requirements R1 through R6;

1. *R1 and R2* Jitter measurement can be performed in real time using the board, which is not possible with other methods. For example, the TIA or SIA methods require a non-zero dead-time counter, which translates into long test times. In addition, the non-zero dead time TIA method only measures period jitter, not timing jitter, in a practical way. Using the jitter measurement board, it takes 0.2 msec to measure sinusoidal timing jitter at $f_J = 5$ kHz.
2. *R3* In contrast to other test methods, the jitter testing board does not require a reference signal or any internal/external trigger signal.
3. *R5* The size of the jitter measurement board, which is shown in Figures 12 and 13, is approximately 2.4" x 2.0" x 1". It is small enough to be used as part of the performance

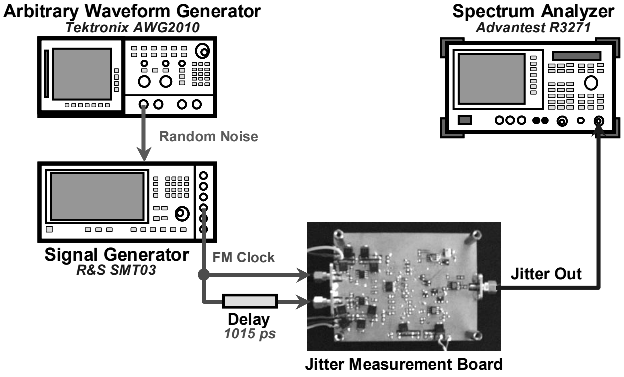

Figure 10. Test Setup to measure random jitter.

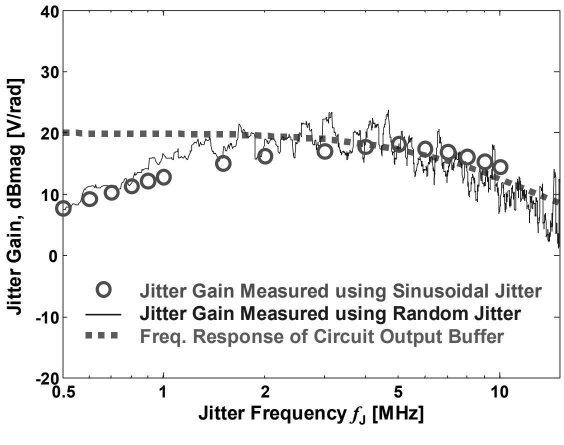

Figure 11. Jitter transfer function of jitter measurement board with sinusoidal jitter/random jitter input.

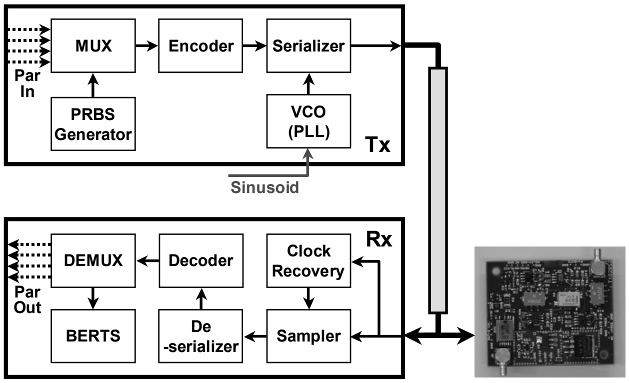

Figure 12. Sinusoidal jitter tolerance testing for communication systems.

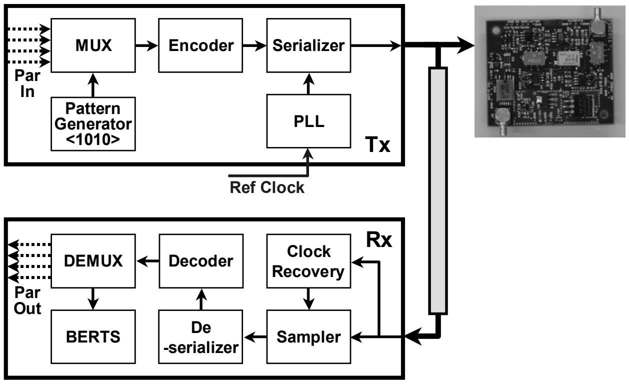

Figure 13. Testing jitter generation in communication transmitters.

board or to be integrated into the ATE test head for production test. It is substantially smaller than existing jitter test instruments (oscilloscopes, TIAs), which are bulky and can only be used for characterization tests.

4. *R6* The per-unit cost of this jitter measurement board is about \$2K - \$3 K. This is many times less than the cost of other commercial jitter test systems currently on the market.

The combination of real-time capability, size, and cost makes this jitter measurement board a unique entry in the test equipment market. The board acquires timing jitter measurements that can be used in further data analysis to extract more information. Post-processing of the acquired data is performed on the ATE to reduce measurement noise and jitter statistics. The board can also be used to determine the frequency content of the jitter.

However, the jitter measurement board currently has several limitations:

1. The 1-UI delay element must be adapted to each specific frequency of the signal under test. If the frequency changes, the delay element must be changed to ensure that the delay is still 1 UI = 1/ f_{CLK}. Programmable delay elements will be required to make the board applicable to a wide range of input signal frequencies.
2. The 1-UI delay element is not precise. This delay uncertainty is reflected in larger or smaller measured timing jitter values. Therefore, each board needs to be calibrated during actual testing to ensure better accuracy.
3. The board's frequency performance is limited by the PFD, which in currently limited to 2 GHz. This frequency limitation can be improved in the future with the implementation of a higher speed PFD.

Note: Another way to overcome the frequency limitation is to combine the board with the frequency divider [2].

7. Conclusion

This paper presented the design and performance results of a jitter-measurement board capable of real-time testing of sinusoidal jitter tolerance and intrinsic random jitter in computers and communication systems. The design utilizes a combination of a delay element, phase-frequency detector, and time-to-voltage converter based on the charge pump concept. The performance of the board has been verified in several sinusoidal and random jitter tests. Because the board has short test times, is small in size, and is very low in cost compared to conventional jitter testing instruments, it provides a very attractive testing capability for the manufacturing environment.

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