Experimental Results for High-Speed Jitter Measurement Technique

Karen Taylor, Bryan Nelson, Alan Chong, Hieu Nguyen, Henry Lin, Mani Soma,
Hosam Haggag[2], Jeff Huard[3], Jim Braatz[3]

Department of Electrical Engineering, University of Washington, Seattle, WA
[2]Santa Clara Design Center, National Semiconductor, Santa Clara, CA
[3]Tacoma Design Center, National Semiconductor, Federal Way, WA

Abstract

A BIST method to measure jitter without external references is presented. Measured data from 0.25-μm BiCMOS chips show jitter resolution about 30 to 50 ps over 8 cycles of a 1 GHz input signal.

1. Introduction

Data communication systems and microprocessor speeds are moving into the GHz range. With the increase in data rates, it is becoming more difficult to meet the timing requirements, and system designers require more accurate jitter measurement techniques. The cost of jitter measurement is high using Automated Test Equipment (ATE) for GHz clocks, and built-in self test (BIST) is an option to consider. A successful BIST design must possess the following characteristics:

1. Functionality at GHz frequencies
2. Quick measurement (<1 ms/5000 samples)
3. High Resolution (<10 ps)
4. Immunity to noise and mismatch
5. Digital components
6. Minimal inputs and outputs
7. Minimized area

There are many designs to convert time to a digital value or to measure jitter. One recent external technique measures jitter by digitizing signal samples [1] while another one uses statistical analysis combined with undersampling [2]. The digitization method in [1] applies a sine wave to an analog-to-digital converter (ADC) and uses the signal under test as the ADC clock. With the undersampling technique [2], the test signal is sampled by an ATE in incremental time shifts near an edge transition and stored to create a statistical picture.

Examples of popular on-chip implementations of time-to-digital converters (TDC) are the delay lock loop (DLL) and the vernier delay line (VDL). The DLL measures the phase difference between a series of delay elements and the signal under test [3, 4]. The VDL extends DLL by measuring the differences between two gate delays [5]. Matching issues of delay elements in VDL was solved by component-invariant VDL, at the expense of test time [6]. These techniques can be easily integrated for on-chip test. However, these two techniques require a jitter-free reference clock. As a result, these methods require careful design consideration to minimize jitter in the reference signal.

In past approaches, TDC architecture was comprised of a time-to-amplitude converter followed by an ADC [7]. Two voltages are pre-charged to a fixed value and discharged over a measured time. The voltage difference is converted into the time domain. This method requires an off-chip solution for the capacitor, uses a reference voltage for the ADC and is implemented using emitter coupled logic (ECL). Integration using this technique for BIST is difficult in CMOS IC technology.

Other implementations [10] use peak detectors and comparators to measure time. The peak detectors are used to minimize the stored data while a time-to-amplitude converter acquires the timing information until an ADC can digitize the value. A final solution in [9] uses delay lines and an interpolator to improve the measurement accuracy. Counters count the gate delay and the periods to provide a time measurement.

The design for our measurement technique was presented in [8], and the purpose of this paper is to present the test results. The technique uses the clock signal under test to control the charging of the input capacitance of an ADC. The charged voltage is a function of the clock period, and the ADC converts this voltage to a digital measure of the clock period, from which jitter can be extracted. This method measures accumulated jitter over N clock cycles, where N is a selectable value. One advantage of this design is that it does not require an external jitter-free reference clock or a voltage reference. Figure 1 shows the design architecture [8].

0-7803-8580-2/04 $20.00 Copyright 2004 IEEE

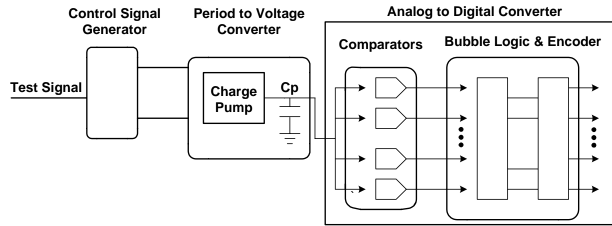

Figure 1: Jitter measurement architecture.

This paper consists of the following sections. In section 2, a review of the design implementation is given. Section 3 describes the test setup and the test plan while section 4 shows the measured results from the fabricated chips. Section 5 compares the design measurements with measurements by Wavecrest equipment while section 6 discusses limitations of this design. Section 7 shows possible design improvements, section 8 compares these results with previous works, and section 9 summarizes the key features. Conclusions are drawn in section 10.

2. Design implementation

This design was created from theoretical ideas and analysis. Appropriate device sizes and robust design were determined through simulation using HSPICE. The design implementation and the simulation results follow.

2.1 Theoretical design

The time-to-digital conversion (TDC) implemented in this design converts an input clock period to a voltage, which is then digitized. The digitized value represents the measured clock period. Period jitter can be extracted from the difference between the expected value and the measured value. Statistical post-processing can be performed on this measured data for other jitter extraction. The method permits the measurement of accumulated jitter over N periods, where N is selectable (N=8, 10, 16, and 18). This capability allows jitter sampling over many cycles, potentially useful to study jitter as function of time.

The period-to-voltage converter uses a simple charge pump to charge the gate capacitance of the input comparators of the ADC. The comparators are all-digital (as opposed to the conventional analog comparators) and use inverter chains to set the reference levels for comparisons. The inverter chains are designed with different switching thresholds. Each threshold voltage represents the reference voltage of that comparator. Each chain is a cascade of 3 stages, each stage composed of parallel inverters: the first stage has 8, the second has 4, and the last has 2 parallel inverters. This topology makes the design more robust with respect to process variation [8]. The inverter thresholds (reference levels) were separated by 35 mV, determined through analysis to make sure that neighboring chains were unlikely to switch out of sequence due to process variations. Bubble correction logic eliminates any overlap in the output of the comparators due to process variation and device mismatch. A regular flash encoder provides the final digital output.

Figure 2 illustrates this method for period jitter measurement. The top plot shows the clock input converted into the charge control signal. The middle plot shows the charging of the ADC input capacitance (composed of gate capacitances of all input comparators). The bottom plot shows the histogram of the measured outputs for jitter extraction.

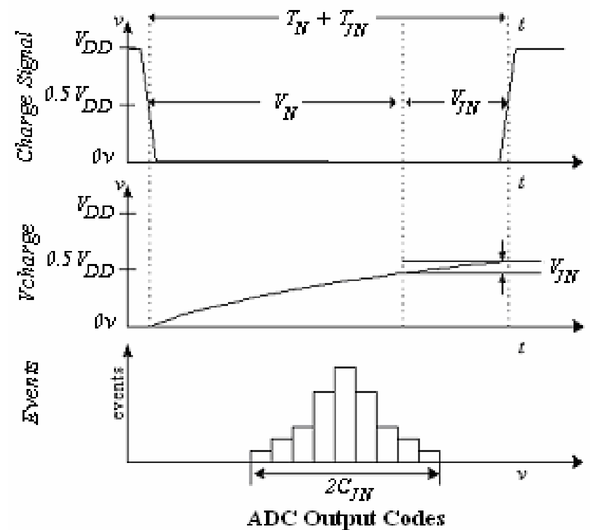

Figure 2: Proposed jitter measurement method.

The design was implemented in a 0.25-µm BiCMOS process, even though all the circuits are strictly CMOS. There are two additional test structures besides the complete design. The first test structure is used to check the reference level and the functionality of each comparator chain. The second test structure is a set of comparators designed with different reference levels separated by 16 mV, 8 mV and 4 mV. This structure determines whether a higher resolution can be implemented by decreasing the separation of the comparators' reference levels.

Figure 3 shows the layout of the entire design: section A is the jitter measurement circuit, section B is one complete comparator, and section C is the set of test comparators previously described.

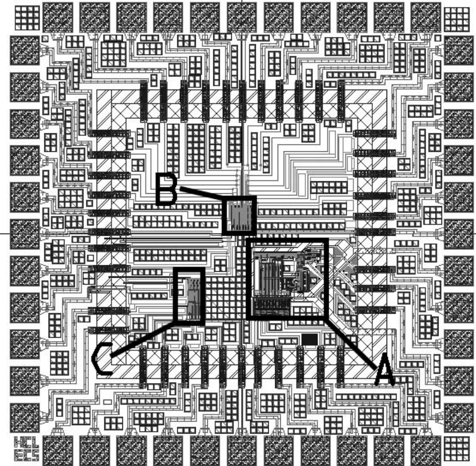

Figure 3: Chip layout.

2.2 Simulated results

We performed extensive simulations to prove the concept and function of the design. The circuit measures eight periods (N=8) and operates from 625 MHz to 1 GHz with the comparator chains spaced 35 mV apart. For correct operation, the output voltage range of the period-to-voltage converter has to match the input voltage range of the ADC for all process variations. Process variations is the critical factor determining the final range and resolution of the TDC circuit, and our simulations use five different process corner models of NMOS and PMOS shown in Table 1.

Table 2 summarizes the simulation results for the DNL, INL and the voltage difference corresponding to 1 least significant bit (LSB) over process corners. The maximum DNL is 0.2 LSB and the maximum INL is 0.574 LSB. A more thorough analysis of the simulation results can be found in [8].

Table 1: Simulated Corner Models.

SS:	Slow NMOS/Slow PMOS
SF:	Slow NMOS/Fast PMOS
TT:	Typical NMOS/Typical PMOS
FS:	Fast NMOS/Slow PMOS
FF:	Fast NMOS/Fast PMOS

Table 2: LSB, INL, and DNL variations.

	SS	SF	TT	FS	FF
LSB	0.029	0.035	0.035	0.034	0.039
LSB+/-	0.001	0.006	0.001	0.005	0.001
DNL+/-	0.04	0.17	0.03	0.20	0.04
INL+/-	0.078	0.574	0.019	0.514	0.120

Figures 4 and 5 show the simulated DNL and INL for these process corners at room temperature. Figure 6 shows the output voltage of the period-to-voltage converter as function of the input signal period over process corners. While the variations are considerable, note that linearity is preserved and the shift in voltage levels can be calibrated before each test.

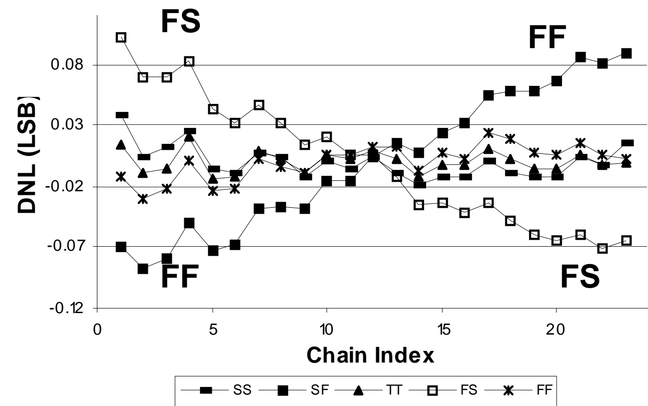

Figure 4: DNL process variations for ADC at 25°C.

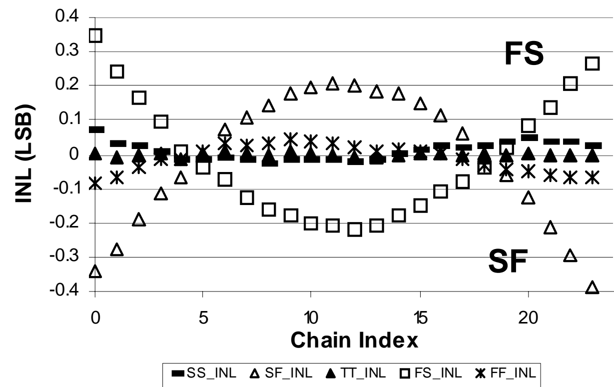

Figure 5: INL process variations for ADC at 25°C.

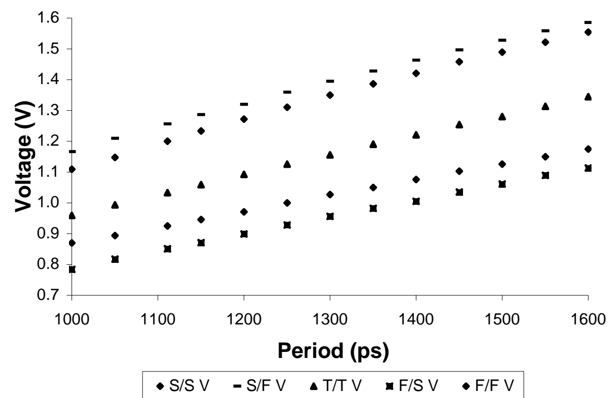

Figure 6: Voltage versus time over process corners at T=25C°, N=8.

3. Test setup and test plan

The design was fabricated in a 0.25µm BiCMOS process provided by National Semiconductor Corporation. We received twenty-four chips, packaged in 44-pin leadless leadframe package (LLP), and designed a load board to test these chips. The test setup and test plan follow.

3.1 Test setup

The load board (Figure 7) was designed to accommodate a large number of I/O from the jitter measurement circuit as well as the two additional test structures. The board also includes appropriate series terminations and power supply and bias circuits. Series terminations were chosen over parallel terminations to limit power consumption. The trace impedance calculated from the board vendor's specifications was around 80 Ohms, so a resistor of 0.22 Ohms was used to terminate traces. No major voltage reflections were noticed during testing, so this series resistor value was kept.

The Agilent signal generator (Figure 8) generates a $1V_{pp}$ sine wave with DC level at 0V. To offset this signal to mimic a clock signal, the load board includes a DC level shifter (top right corner of Figure 7). AC/DC blocks were used to prevent signal loss in these circuits.

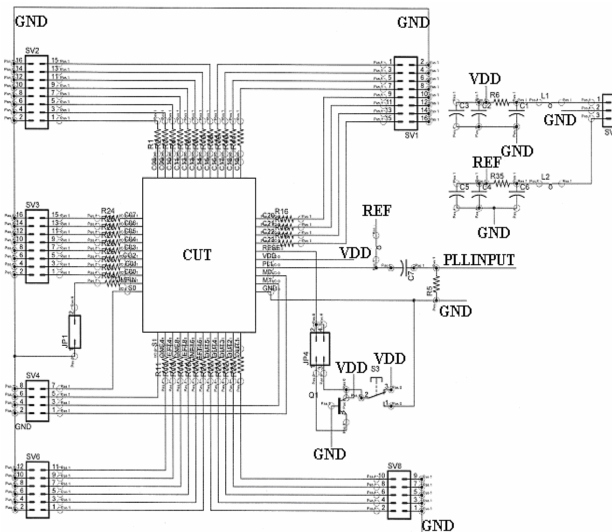

Figure 7: Load board layout.

The test set-up (Figure 8) includes: Agilent E8254A PSG-A Series signal generator, Tektronix TDS 784D Oscilloscope, Tektronix P2521G Programmable Power Supply, Tektronix TLA715 Logic Analyzer, and Wavecrest SIA-3000 Signal Integrity Analyzers. The signal generator generates the clock signal to be tested. The oscilloscope gives us an alternate means to monitor this clock signal while the logic analyzer examined the outputs.

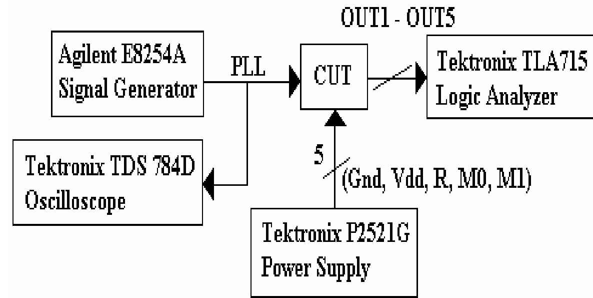

Figure 8: Test setup.

3.2 Test plan

The test plan verifies the chip function, examines the design issues and provides data for design improvement.

3.2.1 Comparator testing

The goals of comparator testing are:

- Determine the voltage separation between comparator thresholds,
- Provide a voltage-to-code mapping,
- Determine whether finer threshold separations can be achieved,
- Determine comparator speed, and
- Determine design robustness over process.

The same tests are performed for the isolated comparator structure and comparators in the additional chains.

Initially, a stuck-at fault test is applied to check the basic comparator functionality. Applying a square wave to the input of the comparators reveals any stuck-at faults on the outputs. The correct output should also be an inverted square wave in reference to the input. An incorrect output bit found with this method can be understood as a fault somewhere in the respective comparator chain. The location of the fault within the inverter chain cannot be determined since the chains have only one input.

To determine the voltage thresholds of the comparators, analog voltages (from a power supply) are stepped in increments of 10 mV at the input, and the corresponding output code is recorded by a logic analyzer.

To test the comparator speed, a ramp signal is applied to the comparator. The period of the ramp signal is decreased incrementally until we detect missing codes at the output of the comparator. The first

occurrence of missing output codes indicates the maximum operational frequency of the comparator.

3.2.2 Complete design testing

The goals of complete design testing are:

- Observe the influence of process variations,
- Create time-to-code mappings,
- Observe the effects of power supply variation, and
- Generate data for further analysis.

To meet these objectives, the transfer curves of the design are analyzed, which provide insight into I/O characteristics, input range, measurement resolution, and process and voltage variations.

To generate transfer curves experimentally, a value of N is selected, a test signal of a specific frequency is applied to the input, and the output codes are recorded. The input signal frequency is then incremented in 10 MHz steps, and the procedure is repeated until the full range of output codes has been spanned. This procedure can also be used to determine the effects of voltage variation.

To observe the effects of power supply variations, the above procedure is repeated with power supply settings varying from V_{DD} – 10% to V_{DD} + 10%. The 10% maximum variation usually corresponds to the worst case.

The N values chosen for this design were 8, 10, 16, and 18. The center frequencies were respectively 900 MHz, 1 GHz, 2.4 GHz, and 3 GHz. These values were chosen based on the wireless standards in use today, and some were chosen to observe the limits of the design. However, due to process, voltage and temperature (PVT) variation, the center frequency may be different from the design value; hence, the large frequency range used in generating the full range transfer curves.

4. Experimental results

Testing was performed in two main segments. First, the comparators were tested and then the complete design was tested.

4.1 Comparator results

After a basic stuck-at fault test revealed a fully functional chip, the comparators were tested with a ramp signal to determine the switching threshold for each comparator chain, and the threshold separations between chains. A ramp signal, with similar rise time as seen on the input of the full circuit ADC, was created using a square wave instead of a ramp signal from the function generator. A square wave was used because the rise time of the generated ramp signal was too slow and caused the ADC output to oscillate. The square wave was zoomed in on the rising edge, where it appeared to be a ramp signal, and the switching threshold of each comparator chain was acquired.

The individual comparators, shown in section C of Figure 3, had promising test results for the 16 mV and 8 mV comparator threshold spacing. Table 3 describes the average results and the standard deviation across the chips tested for each threshold spacing. For the designed 16 mV spacing, the average measured threshold spacing was 14.96 mV with a standard deviation of 2.24 mV. The threshold spacing error was on average less than 10%. The comparator designed with 4 mV threshold spacing fails this specification and shows that 8 mV threshold spacing is likely the lower limit for this specific design. This lower limit relates to the precision of our jitter measurement method.

Table 3: Individual comparator test results.

Designed threshold spacing (mV)	Tested comparator spacing (mV)	Tested spacing std. (mV)	Input voltage Vin (mV)
4	15.76	5.96	612.88
8	6.92	2.09	613.20
16	14.96	2.24	617.60

Figure 9 shows the outputs of two comparator chains when a square wave signal is applied to the input. The threshold voltage spacing was measured at the amplitude of $V_{DD}/2$ for each comparator output. We note that direct external probing creates a significantly different load on the comparators than during normal operation in the full BIST design. Due to the capacitive coupling between the input and output of the basic inverter structure used in the comparator design, the different capacitive load has an impact on the measured switching threshold of a comparator.

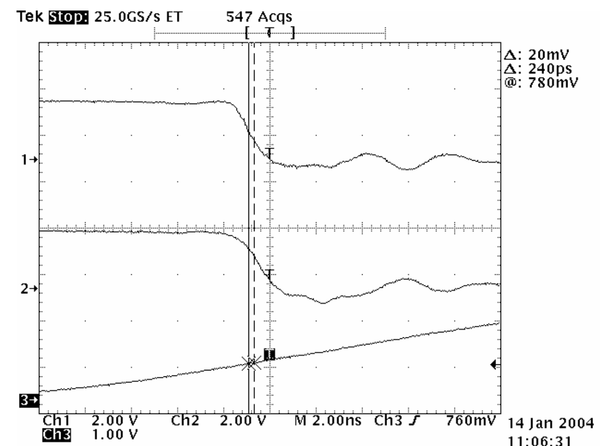

Figure 9: 16mV-spaced individual comparator.

Threshold measurements of all the comparator chains in a separate ADC show a wider variation than expected. Threshold spacing between each individual chain varied drastically when measuring the output switches at $V_{DD}/2$, both due to the load difference described above and due to the high-frequency Miller effect between the input and output of each inverter. The measurement was extremely sensitive to the input signal slew rate and this sensitivity accounts for the wide variation in threshold spacings. Comparator threshold spacing between chains 1 and 24 had an average value of approximately 25 mV compared to the designed 35 mV.

4.2 Complete design results

The results from the full measurement chip testing were positive. The device response followed the simulation results with respect to process variations. The next few figures illustrate the transfer characteristics, INL, DNL, and supply dependence of the devices that were tested.

Figures 10 through 13 demonstrate some interesting statistics. The maximum DNL is less than 0.8 LSB, the maximum INL is less than 1.2 LSB, the resolution is 55 ps and the power consumption is 16 mA at 2.5 V. The linearity values were slightly higher than simulated, but the resolution was better than the simulated values and the power consumption was smaller than simulated values.

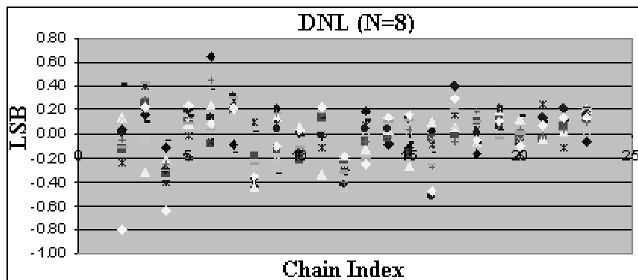

Figure 10: DNL of tested chips, N=8.

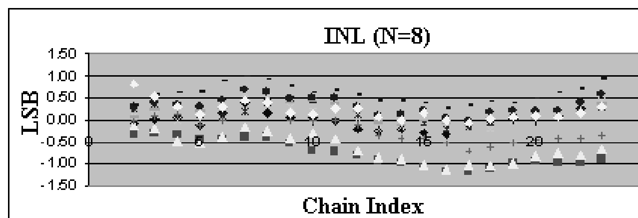

Figure 11: INL of tested chips, N=8.

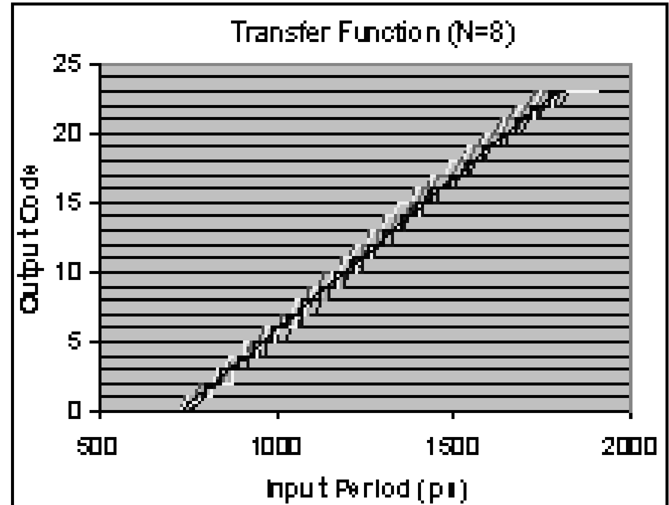

Figure 12: Transfer function of tested chips, N=8.

The experimental data agrees well with simulation for most of the design criteria. At high frequencies, the limit turns out to be the D flipflop in the front-end circuit. At N=16 and 18, when the input signal frequency is 2 to 3 GHz, the front-end divide-by-2 circuit does not operate fast enough to generate the correct control signal for the charge pump; hence, the input range is reduced. For lower input frequencies (up to 2 GHz) and other values of N, all circuits operate within their specifications and the measurement is correct. At N=8, there was only one chip (out of 24) with a missing output code.

Testing results at different supply voltages [V_{DD}-10%, V_{DD} + 10%] agreed with the predicted threshold values. As V_{DD} increases, the threshold voltages of the comparator chains increase. This results in offsetting the typical frequency range to a lower scale, and vice versa for the case when V_{DD} is decreased. Note that the transfer function remains quite linear (Figure 13) and the power supply variation only induces a horizontal shift in the whole curve.

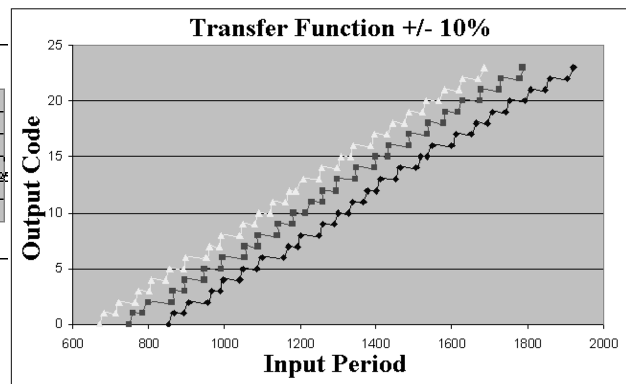

Figure13: Transfer function vs. power supply.

4.3 Simulated vs. measured results

The simulation values and measured values were slightly different. Some useful information and interesting facts can be drawn from comparing the values. Table 4 presents a comparison between the simulated and measured data.

Table 4: Result comparison.

Timing Characteristics	Simulated	Measured
Measurement Frequency	625 MHz - 1 GHz	600 MHz - 1.4 GHz
LSB	70 ps	55 ps
DNL (3σ)	0.2 LSB	0.5 LSB
INL (3σ)	0.8 LSB	1.2 LSB
Power Consumption	45 mW	40 mW

With respect to operating frequencies, the simulation was performed only for the case N=8 and the frequency range is between 625 MHz and 1 GHz. The measured results show higher operating frequencies since we tested the circuit for other values of N representing faster input signals. As mentioned above, the front-end divide-by-2 circuit is the limiting factor in operating frequencies and starts to fail at about 1.4 GHz.

The measured LSB was smaller, thus better, than the simulated LSB. We were extremely conservative in estimating threshold separation in the simulation, and the real results show much better resolution.

The final difference between the simulated and measured results is in the linearity values. The DNL and INL measured values are larger than the simulated values. The variations of the threshold values are not consistent over all the chains, and some variations are significantly higher than the designed 35 mV, thus making the linearity values larger. Despite this difference, the measured DNL and INL values are still within normally specified limits for ADC.

5. Comparison with Wavecrest results

Once the specifications of the chip were tested, the circuit was used to measure a signal produced by an LMX2505 PLL tested with its own evaluation board. The PLL was controlled to produce an 800 MHz output. The PLL output signal was measured by the jitter measurement circuit, and the resulting logic analyzer results were compared to the results from the Wavecrest SIA-3000 signal analyzer (Figure 14).

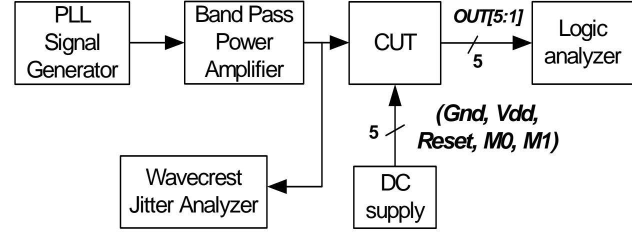

Figure 14: Jitter measurement setup.

To inject jitter into the PLL output signal, this signal is first passed through a power amplifier with a bandpass filter of variable amplitude response and center frequency. The filter creates controllable additional phase noise which in turns results in timing jitter of the PLL signal. The power amplifier is adjusted to provide the correct signal amplitude range for both the Wavecrest instrument and for our circuit. The PLL signal, after the jitter injection and the amplification, is simultaneously applied to the Wavecrest SIA-3000 instrument and to our circuit to compare the measured results.

The results of a single chip measurement comparison are displayed in Figure 15. Period jitter was determined from the device under test (DUT) using equation (1), where M=5000 and T_{AVG} was 1.25 ns. We collected only 5000 samples for this test. Since the minimum step size (or resolution) of our circuit is 55 ps (Table 4), the raw data in Figure 15 shows this lower limit. The key difference in the results in Figure 15 is also due to post-processing method. Wavecrest values are computed using their tail-fit algorithms while our results were computed using equation (1) without building a histogram. The measured accumulated jitter by our circuit was on average 50 ps higher than what the Wavecrest value, mainly due to the limited resolution and the lack of statistical analysis. With a larger number of samples and a histogram-based analysis, we expect the difference to be about 20 – 30 ps, or 15% of the measured jitter values. Considering that this jitter measurement circuit is designed for the first time and is architecturally much simpler than the Wavecrest SIA-3000, the 15% difference is rather encouraging. With better layouts and more robust design methods, the on-chip measurement circuit would approach the same level of accuracy.

$$J_{RMS} = \sqrt{\frac{1}{M}\sum_{n=1}^{M}(T_N - T_{AVG})^2} \qquad (1)$$

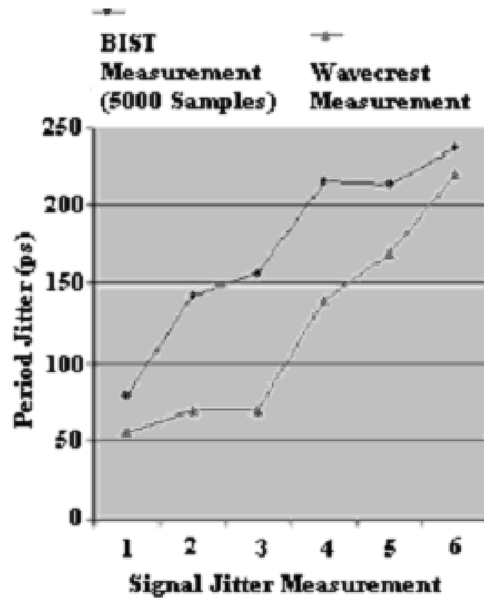

Figure 15: Period jitter measurement comparison.

6. Design limitations

The goals not obtained by the present design were high resolution (<10 ps) and good immunity to mismatch. The simulated resolution for this design was 70 ps and the measured resolution in single-shot measurements is 55 ps. With repeated measurements to average out noise and with calibration, the resolution is closer to 30 ps. This is still higher than the desired value of 10 ps, but is reasonable for a first prototype. The DNL values are within 0.5 LSB, higher than simulated results but still within specifications. The INL values are higher due to the variations of the comparator thresholds over a large number of comparators.

Choices made in the current design that limited the measurement resolution were the threshold spacing between comparator chains, charge pump speed and the use of high N values to divide down the input signal. Due to the novel comparator design used to minimize area and eliminate analog components, conservative threshold spacings were used. Smaller threshold spacing tests were left to sub-circuits placed on the fabricated device, and show that the separations can be decreased to improve the resolution of the circuit. Since the comparator gate capacitance was used as the load capacitance for the charge pump, the amount of current drive was limited to maintain a fairly linear charge output.

The simulation of the comparator chains took into effect process mismatches by creating a cascaded 8-4-1 inverter combination. The layout was not designed to minimize mismatches due to limitations in layout time. Taking into account wafer gradients and not using minimum channel length (L) values in the transistors would possibly decrease the INL and DNL to values closer to the desired values.

7. Design improvements

To address the design limitations discussed in the previous section, the following future improvements could be made. Since measurement resolution is the highest priority for the future design, changes that would create <10 ps resolution are the most important. Nonlinearity at the output, due to speeding up the charge pump to gain measurement resolution, can be calibrated out using the obtained time-to-code mapping. This would also allow for smaller N values to divide down the input frequency, which directly correlates to the resolution.

Since the division circuit reduces the resolution and prevents the design from working at higher frequencies, it is possible to completely remove this component of the design. It only adds functionality of measuring more than one input frequency. It is possible to decrease the wide input frequency range and improve the resolution of the circuit by removing this section of the design. This would also decrease the number of input pins necessary.

The results from the single comparator chains with smaller threshold spacing show that the thresholds can be placed closer together, which would improve the circuit resolution. Further testing can be completed to analyze layout noise issues so that multiple full designs can be fabricated on the same chip without negatively affecting each other. With smaller separations an 8-bit output is possible.

Another way to increase the resolution of the design is to develop a different control signal generator that measures the difference in time between cycles rather than the entire time of a cycle. This reduces the measurement range required for the comparators since only a fraction of the input period will be measured. This allows each bit to represent a smaller time value. Figure 16 shows the idea for measuring cycle-to-cycle jitter instead of period jitter. The voltage controlled delay element will be calibrated to create a signal path delay of one period using a delay locked loop. The difference between the two periods will control the charge pump. This new front end can also be used in parallel with the original control signal generator to allow for different resolution settings.

Another limitation of the presented design is the high INL and DNL created by the nonlinearity in the charge pump and process variations within the threshold voltage values of the comparator chains. By obtaining an output code-to-time mapping and calibration, the effect of the large INL and DNL will be negligible. Larger channel length values should be used to minimize mismatch between sensitive parts.

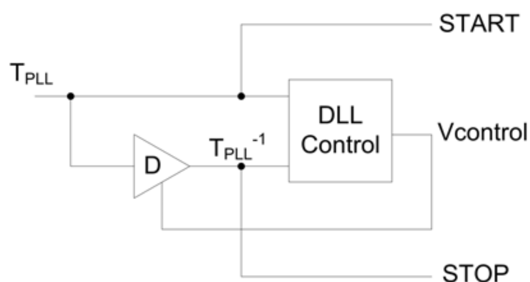

Figure 16: Cycle-to-cycle jitter measurement control.

8. Comparison with previous works

An analysis between existing on-chip fabricated jitter measurement techniques and the proposed method is performed based on the following criteria:

1. Functionality at GHz frequencies
2. Quick measurement (<1 ms/5000 samples)
3. High resolution (<10 ps)
4. Immunity to noise and mismatch
5. Digital components
6. Minimal inputs and outputs
7. Minimized area

For the first criterion, undersampling by ATE [2] is not technically a BIST method and therefore is removed from the analysis. The ADC sampling method was demonstrated at 75 MHz and is limited by the speed of the ADC [1]. The DLL method was shown to operate at 240 MHz [4]. The full VDL method was demonstrated at 125 MHz [5] while the component invariant VDL was demonstrated to operate at 20 MHz [6]. The proposed technique measures up to 1.4 GHz signals using a divide-by-N approach. This method can be scaled to measure higher frequencies, with the fundamental limitation imposed by the speed of the D flipflops and counters.

Measurement time is another critical part of IC testing. The BIST jitter measurement methods include DLL, VDL, and component-invariant VDL. The DLL implementation would take approximately 15 ms to measure 5000 samples with 30 taps at 10 MHz. The VDL method would take approximately 5 μs to measure 5000 samples with a reference clock period of 1 ns. On the other hand, component-invariant VDL method takes more time than VDL. If the period of the clock-triggered oscillator is 0.5 ns and the timing resolution is 1 ps, it will take approximately 0.625 ms/N_{oc} for the total test time. For the same performance, component-invariant VDL would require 125 data-triggered oscillators.

When a 1.25 ns period signal was applied, the total sampling time for a 5000-measurement sample was 50 μs. Therefore the proposed method is faster than ADC sampling, current DLL methods, and invariant VDL.

Resolution of the jitter measurement is another important criterion. Undersampling can measure 1 ps resolution at 500 MHz while ADC sampling can measure 1.3 ps at 75 MHz. The full VDL has been shown to measure 30 ps resolution while at 125 MHz [5]. The component-invariant VDL measures 122 ps at 20 MHz. The proposed method was able to measure 30 - 50 ps RMS accumulated jitter over 8 cycles (4 to 6 ps per cycle) for a 1 GHz input signal. The potential resolution being 12 - 16 ps RMS accumulated jitter over 8 periods if tighter voltage threshold spacing were used in the ADC. The proposed technique raw resolution is limited by the ADC, or more exactly, the spacing of the reference levels in the ADC. A cycle-to-cycle jitter measurement method would increase the resolution significantly with minimal changes in the design.

Noise and mismatch is another concern for BIST. The component-invariant VDL eliminates the mismatch issues inherent in the VDL delay elements at the expense of test time or area. The INL values for fabricated VDL implementations, resulted in approximately 1 LSB. This can be calibrated out by use of a time-to-code mapping, but requires external testing equipment to do so. The INL and DNL of the component invariant VDL was smaller than 0.5 LSB, creating less need for a time-to-code mapping calibration step. Test results from the proposed design revealed an INL of 1.0 LSB meaning that nonlinearity in the charge pump output was an issue. Possible errors at the output due to noise in charge pump were minimized by careful spacing of the threshold levels of each comparator. Mismatches between individual comparators were minimized through careful design and layout of parallel inverter combinations. VDL, component-invariant VDL, and our method all use digital components.

The proposed method only requires the signal under test as the input signal. Extra select bits can be used to test at multiple frequencies, but are not necessary. For other test methods such as ADC sampling, VDL, and component-invariant VDL, an additional reference clock signal is needed. The number of outputs for all on-chip testing is determined by the resolution of the measurement. The outputs can be minimized to only one output signal, which can be serially clocked out with a control input. Overall this design could only require three I/Os, whereas the other on-chip solutions will require more due to an additional reference clock.

Area is another concern for BIST. VDL, component-invariant VDL, and the proposed method are implemented on-chip. Component-invariant VDL takes 0.12 mm^2 using a 0.18 μm process and the full VDL takes 10 mm^2 in a .7 μm process. The proposed implementation takes only 0.0575 mm^2 using a 0.25 μm process. All techniques use an external tester to obtain the histogram to minimize on-chip data storage.

9. Summary of key features

The proposed design has been fabricated and tested. It operates up to 1.4 GHz and measures accumulated jitter over a selectable number of periods. The design is easily modified to improve resolution and to increase the input frequency. The circuit can be redesigned to handle higher frequencies by resizing the charge pump or redesigning the flip-flops in the control signal generator. These flip-flops limit the maximum frequency and are not necessary for the circuit to measure jitter. The resolution can be improved by redesigning the control signal generator for cycle-to-cycle jitter measurement or by decreasing the threshold spacing between the comparator chains.

The method does not require external references for the comparators, and works for higher frequencies. The input frequency range is wide with selectable dividing ratio, so several PLL signals can be measured using the same unit. The linearity parameters can be improved using better circuit and layout techniques to reduce process variations, and calibration can be used for better accuracy.

10. Conclusion

This paper presents an on-chip all-digital CMOS circuit to measure accumulated jitter over N periods. Measurement results from fabricated chips show that a maximum input clock signal of 1.4 GHz can be measured with 30 - 50 ps RMS accumulated jitter resolution. Design improvements from architectures to circuits are discussed and the method has potentials in other timing measurement applications.

10. Acknowledgments

Partial financial support (including test resources support) is provided by National Science Foundation Grant #CCR-0120255, ITR Grant, SRC Contracts #2000-TJ-860, 2001-HJ-926, and 2001-TJ-916. We would like to thank National Semiconductor Corporation for the PLL circuit used as a case study and for technical discussions regarding jitter measurement.

References

[1] S. Cherubal, A. Chatterjee, “A High-Resolution Jitter Measurement Technique Using ADC Sampling”, Proc. IEEE International Test Conference, pp. 838-847, 2001

[2] W. Dalal, D. Rosenthal, “ Measuring Jitter of High-Speed Data Channels using Undersampling Techniques”, Proc. IEEE International Test Conference, pp. 814-818, 1998

[3] M. Mota, J. Christiansen, “A four-channel self-calibrating high-resolution time to digital converter”, IEEE International Conference on Electronics, Circuits and Systems, 1:409-412, 1998

[4] S. Sunter, A. Roy, “BIST for Phase-Locked Loops in Digital Applications”, Proc. IEEE International Test Conference, pp. 532-540, 1999

[5] N. Abaskharoun, M. Hafed, G. W. Roberts, “Strategies for on-chip sub-nanosecond signal capture and timing measurements”, Proc. IEEE Custom Integrated Circuits Conference, pp. 251-254, 2001

[6] A. H. Chan, G. W. Roberts, “A synthesizable, fast and high-resolution timing measurement device using a component-invariant Vernier delay line”, Proc. IEEE International Test Conference, pp. 858-867, 2001

[7] O. Sasaki, T. Taniguchi, T. K. Ohska, H. Kurashige, “A high resolution TDC in TKO BOX System”, IEEE Transactions on Nuclear Science, Vol. 35, No. 1 pp. 342-345, 1988

[8] H. Lin, K. Taylor, A. Chong, E. Chan, M. Soma, H. Haggag, J. Huard, and J. Braatz, “CMOS Built-In Test Architecture for High-Speed Jitter Measurement”, Proc. IEEE International Test Conference, pp. 67-76, 2003

[9] R. Szplet, J. Kalisz, “Interpolating Time Counter with 100 ps Resolution on a Single FPGA Device”, IEEE Trans. Instrumentation and Measurement, pp. 879-883, 2000

[10] P. O’Connor, G. De Geronimo, A. Kandasamy, “Amplitude and Time Measurement ASIC with Analog Derandomization”, IEEE Nuclear Science Symposium Conference Record, pp. 327-331, 2002