

MRAM Defect Analysis and Fault Modeling

Chin-Lung Su, Rei-Fu Huang, and Cheng-Wen Wu

Department of Electrical Engineering
National Tsing Hua University
Hsinchu, Taiwan 30013, ROC

Chien-Chung Hung and Ming-Jer Kao
Electronics Research and Service Organization
Industrial Technology Research Institute
Hsinchu, Taiwan, ROC

Yeong-Jar Chang and Wen-Ching Wu
SoC Technology Center
Industrial Technology Research Institute
Hsinchu, Taiwan, ROC

Abstract

With the advent of system-on-chip (SOC), the demand for embedded memory cores increases rapidly. The Magnetic Random Access Memory (MRAM) is considered one of the potential candidates that will replace current on-chip memories (RAM, EEPROM, and flash memory) in the future. The MRAM has a high speed and does not need high supply voltage for Read/Write operations, so it has the advantages of RAM and flash memory, making it a potentially good choice for SOC. The testing of MRAM, however, has not been fully investigated. In this work we classify and analyze the MRAM defects and their behavior, and propose its fault models. We have built a SPICE model of MRAM cell and performed defect injection and simulation of a real MRAM circuit. The circuit has been implemented and fabricated with a novel $0.18\mu\text{m}$ technology. The simulation results regarding the correlation between the defects and conventional fault models show that most of the defects can be covered by the stuck-at fault model. The test data based on the fabricated chips show that the stuck-at faults do cover most of the defects on the chips. However, from the experiment we also have identified two new faults, i.e., the Multi-Victims fault and Kink fault.

1 Introduction

According to ITRS [1], embedded memories is occupying a major part of the area of a typical system-on-chip (SOC). Many diversified applications require the SOC to integrate non-volatile memories. Although flash memory is widely used today, it needs high voltage for Program and Erase operations and has reliability issues that are hard to handle [2], increasing the cost of circuit design and process integration. The industry has been trying to find a good alternative non-volatile memory that

can replace flash memory. Possible candidates include magnetic random access memory (MRAM), ferroelectric random access memory (FeRAM), Ovonic memory, etc. Among them, MRAM has been identified as having the potential to become a universal on-chip memory. It is a high-speed, low-voltage, and high-density non-volatile memory with virtually unlimited Read/Write endurance. The data-storing mechanism of MRAM is based on the resistance change of the magnetic tunnel junction (MTJ) device [3]. The MTJ device has two types as classified by magnetoresistive phenomena: giant magnetoresistive material (GMR) [4, 5] and tunneling magnetoresistive material (TMR) [6–10]. They have different magnetoresistance ratio (MR), which is the ratio of the difference of the resistance values in parallel state and antiparallel state to the resistance value in parallel state. The MR of TMR is higher than that of GMR, and according to recent research reports the MR of TMR is about 45%. In [7] a 1-Mbit MRAM has been presented. However, the testing of MRAM is yet to be investigated. Systematic approaches for testing flash memories have been proposed [11–15], in which fault models that capture the characteristics of disturbances and test algorithms to detect these faults are proposed. In [16–18], layout-based defect and fault analysis approaches and tools have been presented, and the SRAM delay fault models are also proposed.

In this paper we classify and analyze the MRAM defects and their behavior, and propose its fault models. We present a SPICE model for MTJ device based on its physical characteristics, and perform defect injection and simulation of a real MRAM circuit that integrates the MTJ device into the MRAM cell array, with a complete peripheral circuit that includes address decoders, sense amplifiers, and reference cells. Defect injection is based on a real layout and the physical model of MRAM cell, with parameters obtained from an experimental process line built in the Industrial Technology Research Institute (ITRI). A systematic defect analysis procedure has been

developed. The circuit has been implemented and fabricated with a novel $0.18\mu\text{m}$ technology. The simulation results regarding the correlation between the defects and conventional fault models show that most of the defects can be modeled by stuck-at faults. The test results from the fabricated chips show that indeed most defects are covered by the stuck-at fault (SAF) model. However, from the experiment we also have identified two new faults, i.e., the Multi-Victims fault (MVF) and Kink fault (KF). We will describe the characterization of these faults, and propose a test scheme for them.

The rest of the paper is organized as follows. Section 2 introduces the basic structure of MRAM cell array and some characteristics of the MTJ cell. The MRAM circuit model is described in Sec. 3. In Sec. 4, the defect injection and systematic simulation flow is described. Section 5 summarizes the experimental results. Finally, Sec. 6 concludes the work.

2 Magnetic RAM (MRAM)

The MRAM cell used in this work is a typical one-transistor-one-MTJ (1T1MTJ) cell, and the data is stored in the MTJ device. The material layers of the MTJ device is shown in Fig. 1. As the figure shows, the MTJ device has a complex material structure, containing layers of PtMn, CoFe, Ru, Al_2O_3 , NiFe, etc. [7, 9, 10]. These material layers are grouped into the antiferromagnet (AF) pinning layer, pinned (ferromagnetic) layer, and free (ferromagnetic) layer. The pinned layer is the synthetic antiferromagnet (SAF) layer, which is a pinned magnet. The MTJ memory cell stores data bit in one of two possible relative orientations of its free magnet to its pinned magnet—either a parallel orientation or an antiparallel orientation. Different orientations have different resistance values. The resistance value of the antiparallel orientation (R_{ap}) is larger than the parallel one (R_p), and the 'Read' circuit can detect the state of the memory cell by assessing the MTJ resistance. The sense amplifier compares the resistance value with that of the reference cell and determines the data bit stored.

The change of the memory cell state is done by reversing the orientation of the free magnet. We use a switching astroid curve to describe the boundary of switching the orientation for the free magnet. Figure 2 shows the ideal switching astroid curve of the MTJ [3, 5, 10], with respect to the easy field axis (H_{easy}) and the hard field axis (H_{hard}). The H_{hard} represents the field along the width of the MTJ, and H_{easy} is that along the length of the MTJ. The ideal switching astroid satisfies the relation

$$H_{\text{easy}}^{2/3} + H_{\text{hard}}^{2/3} = H_{\text{k}}^{2/3}, \quad (1)$$

where the H_{k} is the anisotropic field. In general, the actual switching astroids of MTJs in a real memory cell ar-

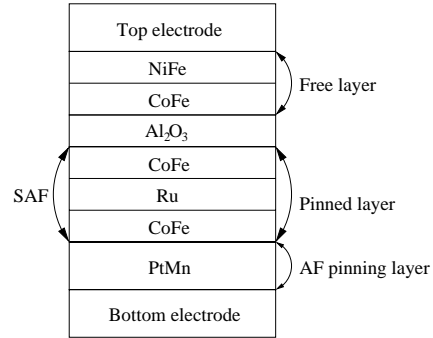


Figure 1: Material layers of the MTJ device.

ray are not ideal, and they are not identical. The curves depend on many factors, e.g., MTJ's shape, edge roughness, surface condition, etc., though they are similar to each other. Of course the MTJs must have a consistent behavior to serve as viable memory elements for an MRAM chip. When the magnet exceeds the switching astroid boundary, it can change the MTJ to a given state (the Write operation). In Fig. 2, it is easy to see that writing the MTJ cell with a single field is in general harder than writing it by dual fields, whether it is H_{hard} or H_{easy} . The MRAM operating region is highlighted in Fig. 2.

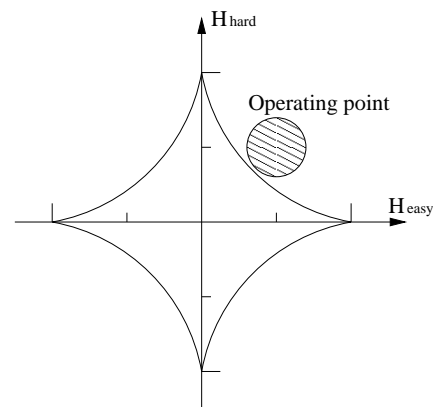


Figure 2: Ideal switching astroid.

Figure 3 shows the basic 1T1MTJ MRAM cell [6, 9, 10]. In this figure, the MRAM cell has three operating lines—the bit-line, Read word-line, and Write word-line. The Read word-line connects the Gate of the MOS transistor that sits under the MTJ device. During the Read operation, the Read word-line turns on the MOS transistor and the sense amplifier can sense the resistance value of the MTJ device through the bit-line. In the Write operation, both the two fields are used for writing the data to the MTJ device (switching the orientation of the free magnet). The Write word-line is used to provide a field for switching the orientation of the free magnet easily, and the orientation of the free magnet depends on the

current direction of the bit-line. The Write word-line is turned off during the Read operation, so the magnet generated from the bit-line alone does not change the state of the MTJ device.

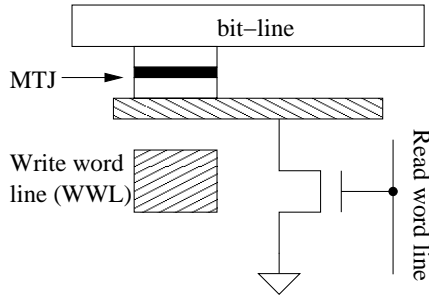


Figure 3: 1T1MTJ MRAM cell.

The switching of the free magnet between the two polarization states is a hysteresis, giving the MTJ device two stable memory states. Figure 4 shows an MTJ device hysteresis loop [5, 7]. The shape of the hysteresis loop can be affected by the materials of the MTJ device. Surface and junction roughness of the magnetic layers also affects the loop, causing a weak ferromagnetic coupling and shifting the hysteresis loop. In the figure, the magnetoresistance ratio (MR) also is indicated, which can be represented by the following equation:

$$MR = \frac{R_{ap} - R_p}{R_p} \quad (2)$$

The vertical axis in Fig. 4 is the resistance value of the MTJ device, and the horizontal axis is the bit-line current. The resistances of the two states are denoted as the antiparallel orientation resistance (R_{ap}) and parallel orientation resistance (R_p), respectively. If the Write word-line current is zero, the hysteresis grows wider (shown in dashed lines) and the bit-line current threshold (for state change) increases. In other words, the change of free magnet orientation is harder when the Write word-line is turned off—the same behavior as described with the astroid curve.

The Read operation of MRAM is done by sensing the resistance value of the MTJ device. Each block of memory cells has one pair of reference cells for resistance value comparison, which is composed of two MTJ cells—one in parallel orientation and the other in antiparallel orientation. The data value stored in the MRAM cell depends on whether the resistance value is larger or smaller than the average value of the reference cells.

3 MTJ Device Modeling

We now present a SPICE model for MTJ device based on its physical characteristics. The MTJ device is a mag-

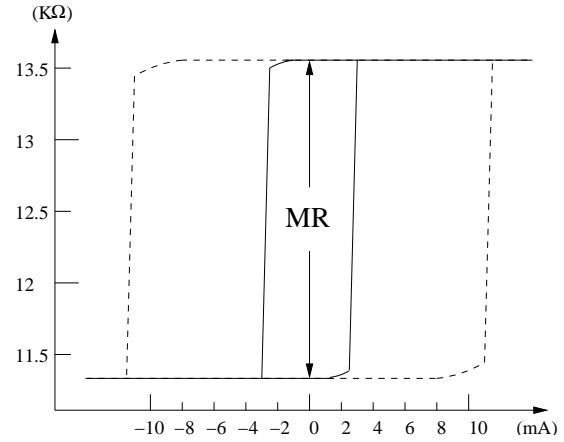


Figure 4: Hysteresis loop of the MTJ device.

netic device, so it is hard to present its characteristics in an electronic circuit using SPICE. We have developed an acceptable SPICE model that consists of three main parts, i.e., the input stage, stable-state stage, and output stage. These three parts together satisfactorily model the physical characteristics and behavior of the MTJ device. They are described next.

3.1 Input Stage

The input stage of the MTJ device is shown in Fig. 5, which represents the main function of the Write operation. The Write word-line controls the controlled voltage source shown in the right part of the figure. The current source in the left part simulates the bit-line current. The Write operation needs both fields to be exercised in order to change the state of the MTJ device, as described in Sec. 2, so there are two sources in this model. The Write word-line represents the source for Write operation that provides a field for reducing the width of the hysteresis loop, and the current source provides the other field for determining the orientation. The data stored depends on the current direction of the current source (i.e., the bit-line current). If the Write word-line is off, the current is not strong enough to change the stored data. However, if the current from the current source is too large due to some defects, it may also change the state of the MTJ device. This behavior is used to simulate the behavior of the switching astroid curve, as shown in Fig. 2. This model can be used to simulate both the fault-free and faulty behavior of the MTJ device.

3.2 Stable-State Stage

The stable-state stage is composed of a capacitor and two diodes, as shown in Fig. 6. These two diodes are

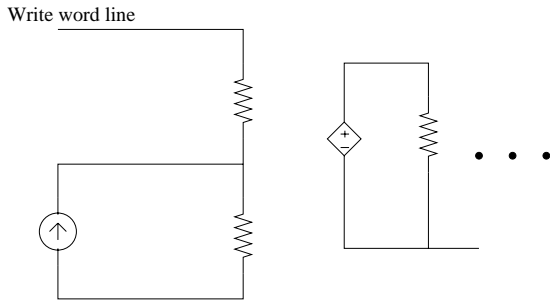


Figure 5: Input Stage SPICE model of the MTJ device.

placed in opposite directions, and each of them has a self-bias. They are used to simulate the two stable states as shown in Fig. 4. For example, if the hysteresis loop is not balanced, the behavior can be simulated by adjusting the bias of the capacitor. Because the stable state is controlled by the previous stage, the supply voltage is a controlled voltage source that is controlled by the previous stage. In Fig. 4, the state switching is not ideal—the transition does not change immediately when we reach the current threshold, i.e., it requires a transition period. The capacitor in this stage is used to simulate this effect—it is used to adjust the slope of the hysteresis loop.

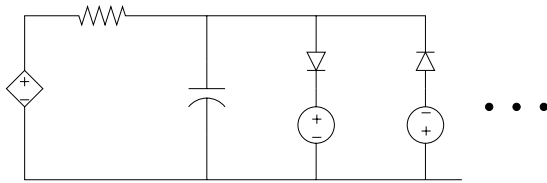


Figure 6: Stable-state stage SPICE model.

3.3 Output Stage

This stage is used to simulate the output stage of the MTJ device. It is for adjusting the resistance values of the MTJ device, including the antiparallel orientation and the parallel one. As shown in Fig. 7, there are two controlled current sources and three resistors in this stage. Note that one of the resistors in this stage has a negative resistance. Its function is similar to the sense amplifier of a RAM. It can increase the difference of two levels and reduce the action time of the output stage. The other two resistors are used to adjust the resistance value of the MTJ model. The bit-line node is connected to the sense amplifier, and the sense amplifier compares its resistance value with the reference pair to determine the value of the stored data.

The whole SPICE model of the MTJ device is shown in Fig. 8. This model includes the three stages and some extra circuits, and it can be connected to real peripheral circuits of the MRAM. The upper part of Fig. 8 shows

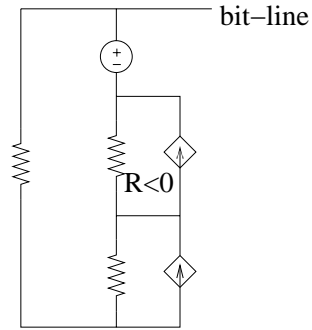


Figure 7: Output stage SPICE model.

the MTJ device model. The MRAM cell is composed of a MOS transistor and an MTJ device (i.e., 1T1MTJ). This cell is connected to the bit-line, Write word-line, and Read word-line, as Fig. 8 shows. This model is simple and effective in simulating the MTJ device. The simulation performed by using this model thus has a high efficiency.

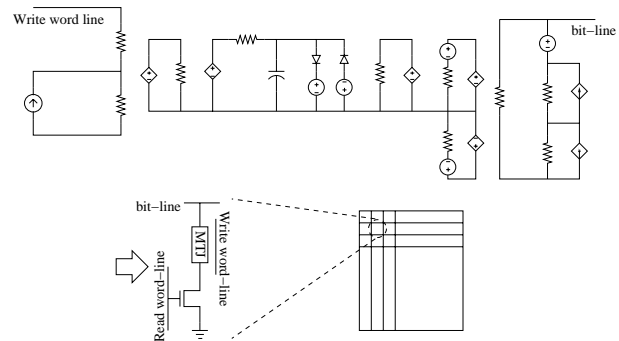


Figure 8: SPICE model of the MTJ device.

4 Defect Injection and Simulation

The MRAM cell is in fact simpler than the SRAM cell, so far as structure is concerned. The defects to be injected for simulation and analysis includes resistive shorts, line breaks, MOS stuck defects, coupling defects, and some defects related to the MTJ device.

4.1 Defect Injection

The defects considered are those on the cell array only, as they are the major difference between SRAM and MRAM. Defect injection is highly dependent on the physical design of the device. We list and explain all the considered defects below.

- Resistive short defects: The resistive short defects may occur in many positions of the circuit. To simu-

late all possible resistive short defects is impossible, so we only describe some important short defects here.

- Write word-line shorted to VDD or VSS: The defect may occur in the Write word-line, address decoder, word-line driver circuit, etc.
- Read word-line shorted to VDD or VSS: The Read word-line is connected to the gate of the switching MOS under the MTJ device, so it can be shorted to VDD or VSS.
- Bit-line shorted to VDD or VSS: The bit-line can be shorted to VDD or VSS. Because the bit-line is connected to the sense amplifier, some defects in the sense amplifier can have a similar behavior, so they are also covered.
- MOS stuck defects: A 1T1MTJ memory cell has a single MOS transistor, which may have defects leading to stuck-on or stuck-off behavior.
- Line break defects: There are three main operation lines in the memory cell array, i.e., the Read word-line, Write word-line, and bit-line. These lines are longer ones in the cell array, so they have higher probability for line break.
- Coupling defects: The coupling defects defined here can occur between neighborhood long lines and between adjacent layers. The Write word-line has the same direction with the Read word-line, but in our design one runs on the middle metal layer and the other on poly-silicon. Although the Write word-line and bit-line run on neighboring layers, they are in different directions (i.e., perpendicular to each other) and only cross at the MTJ region. Therefore, the coupling defects between neighboring layers are less likely to occur, and we consider only coupling on the same layer, i.e., those between Write word-lines, between Read word-lines, and between bit-lines.
- MTJ device defects:
 - MTJ open defect: Some defects may lead to an open MTJ device (i.e., the device is floating), which may result in a large resistance between the bit-line and the switching MOS transistor.
 - MTJ tunneling defect: This defect results in the bit-line being shorted to the switching MOS transistor.
 - Rough junction defect: Smooth junction between the layers is important. If the junction is too rough, the hysteresis loop will shift. This defect is also called topological coupling [7, 10]. Figure 9 shows the effect of the rough junction defect. Note that it may shift in the opposite direction.

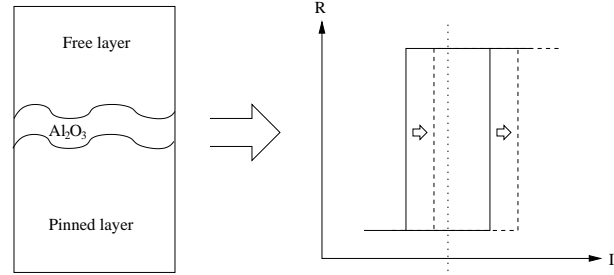


Figure 9: Effect of the rough junction defect.

One important note is that the magnetic field can be considered as composed of many small magnetic components, and the state change is the result of the change of most of the small magnetic components. If a weak magnetic field changes some small magnetic components, these components will be recovered by other components when the magnetic field disappears. Therefore, the MRAM does not have the disturbance faults as widely considered in flash memories. This type of defect thus is not discussed here.

4.2 Defect Analysis

The defect analysis methodology is similar to that for SRAM [17]. It is a systematic and efficient approach to analyzing the memory circuit under the attack of various defects. Figure 10 shows the major steps and tools of the proposed defect analysis and diagnosis system. We use our own RAM fault simulator called RAMSES [19]. Given the RAM cell array circuit and test algorithm, we inject the defects one by one, as discussed above. After a defect is injected, we perform the circuit simulation using the specified March test algorithm. The *March signatures* (also called *traces* or *syndromes* [19–21]) of the faulty memory will be derived. A March signature for a fault under a test algorithm is a vector that records the Read operations in the test that detect the fault. The signatures of the functional faults derived from RAMSES are then compared with the signatures obtained from the injected defects. We group the defects that result in the same signature with a functional fault into an equivalent defect class. Using the signatures, a faster switch-level simulator instead of a circuit-level simulator (such as SPICE) can be used [22], greatly reducing the simulation time. After comparing the defect signature with the fault signature, possible defects that lead to a certain fault can be identified. Moreover, based on the analysis result more realistic functional faults can be defined for different memory circuits, and unrealistic faults can be dropped. The information also helps one optimize the test algorithm. Finally, the simulation result also provides the number of the first detected defects for each Read operations, which can be used to further shorten the test al-

gorithm under the specified test constraints.

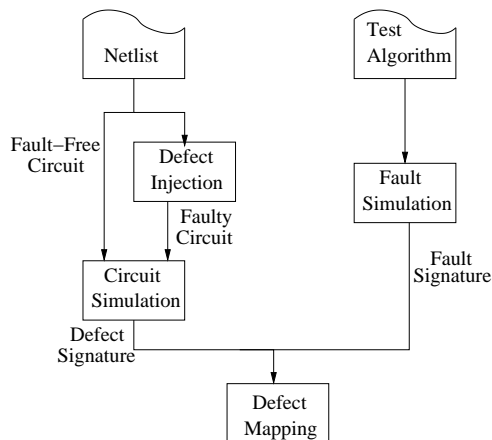


Figure 10: The proposed defect analysis and diagnosis system.

We use a 4×4 MRAM sub-circuit for simulation, with real loads attached, as shown in Fig. 11. The 4×4 cell array is surrounded by dummy cells, word-line loads, and bit-line loads, so realistic behavior can be obtained. The test algorithm we use for this case is the March C– test algorithm [23], which can detect stuck-at fault (SAF), transition fault (TF), coupling fault (CF), address decoder fault (AF), etc. Note that March C– is not good for diagnostics.

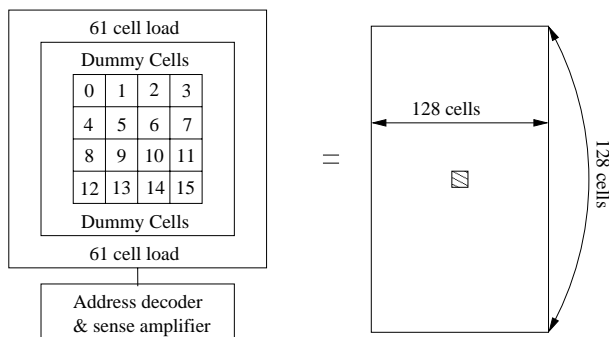


Figure 11: The MRAM sub-circuit with real loads.

Table 1 shows the March signature-based fault dictionary of the March C– test algorithm. It lists the March signatures of the conventional RAM functional faults, including the address-decoder fault (AF), idempotent coupling fault (CFid), inversion coupling fault (CFin), state coupling fault (CFst), stuck-at fault (SAF), stuck open fault (SOF), transition fault (TF), and the fault-free (FF) case. The two parameters inside the parentheses of a coupling fault indicate the operations/states of the aggressor and victim cells, respectively. The symbols D , U , 0, 1, and \sim represent the down transition operation, up transition operation, constant 0 state, constant 1 state, and

inversion operation, respectively. The symbols $>$ and $<$ stand for the relative position between the aggressor and victim cells: the former means that the address of the aggressor is higher than that of the victim, and the latter means the other way around. For example, $\text{CFid}(D;0)<$ denotes the CFid that occurs when there is a down transition in the aggressor that has a lower address than the victim, and the content of the victim is forced to 0. Each column in the table represents one of the 5 Read operations in the March C– algorithm. A dot (.) entry means that the fault will not be detected by the corresponding Read operation. A 1 entry indicates an incorrect Read result where the expected value is 0, while a 0 entry indicates an incorrect Read result where the expected value is 1. Note that in the table $\text{SAF}(0)$ and $\text{TF}(U)$ have the same March signature. It is impossible to differentiate these two faults if we initialize the memory cell array by the all-0 data background [20], unless timing effect is considered.

Table 1: Fault dictionary of the March C– test algorithm.

Fault Type	R_1	R_2	R_3	R_4	R_5
FF
SAF(0)	.	1	.	1	.
SAF(1)	0	.	0	.	0
TF(U)	.	1	.	1	.
TF(D)	.	.	0	.	0
SOF(H)	.	1	.	.	.
SOF(T)	.	.	0	1	0
CFin(D; \sim)<	.	1	.	.	0
CFin(D; \sim)>	.	.	0	1	.
CFin(U; \sim)<	0	.	.	1	.
CFin(U; \sim)>	.	1	0	.	.
CFst(0;0)<	.	1	.	.	.
CFst(0;0)>	.	.	.	1	.
CFst(0;1)<	.	.	0	.	0
CFst(0;1)>	0	.	.	.	0
CFst(1;0)<	.	.	.	1	.
CFst(1;0)>	.	1	.	.	.
CFst(1;1)<	0
CFst(1;1)>	.	.	0	.	.
CFid(D;0)<	.	1	.	.	.
CFid(D;0)>	.	.	.	1	.
CFid(D;1)<	0
CFid(D;1)>	.	.	0	.	.
CFid(U;0)<	.	.	.	1	.
CFid(U;0)>	.	1	.	.	.
CFid(U;1)<	0
CFid(U;1)>	.	.	0	.	.
AF<	0	1	.	.	.
AF>	.	.	0	1	.

5 Experimental Results

5.1 Simulation Results

In this work, the defect injection is done at cell 10 (see Fig. 11). The MR of the MTJ device in this experiment is about 20%. The pre-process (for the peripheral circuits) is done by a standard $0.18\mu\text{m}$ CMOS technology. After the pre-process, we add the MTJ devices and the

interconnects using our own MRAM technology [9]. The R_p and R_{ap} values are $11.3\text{K}\Omega$ and $13.6\text{K}\Omega$, respectively. These values come from the measurement results of a real chip. Table 2 shows the simulation results. Where WWL, RWL, and BL denote the Write word-line, Read word-line, and bit-line, respectively. The first column of this table shows the defects as described in Sec. 4.1. The second column shows the resulting faulty cells after the respective defects are injected. The cells can be identified in Fig. 11. The third column shows the behavior of the faulty cells, i.e., their fault models. If the fault is un-modeled (e.g., the first defect in Table 1), its faulty syndrome is presented.

Table 2: MRAM defect mapping table.

Defect	Faulty cell	Behavior
WWL shorted to VDD	8, 9, 10, 11	<0101.>
WWL shorted to VSS	8, 9, 10, 11	SAF(1)
RWL shorted to VDD	0–7, 12–15	SAF(0)
RWL shorted to VSS	8, 9, 10, 11	SAF(1)
BL shorted to VDD	2, 6, 10, 14	SAF(1)
BL shorted to VSS	2, 6, 10, 14	SAF(0)
MOS stuck-on	2, 6, 14	SAF(0)
MOS stuck-off	10	SAF(1)
WWL break	10, 11	SAF(1)
RWL break	10, 11	SAF(1)
BL break	10, 14	SAF(1)
BL and BL coupling		FF
WWL and WWL coupling		FF
RWL and RWL coupling		FF
MTJ open	10	SAF(1)
MTJ tunneling	10	SAF(0)
Rough junction	10	FF or TF or SAF

From Table 2, we see that most of the defects are mapped to the stuck-at faults, and they affect the cells on the same row (the Read/Write word-line) or column (the bit-line). The Write word-line shorted to VDD is an un-modeled fault, and it can be detected by the first four Read operations. Because the Write word-line is always on, when we access another cell (on a different word-line) by supplying current to its bit-line, it may trigger the Write operation to the cell on the same bit-line (and the faulty word-line). The data stored in the MTJ device thus may be modified. The behavior of this defect is not the same as any of the conventional fault models. The Read word-line shorted to VDD affects more cells, because the Read current on the bit-lines can leak from the cells on this Read word-line. Other cells, except those on this Read word-line, are stuck-at 0—this defect affects all cells in the cell array except those on this Read word-line. The faulty behavior of the MOS stuck-on defect is similar to this defect. The last defect shown in the table has multiple faulty behaviors, depending on the severity (or size) of the defect, i.e., the degree of roughness of the junction. The rough junction defect can shift the hysteresis loop, and the faulty behavior depends on how much the loop is

shifted. If the shift is small, it may not affect the MTJ device and the MRAM may look fault-free. When the shift becomes larger, the transition fault will be seen. If the defect is large enough and the hysteresis loop shifts even more, the faulty behavior becomes the stuck-at fault.

There are other possible defects in the MRAM circuit, but it is impossible to simulate all the defects. The coupling defects shown in Table 2 all result in a fault-free behavior under the given test algorithm. Note that the coupling defects are simulated by injecting capacitors between the affected pairs of lines, so the behavior depends on the injected capacitance. The initial value of the MTJ device is at the 1 state, and the initial free magnet to pinned magnet are in antiparallel orientation, so the faulty behavior of the Write word-line shorted to VSS defect is the stuck-at 1 fault. Because the Write word-line is always off and no data can be written to the MTJ devices on this Write word-line, the read out data is the initial state (high impedance state) of the the MTJ device.

The MSCAN test algorithm with solid background and checkerboard background are also applied to the MRAM circuit and simulated. We have injected the defects at cell 10 of the memory cell array, too. The simulation results are similar to that shown in Table 2, with the difference listed in Table 3. The behavior of other injected defects not described in this table are the same with that shown in Table 2—the test result of the March C– algorithm. The only difference is the defect where the WWL is shorted to VDD. Because the MSCAN test algorithm with solid background writes all cells to the same state before reading them, the interaction of the Read/Write operations between memory cells is not available. The behavior of this defect becomes fault-free (FF) under the MSCAN test algorithm with solid background. The checkerboard background does not always detect this defect. It observes the data only at some special locations, where the data of the faulty word-line are different from the last word-line. For example, if this defect is injected to cell 6 instead of cell 10, its behavior becomes fault-free. Because the last word-line has the same data with the second word-line, it can recover the value of the second word-line. From the above discussion, we can see that the MSCAN test is not good for this defect, which normally is detected by the (ra,wb) test element. If the defect cannot be neglected in MRAM, the MSCAN test algorithm is not good enough. In that case, the March C– test can be used.

Table 3: Defect mapping with different backgrounds.

WWL shorted to VDD at cell 10		
Background	Faulty cell	Behavior
Solid		FF
Checkerboard	8, 9, 10, 11	Inversion background

Table 2 lists just some of the possible defects and their simulation results. Others can be added easily. The approach is good for MRAM product characterization and diagnosis. We have designed and implemented a real MRAM chip. The test data and analysis results from the fabricated chip are presented next.

5.2 Test Data Analysis

Our MRAM test chip is implemented and fabricated with a novel $0.18\mu\text{m}$ technology. The logic circuits are fabricated with the standard CMOS process, and the MTJ cells are constructed between the Metal-3 and Metal-4 layers. Figure 12 shows a partial bit-map of one of the failed chips, where BL and WL denote the bit-line and word-line directions, respectively. In the bit-map, 1 and 0 represent faulty and fault-free cells, respectively. The cells on each bit-line use the same pair of reference cells (a special design in MRAM), whether they are in the right or left bank of the cell array. If the reference cells mismatch, the shifted resistance value will result in a current that deviates from the middle of the two states. In that case, all cells on this bit-line will fail. On BL-15, all cells are faulty, except the cell on Row 1C. This fail pattern is the same as the MOS stuck-on defect shown in Table 2. We can diagnose the defect with this fail pattern. In this bit-map, we also can see that all cells on the WL-04 are faulty. It may be caused by the Write word-line or Read word-line short defect, according to our simulation result. Our result also shows that a high percentage of defects cause row or column failures.

WL	BL															
	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
00	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
01	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
02	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
03	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
04	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
05	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
06	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1A	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1B	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1D	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1E	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1F	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Figure 12: Partial bit-map of a 1Kb MRAM chip.

We also characterize the defects in the test chips with measured parameters, and compare them with the simulation results. Most of the defects were predicted by the simulation results, but we did find some defects that were un-modeled and not observed in the simulation.

- MTJ process variation: the MTJ cell has a more complicated process that requires many different materials. There are many factors that can cause the MTJ device to fail. According to our measurement result, the thickness of some layers of the MTJ device (e.g., Al_2O_3) is very hard to control, and the resistance of the MTJ cell increases very quickly as the thickness decreases (10X per \AA). A defect can result in large resistance value of MTJ, which can be mapped to the MTJ open defect.
- Over etching: the MTJ process is not the standard CMOS process—we need to add some extra materials on top of the CMOS devices. The over etching defect may occur at a junction node between the switching MOS and MTJ cell, and it results in a large resistor between the switching MOS and MTJ cell. The fault behavior of this defect is a large resistance value on the reading path. It also can be modeled as an MTJ open defect.
- Over current: this defect is a fatal defect, i.e., the MTJ will be destroyed when it is accessed. After access, the MTJ becomes a broken one, i.e., it is similar to an MTJ open defect.
- MTJ tunneling: the defect may occur due to process variation or particles, and it reduces the resistance value of the MTJ device. It is similar to a short between the switching MOS and bit-line. The behavior of this defect is the stuck-at 0 fault.

The MTJ device is very sensitive to the resistance value, because the difference between R_{ap} and R_p is small—only several $\text{K}\Omega$ s. If the resistance value varies, the output value of the sense amplifier will be different. Therefore, most of the defects in the MTJ device resulting in open or short behavior can be modeled as the stuck-at 1 or 0 fault, respectively.

5.3 MRAM Specific Faults

Here we focus on the defects that can be modeled by the Multi-Victim fault (MVF) and Kink fault (KF) models. These faults are observed and characterized from the test data and the parameters measured.

- Multi-Victim fault (MVF): due to process variation of the MTJ device, its astroid curve may drift. This defect usually affects a cluster of cells, and these affected cells have similar faulty behavior. They can easily change to 0 or 1, depending on the drift direction of the astroid curve. The faulty cells will be easily affected by the neighboring cells when they are executing the Write operation. The behavior of

this fault is similar to a multi-cell coupling fault. Since this fault affects several cells, we call it MVF. Figure 13 shows an example of MVF. The left part of the figure shows the MTJ astroid curve drifts to the left, and right part of the figure shows the corresponding bit-map obtained from a failed chip. In the bit-map, there are eight faulty cells, which are all in the same neighborhood. The number of faulty cells, or the size of the fail region, depends on the degree of the process variation. The Write current of the faulty cells depends on how much the astroid curve drifts.

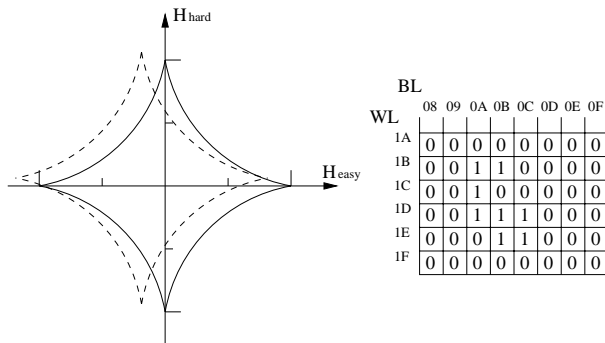


Figure 13: The Multi-Victims fault of MRAM.

- Kink fault (KF): the name KF comes from the kink curve in the hysteresis loop, as shown by the dashed line in the left part of Fig. 14. The kink in the *MR* curve is from the vortex of the MTJ device, which is strongly correlated to the cell shape and saturation magnetization of the free layer. The faulty behavior is shown in the right part of Fig. 14, where the faulty loop is indicated by the dashed lines. If the *MR* curve is affected by a kink, the hysteresis loop shrinks and the *MR* is less than the fault-free value. This fault affects the access time of the MTJ device, resulting in a new middle state of the loop—between the R_{ap} and R_p states. The middle state will look random, i.e., the value of the faulty cell may be 1 or 0, depending on the degradation of the *MR* curve. The behavior is similar to a random fault in DRAM.

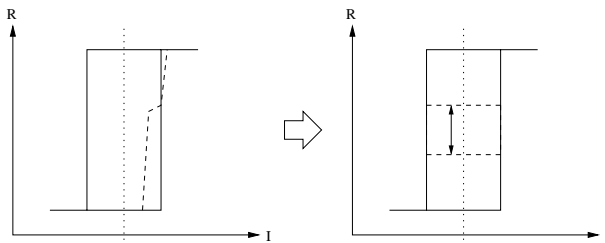


Figure 14: The Kink fault of MRAM.

To detect the two new faults, the test algorithm needs some modification. The MVF can be detected by March C–, though the test is not good for diagnosing the MVF. The KF is harder to detect than other faults. We have done some experiments to characterize this fault. Our experimental results show that the KF disappears if we apply a large current (magnetic field) on it. The large magnetic field resets all cells to their initial state—high impedance state, so the KF will be recovered. The KF appears again after some Read/Write operations, so this fault can be classified as a reliability fault. To detect this fault we reduce the Write word-line current in the faulty cell. The degree of current down grade depends on the MTJ device. In our case it is 90% of the original current. Note that the degraded current must be larger than the threshold current, or it cannot reverse the free layer of the fault-free MTJ device. The degraded current can effectively activate the KF, and the fault effect can be observed by the Read operation. Note that the degraded-current test does not cover all MVF—the smaller current can fail to activate some faulty cells, so the original normal-current test is also needed. The complete test algorithm we use include 1) the March C– test with 100% current and 2) the March C– test with 90% current for KF detection. It is possible to reduce the test time by using a shorter test for KF. The degraded-current test is applied in Step 2, because the KF can be activated more easily after some Read/Write operations. This test scheme may not be the shortest one, but it effectively covers the observed faults on the fabricated chips.

6 Conclusions

We have presented a SPICE model for the MTJ device based on its physical characteristics, and performed defect injection and simulation of a real MRAM circuit. Defect injection is based on a real layout and the physical model of MRAM cell, with parameters obtained from an experimental process line built in the ITRI. We have also presented the defect mapping table for defect simulation, and analyzed the simulation results using a systematic defect analysis procedure. The circuit has been implemented and fabricated. The simulation results regarding the correlation between the defects and conventional fault models show that most of the defects can be modeled by stuck-at faults, and row and column disturbances are possible due to inter-layer (junction) defects. Also, the MSCAN test algorithm is not good enough for MRAM, but the March C– test can be used in general. The approach is good for MRAM product characterization and diagnosis. Based on the test results from the fabricated MRAM chips, most faults are predicted by our simulation, except MVF and KF. To detect these two faults, a degraded-current test has been proposed and shown to be effective. This is the first step toward MRAM testing.

We will continue to modify the model, investigate such defects, and develop suitable test and diagnosis scheme MRAM in the future.

References

- [1] Semiconductor Industry Association, "International technology roadmap for semiconductors (ITRS), 2001 edition", Dec. 2001.
- [2] R. Barth, "ITRS commodity memory roadmap", in *Proc. IEEE Int. Workshop on Memory Technology, Design and Testing (MTDT)*, San Jose, July 2003, pp. 61–63.
- [3] S. Parkin, X. Jiang, C. Kaiser, A. Panchula, K. Roche, and M. Samant, "Magnetically engineered spintronic sensors and memory", *Proc. of the IEEE*, vol. 91, no. 5, pp. 661–680, May 2003.
- [4] R. A. Sinclair, S. A. Mundon, S. C. Aryal, and C. M. Sinclair, "A practical 256K GMR NV memory for high shock applications", in *Proc. Nonvolatile Memory Technology Conf.*, June 1998, pp. 38–42.
- [5] W. Reohr, H. Honigschmid, R. Robertazzi, D. Gogl, F. Pesavento, S. Lammers, K. Lewis, C. Arndt, Y. Lu, H. Viehmann, R. Scheuerlein, L.-K. Wang, P. Trouilloud, S. Parkin, W. Gallagher, and G. Muller, "Memories of tomorrow", *IEEE Circuits and Devices*, vol. 18, no. 5, pp. 17–27, Sept. 2002.
- [6] A. Bette, J. DeBrosse, D. Gogl, H. Hoenigschmid, R. Robertazzi, C. Arndt, D. Braun, D. Casarotto, R. Havreluk, S. Lammers, W. Obermaier, W. Reohr, H. Viehmann, W. J. Gallagher, and G. Muller, "A high-speed 128Kbit MRAM core for future universal memory applications", in *Symp. VLSI Circuits, Digest of Technical Papers*, June 2003, pp. 217–220.
- [7] M. Durlam, P. J. Naji, A. Omair, M. DeHerrera, J. Calder, J. M. Slaughter, B. N. Engel, N. D. Rizzo, G. Grynkewich, B. Butcher, C. Tracy, K. Smith, K. W. Kyler, J. J. Ren, J. A. Molla, W. A. Feil, R. G. Williams, and S. Tehrani, "A 1-Mbit MRAM based on 1T1MTJ bit cell integrated with copper interconnects", *IEEE Journal of Solid-State Circuits*, vol. 38, no. 5, pp. 769–773, May 2003.
- [8] T. Honda, N. Sakimura, T. Sugibayashi, S. Miura, H. Numata, H. Hada, and S. Tahara, "MRAM-writing circuitry to compensate for thermal-variation of magnetization-reversal current", in *Symp. VLSI Circuits, Digest of Technical Papers*, June 2002, pp. 156–157.
- [9] C.-C. Hung, M.-J. Kao, W.-C. Lin, S. Chao, D. Tang, and M.-J. Tsai, "Low writing current magnetoresistive random access memory (MRAM) with side metal pillar write word line (PWWL)", in *Int. Symp. Advanced Magnetic Technologies*, Taipei, Nov. 2003.
- [10] H. J. Kim, W. C. Jeong, K. H. Koh, G. J. Jeong, J. H. Park, S. Y. Lee, J. H. Oh, I. H. Song, H. S. Jeong, and K. Kim, "A process integration of high-performance 64-Kb MRAM", *IEEE Trans. Magnetics*, vol. 39, no. 5, pp. 2851–2853, Sept. 2003.
- [11] M. G. Mohammad, K. K. Saluja, and A. Yap, "Testing flash memories", in *Proc. 13th Int. Conf. VLSI Design*, Jan. 2000, pp. 406–411.
- [12] M. G. Mohammad and K. K. Saluja, "Flash memory disturbances: modeling and test", in *Proc. IEEE VLSI Test Symp. (VTS)*, Marina Del Rey, California, Apr. 2001, pp. 218–224.
- [13] J.-C. Yeh, C.-F. Wu, K.-L. Cheng, Y.-F. Chou, C.-T. Huang, and C.-W. Wu, "Flash memory built-in self-test using march-like algorithms", in *Proc. IEEE Int. Workshop on Electronic Design, Test, and Applications (DELTA)*, Christchurch, Jan. 2002, pp. 137–141.
- [14] K.-L. Cheng, J.-C. Yeh, C.-W. Wang, C.-T. Huang, and C.-W. Wu, "RAMSES-FT: A fault simulator for flash memory testing and diagnostics", in *Proc. IEEE VLSI Test Symp. (VTS)*, Monterey, California, Apr. 2002, pp. 281–286.
- [15] S.-K. Chiu, J.-C. Yeh, C.-T. Huang, and C.-W. Wu, "Diagonal test and diagnostic schemes for flash memories", in *Proc. Int. Test Conf. (ITC)*, Baltimore, Oct. 2002, pp. 37–46.
- [16] C.-W. Wang, K.-L. Cheng, J.-N. Lee, Y.-F. Chou, C.-T. Huang, C.-W. Wu, F. Huang, and H.-T. Yang, "Fault pattern oriented defect diagnosis for memories", in *Proc. Int. Test Conf. (ITC)*, Charlotte, Sept. 2003, pp. 29–38.
- [17] R.-F. Huang, Y.-F. Chou, and C.-W. Wu, "Defect oriented fault analysis for SRAM", in *Proc. 12th IEEE Asian Test Symp. (ATS)*, Xian, Nov. 2003, pp. 256–261.
- [18] R.-F. Huang, Y.-T. Lai, Y.-F. Chou, and C.-W. Wu, "SRAM delay fault modeling and test algorithm development", in *Proc. Asia and South Pacific Design Automation Conf. (ASP-DAC)*, Yokohama, Jan. 2004, pp. 104–109.
- [19] C.-F. Wu, C.-T. Huang, K.-L. Cheng, and C.-W. Wu, "Fault simulation and test algorithm generation for random access memories", *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 4, pp. 480–490, Apr. 2002.
- [20] T. J. Bergfeld, D. Niggemeyer, and E. M. Rudnick, "Diagnostic testing of embedded memories using BIST", in *Proc. Design, Automation and Test in Europe (DATE)*, Paris, Mar. 2000, pp. 305–309.
- [21] C.-F. Wu, C.-T. Huang, C.-W. Wang, K.-L. Cheng, and C.-W. Wu, "Error catch and analysis for semiconductor memories using March tests", in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, San Jose, Nov. 2000, pp. 468–471.
- [22] P. Nagaraj, S. Upadhyaya, K. Zarrineh, and D. Adams, "Defect analysis and a new fault model for multi-port SRAMs", in *Proc. IEEE Int. Symp. Defect and Fault Tolerance in VLSI Systems (DFT)*, San Francisco, Oct. 2001, pp. 366–374.
- [23] A. J. van de Goor, *Testing Semiconductor Memories: Theory and Practice*, ComTex Publishing, Gouda, The Netherlands, 1998.