CMOS IC diagnostics using the luminescence of OFF-state leakage currents

Stas Polonsky,* Keith A. Jenkins,* Alan Weger,* Shinho Cho†
*IBM T.J. Watson Research Center
Yorktown Heights, NY 10598
Email: polonsky@us.ibm.com
† Silla University, Korea
Email: scho@us.ibm.com

***Abstract*— The light emission from ever increasing leakage currents in advanced CMOS technologies can now be reliably measured using existing photon detectors. The measurements of this emission provide valuable information about the operation of ICs. In this paper we suggest and experimentally demonstrate the following optical techniques: (1) transient logic state detection, (2) transient device temperature measurement, and (3) signal integrity analysis, including crosstalk and power supply noise measurements.**

I. Introduction

The progress of microelectronics complicates IC diagnostics, making many existing methods obsolete. For example, electrical IC characterization using mechanical probes is difficult and will become more difficult due to shrinking feature sizes, multiple metal layers, and increasing device complexity.

Mechanical probing faces the following major problems. First, the access to deep submicron wires requires complex and expensive techniques like Focused Ion Beam (FIB) for probe point creation. More important, the increasing number of metal layers often makes impossible the access to wires deep in the metal stack. Second, the load capacitance and/or resistance of mechanical probes limits the bandwidth of timing measurements. Third, the proliferation of flip-chip IC packaging makes the access to the front side of an IC impossible, and, consequently, renders this type of probing obsolete.

Another example of electrical IC characterization is e-beam probing. This method provides better spatial and timing resolution while being significantly more expensive. It suffers basically from the same problems as the previous technique: the increasing number of metal layers and the front side inaccessibility.

Photon emission microscopy (PEM) is an alternative method of IC diagnostics. This method uses visible and near infrared photon emission from transistors, pn-junctions and similar structures to make conclusions about the operation of an IC. PEM uses time integrating detectors (such as CCD cameras, Focal Plane Arrays, etc.) to obtain the data. The PEM can be performed both from the front-side and back-side of an IC.

The back-side PEM enjoys increasing interest due to the fact that it circumvents the two major problems of other techniques: multiple metal layers and flip-chip packaging.

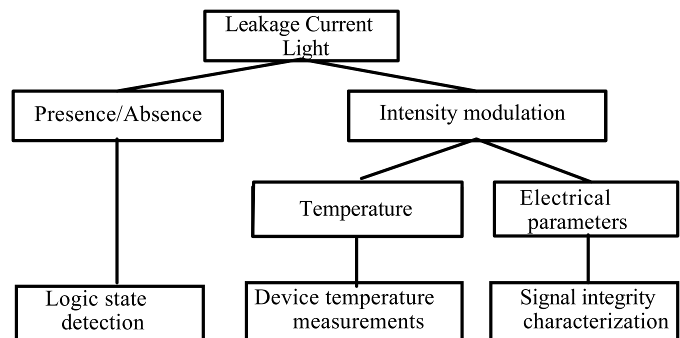

Fig. 1. Classification of OFF-state luminescence

Picosecond Imaging Circuit Analysis (PICA) is a recently introduced time-resolved variant of PEM [1], [2]. It is based on detection of single photons emitted by MOSFETs while in saturation. Each time a CMOS circuit switches logic state, the FETs are briefly in saturation and a weak picosecond light pulse is emitted. The technique proved to be successful enough that commercially available tools were developed to perform PICA [3].

Until recently, the only source of light emission from MOSFETs was hot electron radiation from saturated devices. All existing PEM techniques for MOSFETs are based on this type of light emission. As the size of MOSFETs decreases, two types of parasitic leakage currents become increasingly important - gate tunneling current (this type of current is also present in MOS capacitors) and OFF-state drain to source current. Each type of leakage current results in photon emission or, simply, leakage light. At present, the luminescence of gate tunneling current (L_G) is negligible compared with that of OFF-state leakage (L_{OFF}). In general, L_{OFF} increases with the increase of leakage current as well as the increase of the voltage difference applied to the device; it also increases with the device temperature.

The analysis of L_{OFF} may provide valuable insights into optical IC diagnostics, as shown in the following sections.

II. Applications of OFF-state luminescence

Figure 1 is an explanatory diagram classifying the applications of leakage current light analysis. There are two major

 0-7803-8580-2/04 $20.00 Copyright 2004 IEEE

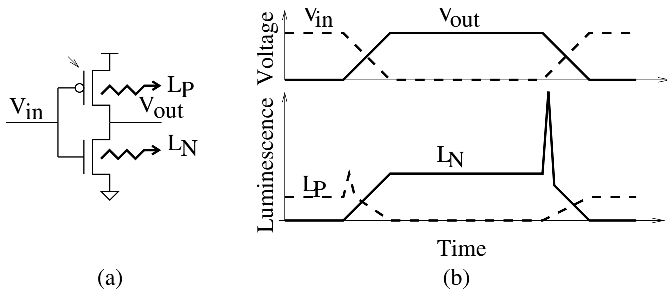

Fig. 2. Logic states detection in CMOS inverter: (a) schematic diagram; (b) timing diagram of logic states and luminescence.

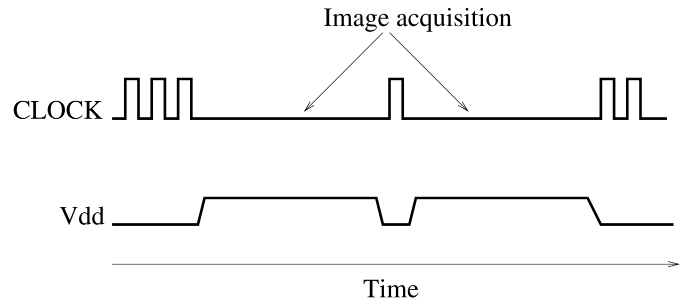

Fig. 3. A concept of static logic state detection.

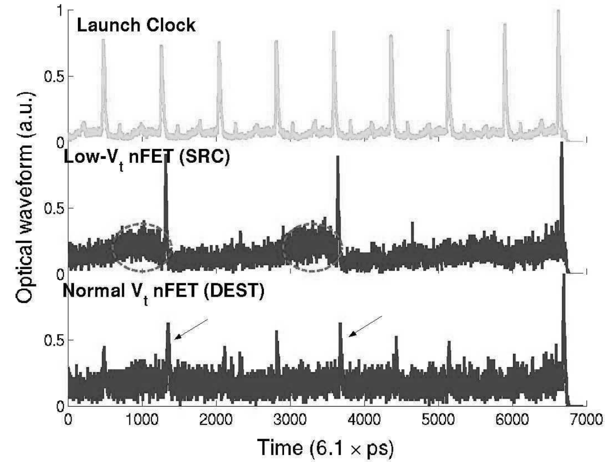

Fig. 4. An example of dynamic logic state detection.

types of possible applications - those that depend on the presence or absence of leakage current light, and those that depend on modulation of intensity of leakage light by various parameters.

The first type allows to detect the logical state of an IC. It can be performed on running IC (transient logic state detection) as well as on stopped IC (static state detection). The immediate use of the former one is to simplify the interpretation of "traditional" PICA data - the knowledge of circuit logic states makes the identification of transition peaks straightforward. The latter technique can be used to debug circuits with limited electric test capabilities such as non-scanable designs or memory structures.

The second type allows to measure various parameters of individual MOSFETs (inside operating IC!!!) such as device temperature T_d , drain-to-source voltage (V_{ds}), gate-to-source voltage (V_{gs}), etc.

These data provide unique possibility to address such important issues as thermal mapping of microprocessors, device self-heating [4]–[6], cross-talk and power noise measurements [7]–[10].

III. L_{OFF} PRESENCE/ABSENCE

The presence or absence of L_{OFF} from a particular MOSFET allows to detect its logical state (ON, OFF). In turn, the knowledge of logical states of MOSFETs allow to reconstruct the logical state of an entire IC. Thus the logical state of an IC can be determined by measurements of leakage light from MOSFETs

Figure 2 illustrates this method for CMOS inverter. The leakage light L_N from nFET is emitted only when the inverter is in logic state 1 (i.e. input $V_{in} = 0$, output $V_{out} = 1$). The leakage light from pFET is emitted only when the inverter is in logic state 0 ($V_{in} = 1$, $V_{out} = 0$). The leakage light luminescence from both types of devices is persistent (i.e. the devices emit the light as long as the inverter is in a definite state), unlike the light emitted by MOSFETs in saturation, which is traditionally used by PEM. This type of light emission occurs when the inverter changes its logical state. The peaks on Fig. 2a correspond to the switching of pFET (label P) and nFET (label N) correspondingly.

Similar considerations show that the state of inverter can be determined using the gate tunneling luminescence. Moreover, both types of leakage light can be used to determine the logic state of an arbitrary CMOS gate.

The measurements of logic states can be performed on both running and stopped ICs.

A. Static logic state detection

The logic state detection of a stopped IC (static state detection) can be performed by using a time-integrating detector such CCD or MCT focal plane array camera. The concept of static logic state detection is shown on Fig. 3. The clock is applied at nominal speed to an IC until a clock cycle of interest is reached. Then the clock is stopped to keep the logical state an IC and the image of leakage currents is taken. During this time the supply voltage Vdd can optionally be raised to increase the intensity of L_{OFF} . After the completion of image acquisition the clock is applied again until the next clock cycle of interest is reached, another image is taken, etc. This technique can even be applied to dynamic circuit families provided that the image acquisition time is smaller then corresponding retention time.

B. Dynamic logic state detection

The measurement of an IC running at speed (dynamic state detection) requires time-resolved imagers (e.g. MCP - multi-channel plate photomultiplier) or single-pixels detectors (e.g.

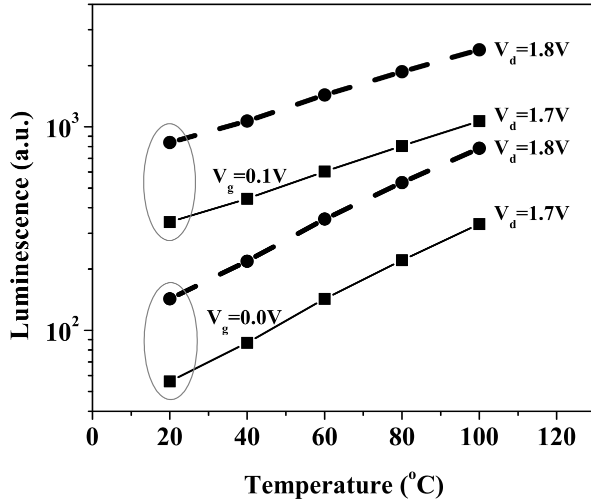

Fig. 5. L_{OFF} dependence on T_d (110 $nm \times 10\ \mu m$ SOI nFET [13]).

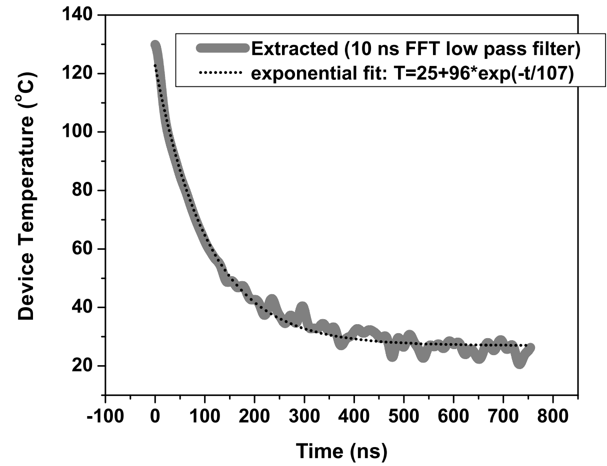

Fig. 6. Extracted device temperature of the SOI nFET. The device is the same as in Fig. 5

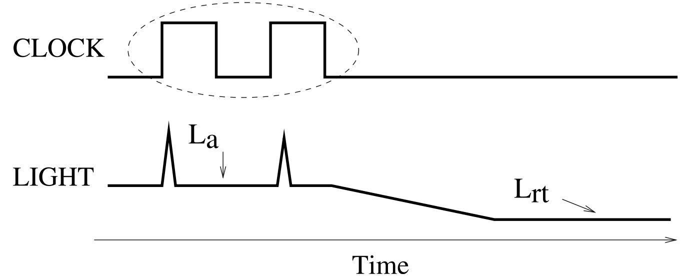

Fig. 7. A concept of temperature measurement in CMOS circuits.

superconducting single-photon detector [3], avalanche photo diode [11], etc.) An example of using this technique is shown on Fig. 4 [12]. The measurements were performed on 0.18 μm SOI microprocessor. The peaks of $LAUNCH\ CLOCK$ mark the falling edge of the capture clock and the the rising edge of the launch clock. Dashed circles mark the light emission due to OFF-state leakage currents. The arrows mark identified peaks of interest for use in "traditional" PICA analysis.

IV. L_{OFF} INTENSITY MODULATION

The second type of leakage light applications is based on the fact that a number of important parameters can modulate its intensity. Once the dependence of the leakage light on a particular parameter is known, it can be inverted to extract the value of the parameter from the leakage light measurements.

A. Device temperature measurement

Off-state current I_{OFF} and, consequently, L_{OFF} , is a very sensitive function of the device channel temperature T_d . In contrast, the on-current is relatively insensitive to temperature and not suitable for this type of measurements. A typical dependence of L_{OFF} on T_d is shown in Fig. 5 for different V_g and V_d.

Similar to I_{OFF} , the curves follow the exponential dependence $log(L_{OFF}) = A + B \times T$, where offset A increases with the increase of V_d, and the slope B decreases with the increase of V_g. The dependence $A(V_d)$ can be explained by drain induced barrier lowering effect. The dependence $B(V_g)$ originates from the fact that the relative contribution of temperature-dependent diffusion component of I_{OFF} (as compared with almost temperature-independent drift component) decreases as $V_g \rightarrow V_t$ [14]. Parameter A can vary between identical devices (e.g. a wire can partially block the device) while parameter B was found constant within experimental accuracy.

Fig. 6 is an example of using this technique to measure the dynamics of nFET cooling after being in ON-state for a prolonged period of time (larger then the corresponding self-heating time constant) [15].

The technique can also optically measure temperature of individual devices in real IC and, consequently, it can be used for time-resolved thermal mapping of microprocessors.

Fig. 7 illustrates one possible implementation this method. Initially, an IC operates at given clock speed (shown as dashed ellipse). The temperatures of individual devices are increased due to their switching activity. The light emitted by an individual transistor consists of peaks that correspond to its switching activity (saturation luminescence) and "baseline" leakage light L_a. After the clock is stopped, the device temperatures decrease and equal ambient temperature which results in the decreased value of leakage light L_{rt} . The temperature of operating device can be extracted using calibration curves similar to that shown in Fig 5.

B. Signal integrity measurements

Various electrical parameters modulate the OFF-state leakage light. A typical dependence $L_{OFF}(V_{gs})$ is shown in Fig. 8 for an nFET from 130 nm technology generation. For

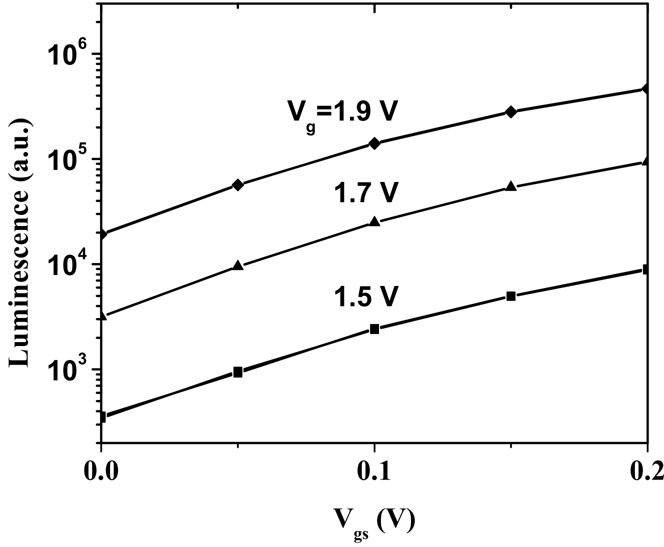

Fig. 8. Calibration curve L_{OFF} (same device as in Fig. 5)

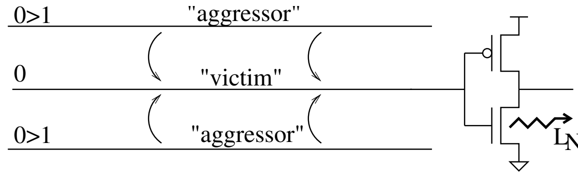

Fig. 9. A concept of optical crosstalk measurement

$V_{gs} \leq V_t$ this dependence is exponential, similar to that of I_{OFF} .

Within the experimental accuracy, the subthreshold slope,

$$S_G = \left(\frac{\partial(log_{10}L_{OFF})}{\partial V_g}\right)^{-1}, \quad (1)$$

is in $100\pm10\ mV/decade$ range, close to the corresponding value of subthreshold leakage current slope.

Similarly, the dependence of L_{OFF} on drain voltage V_{ds} is also exponential. The slope of this dependence,

$$S_D = \left(\frac{\partial(log_{10}L_0)}{\partial V_d}\right)^{-1}, \quad (2)$$

is significantly higer then that of $I_{OFF}(V_d)$. As an example, for a 112 nm channel length nFET, $S_D = 0.230\ V/decade$, considerably steeper than a similar slope of $I_{OFF}(V_d)$ dependence (0.5 $V/decade$).

The most important application of $L_{OFF}(V_g)$, $L_{OFF}(V_d)$ dependencies is the possibility of optical time-resolved measurements of V_{gs} and V_{ds} , or, in other words, optical signal integrity analysis (see Fig. 1).

Experimental technique to measure V_{gs} allows crosstalk analysis. It is illustrated on Fig. 9. The "victim" wire is in logical state 0. It is connected to the input of inverter and is coupled to nearby "aggressor" wires through a variety

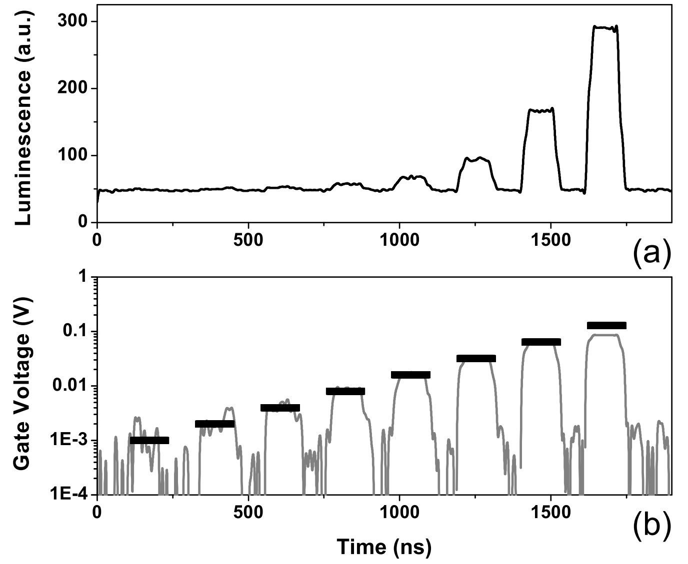

Fig. 10. (a) Time-resolved off-state luminescence from 112 $nm \times 20\ \mu m$ nMOSFET ($V_d = 2\ V$, Measurement time 1000 s); (b) Extracted gate voltage waveform ("crosstalk"). Thick lines correspond to applied pulse height.

of coupling mechanism (e.g. inductive, capacitive, etc.). The leakage light L_N from inverter's nFET is relatively small ($V_{gs} = 0$) The aggressor wires simultaneously transition from logical 0 to 1. The potential of the victim wire increases which leads to the increase of L_N. The use of calibration curves similar to that in Fig. 8 will provide quantitative information about the crosstalk noise in the victim wire.

Figure 10 illustrates the proposed technique and its accuracy. A sequence of voltage pulses of increasing height, generated by an arbitrary waveform generator, is applied to the gate of single nFET kept at constant V_{ds} . Time-resolved voltage V_{gs} is extracted from the measured L_{OFF} using the inverted dependence (1), $V_g = L_0 \times 10^{L_{OFF}/S_G}$. An estimate of L_0 is obtained from measuring the device in quiscent state.

The extracted V_g is compared with actual heights of applied voltage pulses in Fig. 10b. The values are extracted correctly within 3 mV accuracy. For larger voltages, approaching the device's threshold voltage, our simple technique produces underestimated results, and should be replaced by more sophisticated analysis. For our measurements, the timing resolution was limited by the low-frequency experimental setup. For "real-life" on-chip measurements, it will be limited by detector's jitter, which for MCP is about 80 ps. For a new generation of sensitive time-resolved single photon detectors [16], the jitter is as low as 30 ps.

Time-integrating detectors can also be effectively used for crosstalk noise analysis. Two input patterns are chosen: the first pattern corresponds to the "minimum" crosstalk (i.e. no transitions in victim and aggressor lines); the second one corresponds to the "maximum" crosstalk (i.e. simultaneous transitions in aggressor lines, no transitions in the victim line). Photon emission images are taken for both patterns and the

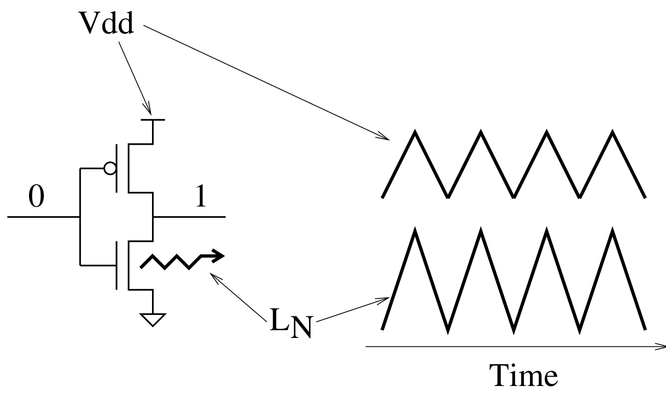

Fig. 11. A concept of power distribution noise measurement

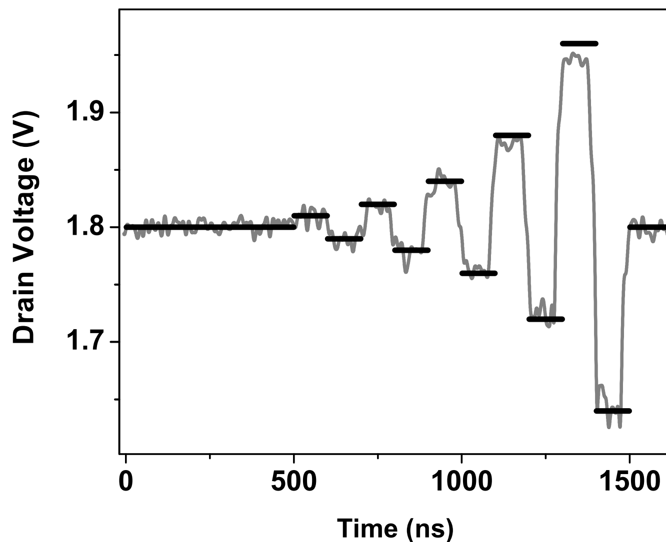

Fig. 12. Extracted "power noise" voltage waveform (same device as in Fig. 10)

difference image is computed. The intensity of light emission from the inverter on the difference image is used to detect if there is any significant crosstalk.

Similarly, the dependence of leakage light in MOSFETs and MOS capacitors on power supply voltage V_{dd} can be used to characterize the power distribution noise caused by circuit switching activity. Fig. 11 explains the method using OFF-state leakage light from an inverter's nFET. When the inverter is in logic state 1, the drain-to-source voltage across its nFET is close to power supply voltage V_{dd} so that the leakage light L_N from this nFET is modulated by V_{dd} . The transient variations of V_{dd} cause corresponding variations of the L_N, which, in turn, can be measured by a time-resolved photon detector.

Fig. 12 illustrates the above approach. This time, the output of the arbitrary waveform generator varies the nFET's drain-to-source voltage. V_{ds} is extracted from the time-resolved L_{OFF} using dependence (2). Drain voltage variations as small as $10 - 20\ mV$ can be reliably measured using this technique.

It is worth to mention that the power noise analysis can also use the leakage light emission from pFETs, gate tunneling light from FETs of any types as well that from MOS capacitors.

V. Conclusion

The amount of light emitted by OFF-state leakage currents in advanced CMOS technologies becomes comparable to that coming from switching MOSFETs. The analysis of this light provides valuable insights into the operation of CMOS circuits. In this extended abstract we suggest and experimentally demonstrate the use of leakage light for detection of logic states of CMOS circuits, time-resolved measurement of the MOSFETs temperature as well as various electrical parameters (V_{gs} , V_{ds}). The later can be used for signal integrity analysis (crosstalk, power noise, etc.)

The full conference paper will have more complete presentation of the concepts and numerous experimental results.

Acknowledgment

The authors would like to thank Modest Oprysko, Marc Taubenblatt, David Heidel, Mark Ketchen, Kai Xiu, Peilin Song, and Franco Stellari for the helpful discussions and support.

References

[1] J. C. Tsang and J. A. Kash, "Picosecond hot electron light emission from submicron complimentary metal-oxid-semiconductor circuit," *Appl. Phys. Lett.*, vol. 70, pp. 889–891, 1997.

[2] J. A. Kash and J. C. Tsang, "Dynamic internal testing of CMOS circuits using hot luminescence," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 330–332, 1997.

[3] N. Goldblatt, M. Leibowitz, and W. Lo, "Unique and practical IC timing analysis tool utilizing intrinsic photon emission," *Microelectronics Reliability*, vol. 41, no. 9-10, pp. 1507–1512, 2001.

[4] L. J. McDaid, S. Hall, P. Mellor, W. Eccleston, and J. Alderman, "Physical origin of the negative differential resistance in SOI transistors," *Electron. Lett.*, vol. 25, pp. 827–828, 1989.

[5] D. A. Dallmann and K. Shenai, "Scaling constraints imposed by self-heating in submicron SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 3, pp. 489–496, March 1995.

[6] B. Tenbroek, M. Lee, W. Redman-White, R. Bunyan, and M. Uren, "Impact of self-heating and thermal coupling on analog circuits in SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1037–1046, July 1998.

[7] T. Sato, D. Sylvester, Y. Cao, and C. Hu, "Accurate in situ measurement of peak noise and delay change induced by interconnect coupling," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1587–1591, October 2001.

[8] C. Werner, R. Gottsche, A. Worner, and U. Ramacher, "Crosstalk noise in future digital CMOS circuits," in *Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings , 13-16 March 2001*, 2001, pp. 331–335.

[9] R. Ho, B. Amrutur, K. Mai, B. Wilburn, T. Mori, and M. Horowitz, "Applications of on-chip samplers for test and measurement of integrated circuits," in *Symposium on VLSI Circuits*, June 1998, pp. 138–139.

[10] K. L. Shepard and Y. Zheng, "On-chip oscilloscopes for noninvasive time-domain measurement of waveforms," in *Proc. of International Conference on Computer Design*, 2001, pp. 221–226.

[11] D. Bodoh, E. Black, K. Dickson, R. Wang, T. Cheng, N. Pakdaman, J. Vickers, D. Cotton, and B. Lee, "Defect localization using time-resolved photon emission on SOI devices that fail scan tests," in *Proc. ISTFA'2002*, November 2002, pp. 655–661.

[12] S. Polonsky, A. Weger, and M. McManus, "Picosecond imaging circuit analysis of leakage currents in CMOS circuits," in *Proc. ISTFA'2002*, November 2002, pp. 387–390.

[13] P. Smeys *et al.*, "A high performance 0.13 μm SOI CMOS technology with Cu interconnects and low-k BEOL dielectric," in *Proc. Symposium on VLSI Technology*, 2000, pp. 184–185.

[14] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 1998.

[15] S. Polonsky and K. Jenkins, "Time-resolved measurements of self-heating in SOI and Strained-Silicon MOSFETs using photon emission microscopy," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 208–210, April 2004.

[16] R. Sobolewski, A. Verevkin, G. Gol'tsman, A. Lipatov, and K. Wilsher, "Ultrafast superconducting single-photon optical detectors and their applications," *IEEE Trans. Appl. Superconduct.*, vol. 13, no. 2, pp. 1151–1157, june 2003.