

# IMPACT OF NEGATIVE BIAS TEMPERATURE INSTABILITY ON PRODUCT PARAMETRIC DRIFT

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## Abstract

*A systematic test methodology is presented that comprehends the impact of Negative Bias Temperature Instability on product parametric drift. A test guard-banding technique to estimate parameter drift under BI and customer use conditions is given.*

## 1 Introduction

One of the primary challenges that is encountered during IC testing of deep sub-micron technologies is the increasing importance of parametric failures [1]. These failures result from the variation of critical parameters such that the combined variation results in a product failing data-sheet specifications. As discussed in [1], parametric failures can result from extrinsic defects, normal process variation, and intrinsic degradation mechanisms.

The focus of our paper is on the accelerated stress and test methodology used to observe the intrinsic degradation mechanisms leading to parametric failure. There are several intrinsic reliability mechanisms in the transistor and metal processing loops. Historically the transistor reliability wear-out mechanisms that have received much attention during product design and reliability characterization are Channel Hot Carrier (CHC) degradation and gate oxide Time Dependent Dielectric Breakdown (TDDB). Another transistor reliability mechanism that has recently become significant and has an observable impact on a product's design, test methodology, and reliability is Negative Bias Temperature Instability (NBTI).

This paper is divided into several sections. We will first describe the CHC, TDDB, and NBTI degradation mechanisms and their relevance in digital CMOS circuits. Next we will discuss the transistor degradation impact due to NBTI on individual transistors and then on simple circuits that are the building blocks of an IC. This will then be followed by a discussion of the impact of NBTI on a high performance, deep sub-micron IC.

The magnitude of the observed impact consequently motivates the need for a systematic test methodology to quantify NBTI induced parameter drift. Details of this systematic technique and supporting data will be presented to establish an unequivocal correlation between NBTI and

product parametric drift. A test guard-banding methodology to account for this drift will then be presented.

## 2 Transistor Reliability Mechanisms

As just mentioned, the three main transistor reliability mechanisms relevant to deep sub-micron technologies are CHC, gate oxide TDDB, and NBTI. The transistor parametric manifestation of CHC is a continuous degradation in transistor drive current,  $I_{DSAT}$ . CHC is known to exhibit strong gate length and frequency dependencies. It occurs only during transistor switching activity [2]. The transistor parametric manifestation of gate oxide TDDB is an increase in leakage through the gate or a decrease in  $I_{DSAT}$ . The breakdown mechanism cause is random in nature and increases in probability with increased oxide area.

NBTI has recently grown in importance as evidenced by an escalation in activity on this phenomenon [3,4]. The transistor parametric manifestation of NBTI is a continuous decrease in  $I_{DSAT}$  and a continuous increase in the threshold voltage,  $V_{TH}$ . This reliability mechanism impacts only the pMOS transistor through the generation of interface states at the oxide silicon interface. It does not have strong gate length dependence as contrasted with CHC. This degradation occurs whenever the pMOS transistor is biased in an on-state.

The importance of NBTI during digital CMOS circuit operation can be easily understood by considering the voltage waveforms in a simple CMOS inverter as illustrated in Figure 1. This figure illustrates that NBTI occurs during digital CMOS circuit operation when the pMOS transistor is fully turned on after charging up the capacitive load.

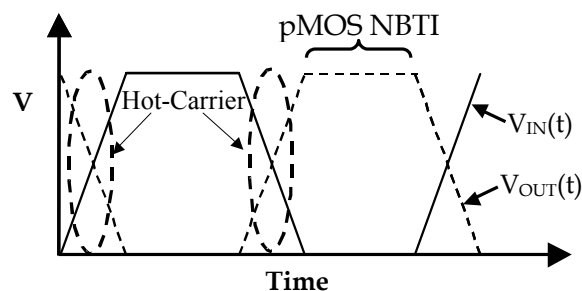
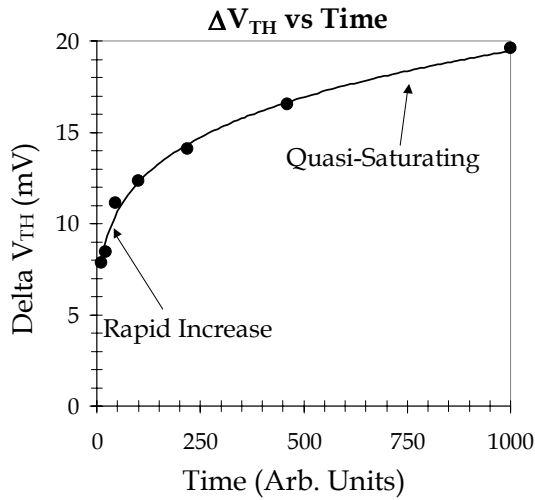
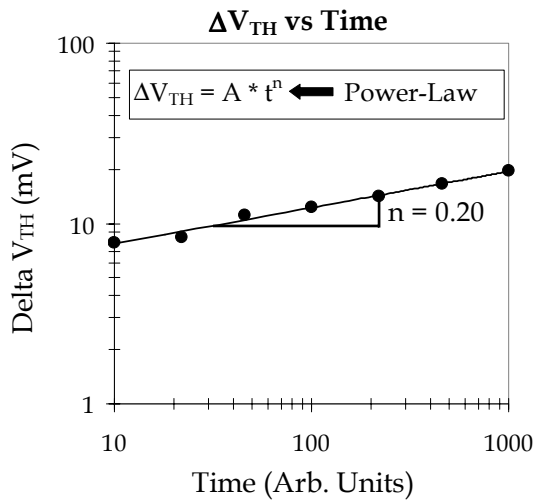


Figure 1: CMOS inverter input/output voltage waveforms.

Since the degradation occurs when the pMOS transistor is effectively biased with a negative gate voltage, the term “Negative Bias Temperature Instability” arises. Note that CHC degradation only occurs during switching transitions while NBTI occurs for a substantially longer period of time when the circuit is not switching and is essentially static. Therefore, one can expect that the duty cycle for NBTI degradation is substantially larger than for CHC and thus potentially more significant during product operation.



(a)



(b)

**Figure 2:** (a) 130 nm process experimental data illustrating pMOS NBTI induced  $V_{TH}$  increase with time on a linear-linear plot, (b) on a log-log scale plot.

We present in Figure 2 experimental data from stressing discrete transistors that illustrates the increase in  $V_{TH}$  versus NBTI stress time. The transistors were processed using a 130nm CMOS process. The NBTI induced  $V_{TH}$  drift shows two behavioral regimes when plotted on linear scale in Figure 2(a). At early stress times, there is a rapid change in the  $V_{TH}$  drift and then for longer time duration, the drift rate

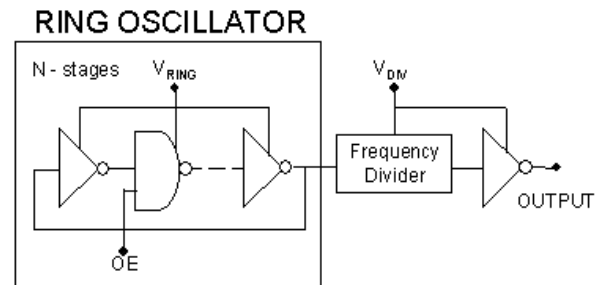
of change decreases in a quasi-saturating manner. This type of functional time dependence typically implies a power-law time dependence, as illustrated in Figure 2(b), where the data of Figure 2(a) is plotted on a log-log scale to reveal a linear behavior.

The slope of this line is called the power-law slope,  $n$ . It is technology dependent and typically ranges in value from 0.15 to 0.30 [3]. The low value of  $n$  ( $n < 1$ ) gives rise to the ‘quasi-saturating’ behavior. It is important to note that NBTI degradation has been shown to follow a power-law time dependence due to the mathematics of the electrochemical reaction/diffusion reaction underlying NBTI degradation [5]. Therefore, the functional form is not merely a curve-fitting exercise but rather a necessary consequence of the degradation physics.

### 3 Circuit Building Blocks

While there have been extensive investigations of the effect of NBTI at the transistor level, there has been relatively little work on the circuit level impact. Recent work has explored the NBTI impact on analog circuits such as operational amplifiers [6]. For digital circuits, an indirect correlation of NBTI drift to circuit performance drift has been reported [8]. We have recently studied the impact of NBTI on prototypical digital circuits and shown the direct impact of NBTI on digital circuit reliability [7]. These findings are summarized in this section.

A ring oscillator (RO) was chosen as the prototypical digital circuit since it is widely used as a performance metric during technology development. This inverter RO, whose circuit schematic is shown in Figure 3, has an oscillation enable pin, OE, that controls whether the RO is oscillating ( $OE=V_{DD}$ ) or not ( $OE=0V$ , static state).

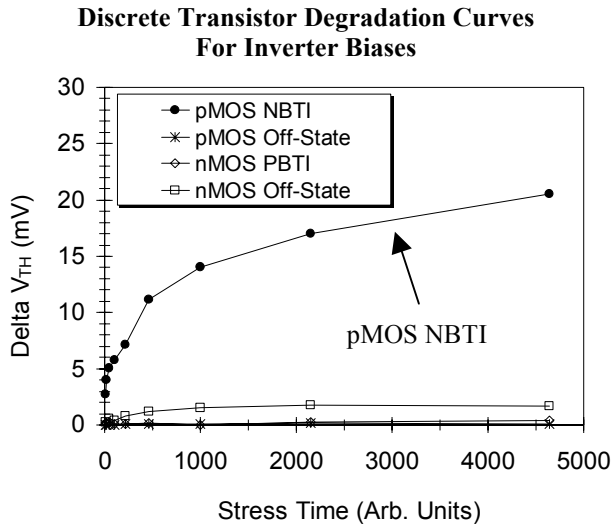


**Figure 3:** Simplified inverter ring oscillator schematic.

When the RO is held in a static state, each nMOS and pMOS transistor is in either the on or off-state. It is instructive at this point to characterize what type of degradation may occur when stressing either the nMOS or pMOS transistor in the on or off-state. The data shown in Figure 4 clearly indicates that pMOS NBTI is the dominant degradation mode for a statically stressed CMOS inverter.

Based on the results in Figure 4, for a statically stressed inverter, the dominant degradation mode is expected to be

due to pMOS NBTI. This implies that the majority of the degradation observed in a statically stressed inverter RO is also expected to be attributed to NBTI degradation. This is a key finding that we exploit extensively later in the paper to link NBTI degradation to product parametric drift.

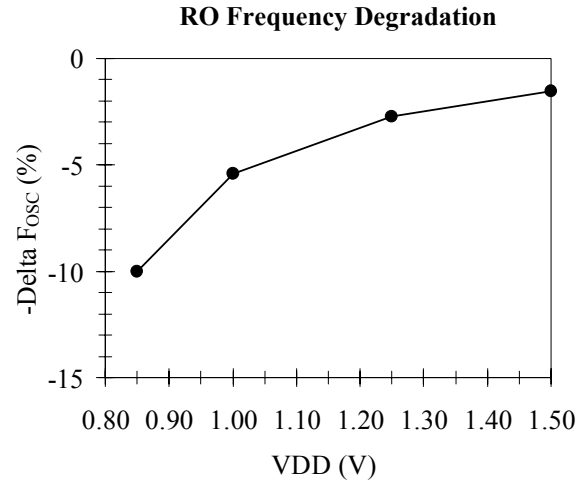


Inverter Biasing Configuration	V <sub>IN</sub>	V <sub>OUT</sub>	NMOS Stress Mode	PMOS Stress Mode
1	V <sub>DD</sub>	0V	On-State	Off-State
2	0V	V <sub>DD</sub>	Off-State	On-State

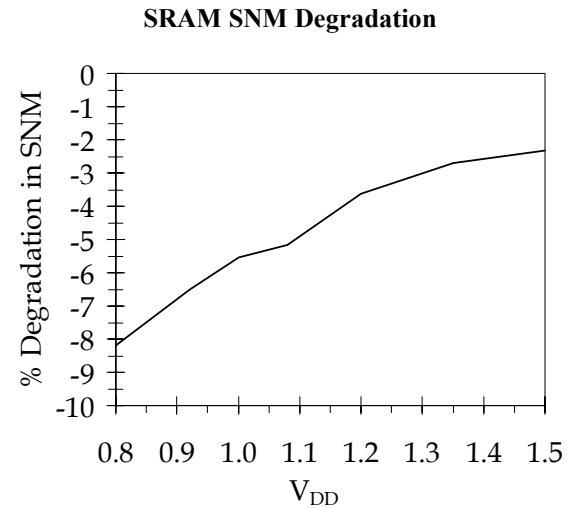
**Figure 4:** V<sub>TH</sub> drift of nMOS and pMOS transistors stressed in both the on and off-state conditions at an elevated voltage and temperature.

Given the circuit shown in Figure 3, we statically stressed an inverter RO under the same conditions as that of Figure 4 and the resulting reduction in the RO oscillation frequency, F<sub>OSC</sub>, is shown in Figure 5. It can be seen that after a given stress period the magnitude of the frequency reduction increases as V<sub>DD</sub> decreases. This is due to a reduction in the voltage headroom of the transistor and indicates that the impact of NBTI is exacerbated as V<sub>DD</sub> is decreased [4].

Now we would like to discuss the impact of another important circuit building block, the 6-T SRAM cell. One key SRAM metric is the Static Noise Margin (SNM). It is crucial to understand the impact of NBTI degradation on the SRAM SNM [9]. The impact of NBTI degradation on SNM was modeled by incorporating NBTI degraded SPICE models in one of the pMOS load transistors of the SRAM 6-T memory cell. The resultant degradation in SNM as a function of V<sub>DD</sub> is shown in Figure 6. This indicates that the SNM degradation increases as V<sub>DD</sub> decreases. For both the RO and SRAM cell, the NBTI induced degradation increases as V<sub>DD</sub> decreases.



**Figure 5:** %-Frequency reduction (Post Stress – Pre Stress) of statically stressed ring oscillators versus V<sub>DD</sub>.



**Figure 6:** The % degradation in SNM, due to NBTI degradation, increases as V<sub>DD</sub> decreases.

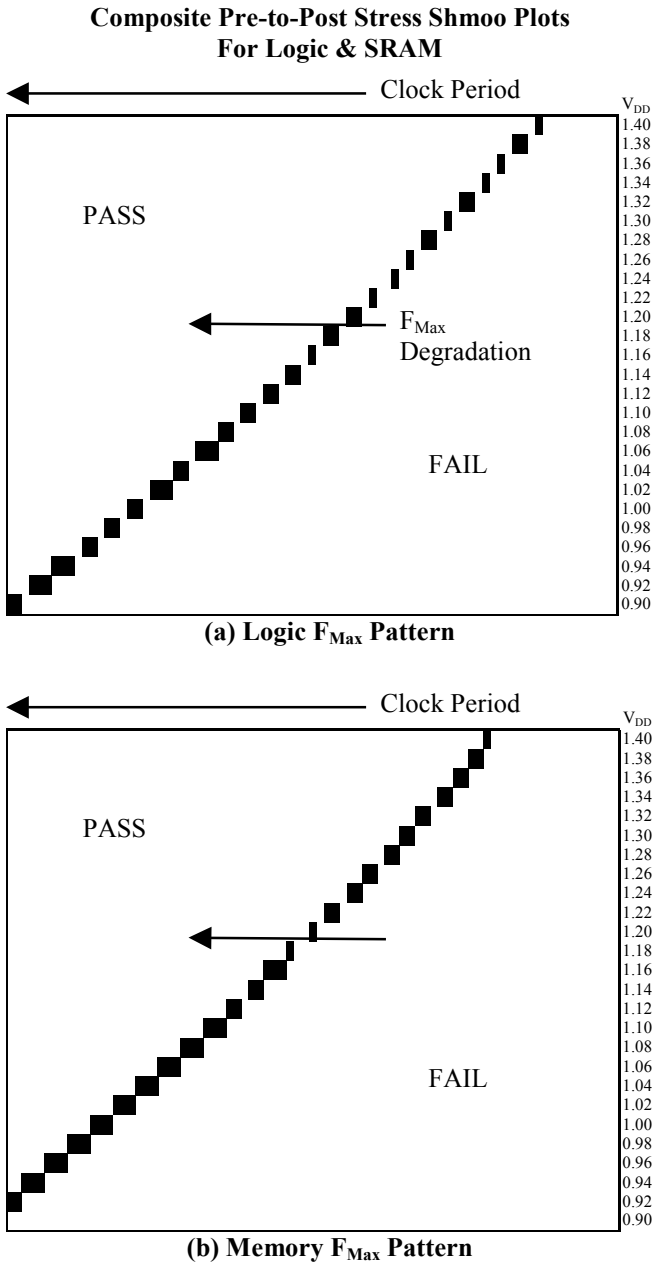
#### 4 Product Impact

To date, there has been only one report on the NBTI impact at the product level [10]. The data reported in this paper addresses the NBTI induced product parametric drift of a 2.5 million transistor count, several hundred MHz IC fabricated in a 130nm process. All of the experimental data reported in this section is based on this product, including Figures 7 and 10-14.

To understand the sensitivity and stability of this product accelerated stress, we measured the F<sub>Max</sub> versus V<sub>DD</sub> Shmoo plot, shown in Figure 7, before and after an accelerated voltage and temperature stress. As can be clearly seen, the Shmoo plots exhibit movement of the failing region to the left indicating the product F<sub>Max</sub> response is degrading. Further, the degradation manifests itself as a

uniform envelope reduction in the  $F_{Max}$  versus  $V_{DD}$  response without the development of any Shmoo holes.

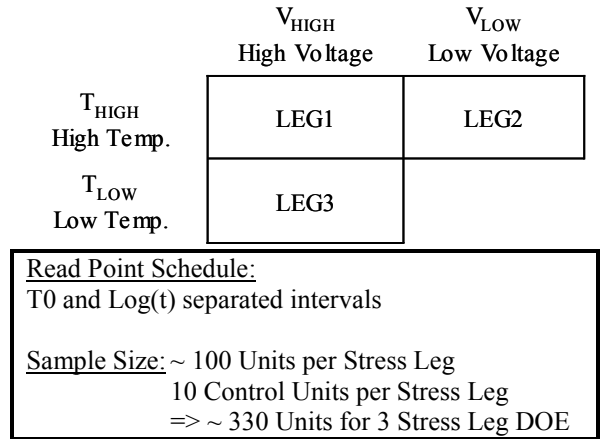
As will be shown later in this section, this  $F_{Max}$  degradation is induced by NBTI. One of the key assumptions underlying this technique is that we can observe, under accelerated stress conditions, product parameter drift due to the transistor level degradation. What is required is a technique that is able to quantify the parametric drift of the standard environmental variables, such as voltage, temperature, and time.



**Figure 7:** Shmoo plot of (a) Logic  $F_{Max}$  pattern and (b) Memory  $F_{Max}$  pattern showing movement (Black squares) towards the left, indicating  $F_{Max}$  degradation after BI stress

#### 4.1 Quantifying Product Parametric Drift

To quantify the product parametric drift, we employ a straightforward 2-Way Design of Experiments (DOE), where the variables are the stress voltage and temperature. The DOE illustrated in Figure 8 is a three Stress Leg experiment that is designed to determine a test pattern specific Voltage Acceleration Factor (VAF) and Temperature Acceleration Factor (TAF).



**Figure 8:** DOE details to quantify product parametric drift.

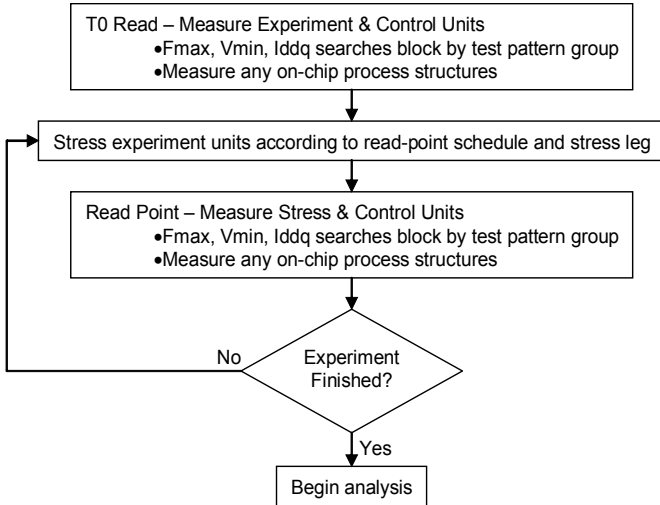
A population of packaged units is stressed at the three stress conditions and all product data parameters are data-logged at a specified read-point schedule. The sample size is approximately 330 units, including 30 control units. The control units are not electrically or thermally stressed and execute the same test program and read-point schedule as the stressed units. The purpose of the control units is to address any ATE induced repeatability and reproducibility issues. The read point schedule used is designed to capture any early drift, typical of NBTI, but also comprehend longer time scales.

The  $V_{HIGH}$  and  $V_{LOW}$  stress values are chosen to be higher than the product BI voltage to accelerate the stress mechanism and observe parameter drift in a reasonable amount of time. The  $T_{HIGH}$  and  $T_{LOW}$  stresses are junction temperature values as determined by  $\Theta_{JA}$  measurements or on-chip thermal monitors. They are chosen with similar considerations as the voltage stresses and are well away from any thermal runaway limits [11].

It should be noted that this experiment leverages the existing BI and test infrastructure that is normally used in product qualification. The BI patterns are run dynamically and generally driven at 5 MHz. The BI patterns executed are repeated ATPG patterns for logic stressing and BIST and/or DMA patterns for memory stressing.

A simplified test flow diagram for executing the experiment is given in Figure 9. The test data collected includes  $F_{MAX}$ ,  $V_{MIN}$ , and  $I_{ddq}$  searches across design blocks and on-chip parametric structures such as ring oscillators.

The ROs are designed to be statically stressed when the product is in the BI oven and receive the same voltage and temperature stress as the product. As discussed in Section 3, the RO will only experience pMOS NBTI degradation. Therefore, any  $F_{OSC}$  drift measured is only due to NBTI.



**Figure 9:** Simplified test flow for executing experiment outlined in Figure 8.

#### 4.2 Product Parametric Drift - Experimental Data

We now present the parametric drift data versus stress time based on the experiment described in the previous section. Shown in Figures 10-12 are plots of the drift behavior versus stress time for  $F_{Max}$ ,  $V_{Min}$ , and  $F_{OSC}$ , respectively. Each data point is the averaged value over all units for each of the three stress legs and control leg. Further, each data point is the delta with respect to the T0 read point with the following definitions:

$$\Delta F_{Max}(\%) = \{F_{Max}(\text{Read-point}) - F_{Max}(T0)\} / F_{Max}(T0) * 100\%$$

$$\Delta F_{OSC}(\%) = \{F_{OSC}(\text{Read-point}) - F_{OSC}(T0)\} / F_{OSC}(T0) * 100\%$$

$$\Delta V_{Min} = V_{Min}(\text{Read-Point}) - V_{Min}(T0)$$

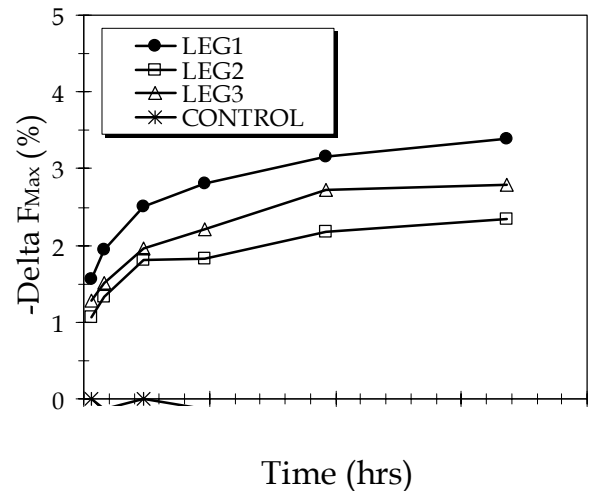
It should be noted that since both  $F_{Max}$  and  $F_{OSC}$  decrease with stress time,  $-\Delta F_{Max}$  and  $-\Delta F_{OSC}$  are plotted to obtain a positive value. This is driven by the mathematical modeling requirements to extract a power law slope.

As is apparent in Figures 10-12, LEG1 ( $V_{HIGH}, T_{HIGH}$ ) exhibits a larger drift magnitude than either LEG2 ( $V_{LOW}, T_{HIGH}$ ) or LEG3 ( $V_{HIGH}, T_{LOW}$ ). This is the anticipated behavior since LEG1 is subjected to the highest voltage and temperature stress. Also, the control units show no drift, as expected, since they are not stressed. The RO drift in Figure 12 can be attributed totally to NBTI, as discussed in Section 3. It is important to note that the drift behavior for all three cases exhibits an “NBTI-like”

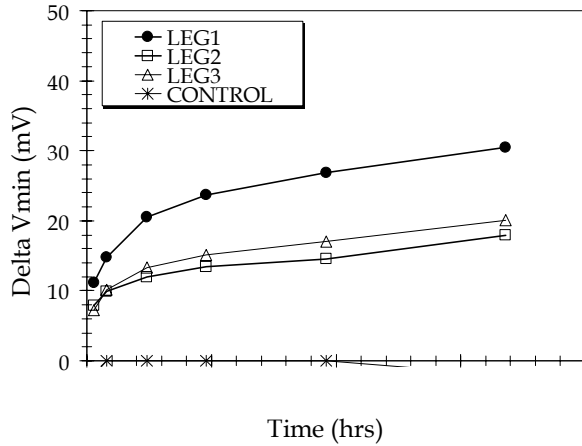
behavior in that there is a rapid drift for early read points and the drift rate quasi-saturates at the longer stress times.

Due to the inherent transistor and interconnect parametric variation present in deep sub-micron processes, products are expected to meet data-sheet specifications at the weak and strong process corners [1]. Typically, during a product ramp-up phase silicon is run at these process corners to characterize the design margin and manufacturability. To understand the product parametric drift sensitivity at these transistor corners, we ran a similar stress experiment as discussed earlier on a set of silicon consisting of Strong, Nominal, Weak, and Very Weak transistors splits. The Very Weak split was below the normal process limits set by the wafer fab. The variation in transistor drive strength was achieved by varying only the gate length while keeping all other transistor design corners the same. The  $\Delta F_{Max}$  and  $\Delta F_{OSC}$  are plotted in Figures 13 and 14, respectively, for the four transistor corners.

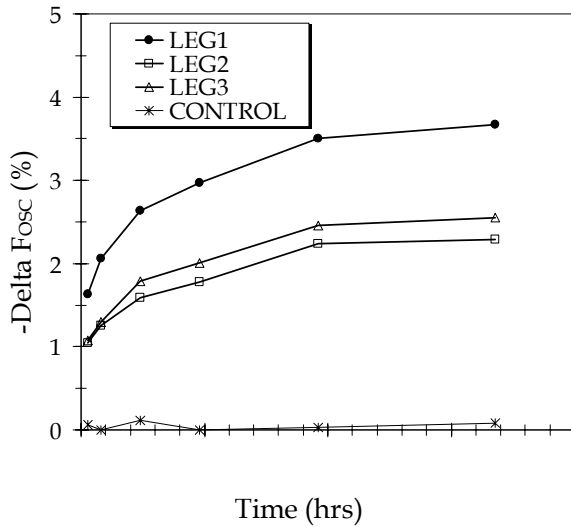
As is apparent in both Figure 13 and 14, no consistent trend is observed for the four splits. This indicates that the degradation phenomena responsible for the drift is not a strong function of the transistor drive strength or gate length. In Section 2 it was noted that the NBTI phenomenon is not gate length sensitive and thus further suggests a link between NBTI and product parameter drift [3].



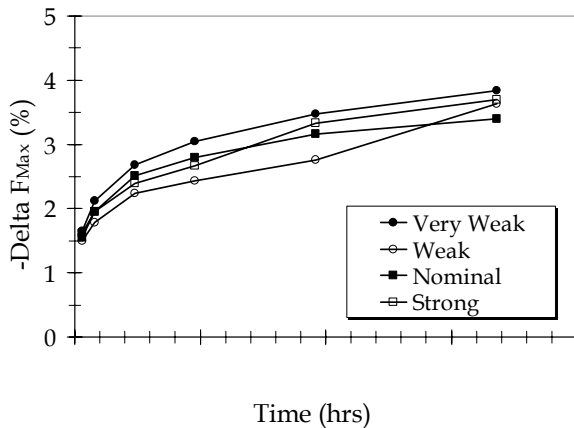
**Figure 10:** Delta  $F_{Max}$  (%) versus Stress Time.



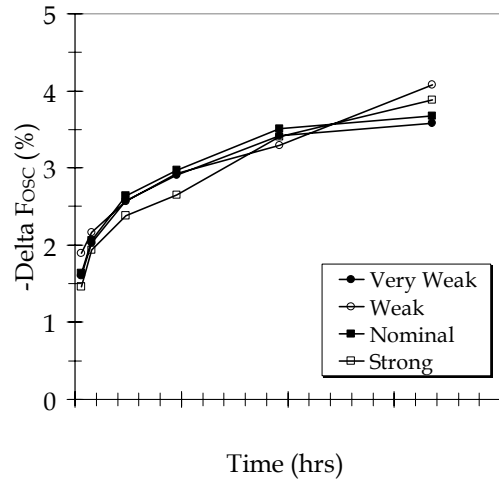
**Figure 11:** Delta Vmin (mV) versus Stress Time.



**Figure 12:** Delta Fosc (%) versus Stress Time.



**Figure 13:** Delta F<sub>Max</sub> (%) versus Stress Time for the four transistor corner splits.



**Figure 14:** Delta F<sub>OSC</sub> (%) versus Stress Time for the four transistor corner splits.

### 4.3 Product Parametric Drift - Modeling

In the previous section, we described the experimental data that suggests a NBTI dependence. It is therefore a natural extension to consider a NBTI kinetics model to describe the drift behavior. If the extracted kinetics from the product data matches the component results, this would give added confirmation of this behavior.

There have been several formulations of NBTI kinetics reported in the literature to describe the kinetics of transistor parametric drift [3,12,13,14]. We have chosen one such formulation to illustrate the parametric drift modeling approach [12]. The underlying assumption we make is that the product parameters follow the same NBTI kinetics as at the transistor level. This assumption will be later shown to be correct. The parameter drift formulation for  $\Delta F_{Max}$  is then given as Equation 1.

$$\Delta F_{Max} = A_o * e^{\beta V} * e^{-E_A/k_B T} * t^n \quad (\text{Equation 1})$$

Where the model parameters are:

$A_o$	Pre-Factor (Units of measured parameter)
$\beta$	Voltage Coefficient (1/V)
$E_A$	Thermal Activation Energy (eV)
$n$	Power-law slope

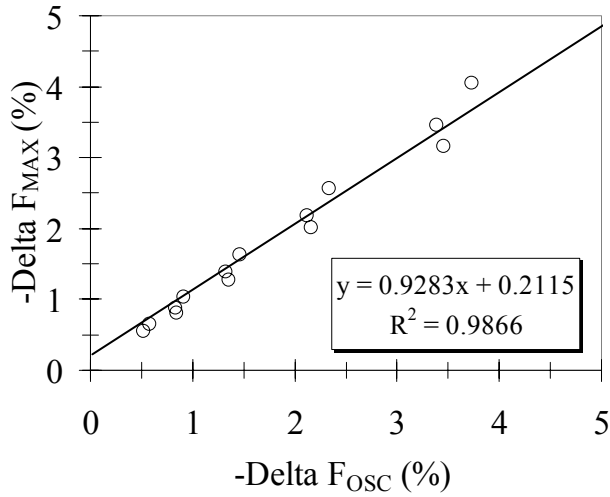
and the other equation values are:

$T$  = Temperature (K)

$k_B$  = Boltzmann's Constant (eV/K)

Although Equation 1 is a non-linear equation, it can be easily linearized by taking the natural logarithm of both sides. The four model parameters can be extracted by solving a multiple linear regression equation with a data set from the experimental data.

We extract the model parameters for the  $\Delta F_{Max}$  and  $\Delta F_{OSC}$  data, shown in Figures 10 and 12, and then plot the model parameter drift against each other in Figure 15. We see an extremely good correlation between the two drift parameters with almost a one-to-one relationship between the two parameters. The model parameters in equation 1 are independently calculated for  $F_{Max}$  and  $F_{OSC}$ . A slope near one with the high  $R^2$  is a strong indication of the simultaneous matching of all the extracted parameters. Further, we note that the RO  $F_{OSC}$  drift is only due to NBTI. Therefore, we can say that the majority of the product  $F_{Max}$  drift is due to NBTI.



**Figure 15:**  $-\Delta F_{Max}$  versus  $-\Delta F_{OSC}$  drift from the experimental data of Figures 10 and 12.

To further establish the correlation between NBTI and product parametric drift, it is instructive to compare the power-law time dependence slope at the transistor, RO, and product level as shown in Table 1.

Level	Power-Law Slope
Transistor	$0.20 \pm 0.01$
Ring Oscillator	$0.20 \pm 0.01$
Product – $F_{Max}$	$0.20 \pm 0.02$
Product – $V_{Min}$	$0.20 \pm 0.02$

**Table 1:** A comparison of the power-law slopes of the parameter drift at the various abstraction levels.

As Table 1 shows, all levels of abstraction give a power-law slope of 0.20. We know from the transistor level data shown in Figure 2 that such a slope value is indicative of NBTI. This is further experimental evidence that NBTI degradation is responsible for the product parameter drift.

#### 4.4 Product Parametric Drift - Test Guard-banding

Now that it has been established that NBTI drift can result in product parameter drift, it is necessary to calculate the expected parameter drift under BI and customer-use conditions. Since a product can have different quality and operational requirements depending on the targeted market segment, a flexible test guard-banding technique is required.

As an example, a product may undergo BI and exhibit an  $F_{Max}$  drift (decrease). It is desired to set a frequency test guard-band to account for both the BI induced drift and the subsequent customer-use drift. We show below a method to calculate the expected  $F_{Max}$  drift under both BI and customer-use.

Given a BI and Customer Use condition:

$T_{BI}$	BI Temperature (K)
$T_{Use}$	Use Temperature (K)
$V_{BI}$	BI Voltage
$V_{Use}$	Use Voltage
$t_{BI}$	BI time duration
$t_{Use}$	Use time

Assuming that we have already determined the functional relationship for the  $F_{Max}$  drift by Equation 1, we can translate the BI condition to the customer use condition to have a common frame of reference. The customer use condition equivalent of BI is then given by Equation 2.

$$t_{Use}^{Eq.} = e^{\frac{\beta}{n}(V_{BI} - V_{Use})} * e^{\frac{E_A}{k_B n} \left( \frac{1}{T_{Use}} - \frac{1}{T_{BI}} \right)} * t_{BI} \quad (\text{Equation 2})$$

The BI induced  $F_{Max}$  drift is then given by Equation 3.

$$\Delta F_{Max, BI} = \Delta F_{Max} \left( V_{Use}, T_{Use}, t_{Use}^{Eq.} \right) = A_o * e^{\beta V_{Use}} * e^{\frac{E_A}{k_B T_{Use}}} * \left( t_{Use}^{Eq.} \right)^n \quad (\text{Equation 3})$$

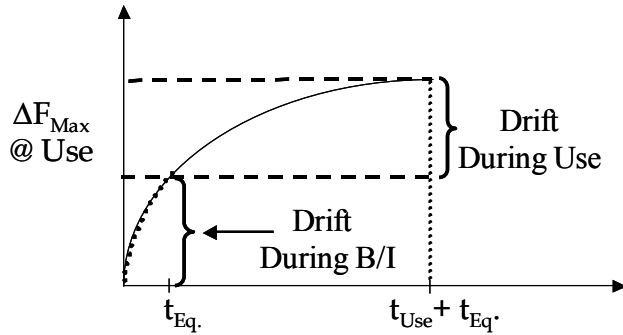
After the part has undergone BI and shipped to the customer, it will operate at a product use condition and thus an additional  $\Delta F_{Max}$  drift will occur. The total  $F_{Max}$  drift will be then given by Equation 4. If the  $F_{Max}$  test guard-banding is done before BI, then the guard-band is given by Equation

4, which accounts for both BI induced and customer use drift.

$$\Delta F_{Max,Total} = A_o * e^{\beta V_{Use}} * e^{-\frac{E_A}{k_B T_{Use}}} * (t_{Use}^{Eq.} + t_{Use})^n$$

(Equation 4)

A schematic representation of the  $\Delta F_{Max}$  behavior under BI and customer use conditions is given in Figure 16. The tester guard-band should be the sum of the BI and Use drift.



**Figure 16:** Schematic representation of the  $\Delta F_{Max}$  behavior under BI and customer use conditions.

## 5 Conclusion

We have shown in this paper the impact of NBTI spanning from the transistor level to the product level. The significant impact of NBTI on a high performance IC has necessitated a systematic test methodology to quantify NBTI induced parameter drift. Details of this systematic technique and supporting data have been presented to establish an unequivocal correlation between NBTI and product parametric drift. The methodology reported here should allow a straightforward technique to comprehend the NBTI impact on high performance products fabricated in deep sub-micron processes.

## 6 Acknowledgments

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## 7 References

[1] J. Segura, A. Keshavarzi, J. Soden, and C. Hawkins, "Parametric Failures in CMOS ICs – A Defect-Based Analysis," *Proc. 2002 IEEE Int. Test Conf.*, pp.90-98, 2002.  
 [2] K. N. Quader, P. K. Ko, and C. Hu, "Projecting CMOS Circuit Hot-Carrier Reliability from DC Device Lifetime," *Proc. of Int. Electron Devices Meeting*, pp.511-514, 1993.

[3] D. Schroder and J. Babcock, "Negative Bias Temperature Instability: Road to cross in deep submicron silicon semiconductor manufacturing," *Journal of Applied Physics*, Vol. 94, No. 1, pp. 1-18, 2003.  
 [4] A. T. Krishnan, V. Reddy, S. Chakravarthi, J. Rodriguez, S. John, and S. Krishnan, "NBTI Impact on Transistor & Circuit: Models, Mechanisms, & Scaling Effects," *Proc. of Int. Electron Devices Meeting*, pp. 349-352, 2003.  
 [5] K. O. Jeppson and C. M. Svensson, "Negative Bias Stress of MOS devices at high electric fields and degradation of MNOS devices," *Journal of Applied Physics*, Vol. 48, No. 5, pp.2004-2014, 1977.  
 [6] R. Thewes, R. Brederlow, C. Schlunder, P. Wiczorek, B. Ankele, A. Hesener, J. Holz, S. Kessel, and W. Weber, "Evaluation of MOSFET Reliability in Analog Applications," *European Solid-State Device Research Conference*, 2001.  
 [7] V. Reddy, A. T. Krishnan, A. Marshall, J. Rodriguez, S. Natarajan, T. Rost, and S. Krishnan, "Impact of Negative Bias Temperature Instability on Digital Circuit Reliability," *Proc. of the International Reliability Physics Symposium*, pp. 248-254, 2002.  
 [8] F. Pagaduan, J. K. Lee, V. Vedagarbha, K. Lui, M. Hart, D. Gitlin, T. Takaso, S. Kamiyama, and K. Nakayama, "The Effects of Plasma-Induced Damage on Transistor Degradation and the Relationship to Field Programmable Gate Array Performance," *Proc. of the International Reliability Physics Symposium*, pp. 315-318, 2001.  
 [9] A. Bhavnagarwala, X. Tang, and J.D. Meindl, "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability," *IEEE Journal of Solid State Circuits*, Vol. 36, no. 4, pp. 658-665, 2001.  
 [10] Y.H. Lee, N. Mielke, B. Sabi, S. Stadler, R. Nachman, and S. Hu, "Effect of pMOST Bias-Temperature Instability on Circuit Reliability Performance," *Proc. of Int. Electron Devices Meeting*, pp. 353-356, 2003.  
 [11] O. Semenov, A. Vassighi, M. Sachdev, A. Keshavarzi, and C.F. Hawkins, "Burn-in Temperature Projections for Deep Sub-micron Technologies," *Proc. 2003 Int. Test Conf.*, pp.95-104, 2003.  
 [12] G. La Rosa, F. Guarini, S. Rauch, A. Acovic, J. Lukaitis, and E. Crabbe, "NBTI – Channel Hot Carrier Effects in PMOSFETs in Advanced CMOS Technologies," *Proc. of the International Reliability Physics Symposium*, pp.282-286, 1997.  
 [13] S. Mahapatra and M.A. Alam, "A Predictive Reliability Model for PMOS Bias Temperature Degradation," *Proc. of Int. Electron Devices Meeting*, pp.505-508, 2002.  
 [14] S. Ogawa, M. Shimaya, and N. Shiono, "Interface-trap generation at ultra-thin SiO<sub>2</sub> (4-6nm)-Si interfaces during negative-bias temperature stressing," *Journal of Applied Physics*, Vol. 77, No. 3, pp.1137-1148, 1995.