IN SEARCH OF THE OPTIMUM TEST SET – ADAPTIVE TEST METHODS FOR MAXIMUM DEFECT COVERAGE AND LOWEST TEST COST

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Abstract

Maintaining product quality at reasonable test cost in very deep sub-micron process has become a major challenge especially due to multiple manufacturing locations with varying defect and parametric distributions. Increasing vector counts and binary search routines are now necessary for subtle defect screening. In addition, parametric tests and at-spec testing is still often necessary to ensure customer quality. Systematic defects are becoming more common and threaten to dominate the yield Pareto. Adaptive test methods are introduced in this paper that demonstrate the capability of increasing or decreasing the test coverage based on the predicted or measured defect and parametric behavior of the silicon being tested. Results promise an increase in product quality at the same time a reduction in test costs.

1. Introduction

Abraham Lincoln said *"You may deceive all the people part of the time, and part of the people all the time, but not all the people all the time."* In the quest for identifying the most optimum test set for defect and performance based testing an appropriate adaptation of that famous quote could be: *" You can test for all of the defects part of the time, part of the defects all of the time but you cannot test for all the defects all of the time!"* This sums up the test cost vs. test quality trade-off problem. The cost of applying all the "necessary" test vectors, temperatures, voltages, Fmax and MinVDD (with binary searches), IDDQ, Functional and At-Speed patterns, Path Delay tests, I/O tests and diagnostic patterns is excessive and certainly not in line with our profitability targets. However, the behavior of defects in Very Deep Sub-Micron (VDSM) processes is systematic and often design dependant in nature [1]. This is increasing the need to adapt new test methods to supplement the traditional stuck-at tests. Also, consider the fact that if an IC is defect-free and meets all of the performance requirements, it does not need to be tested at all! The same issue applies for burn-in where often 100% of the ICs are burned in even though a very small percentage of the ICs have latent defects. The burn-in of defect-free die actually reduces the wear out lifetime of the IC, increasing danger of damage due to handling, thermal runaway or overstress. The obvious problem is that we do not know, in advance, which ICs are defect-free and which ones meet the performance requirements. The key to adaptive test is to utilize data generated from the tester or relevant data from previous processes or measurements in predicting the process for the future tests in order to reduce or increase testing as and when required. The ultimate goal is to apply only the minimum set of tests required to screen the ICs that will fail in the system either as shipped or over time. This will be referred to, in this paper, as the Optimum Test Set (OTS).

Adaptive testing is not a new concept. It has been applied to parametric testing to reduce test costs of analog or mixed signal testing [12]. Test time savings of 26% were noted with the application of adaptive parametric testing [2]. Adaptive test methods for cost reduction have also been applied to path delay tests [3], diagnostic tests [4], test scheduling [5] and IDDQ [6]. Adaptive test has also been shown to improve quality through off-tester post processing and adaptive limit setting for IDDQ and MinVDD outlier screening tests based on neighborhood and other variance prediction techniques [7-9].

Closing the gap between the OTS and the minimum test without sacrificing product quality requires two things:

1. Advanced knowledge of the potential defectivity or performance of the IC being tested;
2. A method of applying different tests or different test flows to selective ICs (on a wafer or in a batch/lot) based on the advanced knowledge.

In this paper, we look at some new adaptive test ideas for increasing defect coverage while reducing test cost and the combined application of the old and new methods towards reaching the Optimum Test Set.

2. Definitions and Terms

Structural Test – Tests to determine any manufacturing defects in the DUT using structures built into the chip.

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Functional Test – Tests using design verification patterns provided by customer or designer and run at product specified speed

At-Spec – Ensuring that a part is operating within the performance space guaranteed for the customer

Parametric Test – Performance testing of cells or cores to ensure that the part lies within the specified process window

Statistical Post-Processing™ (SPP) – Applying statistical techniques to test data for meeting product quality or extracting information.

Minimum Test Set (MTS) - The non-adaptive test set required to ensure required levels of quality

Optimum Test Set (OTS) – The test set that only contains the tests that would make each individual part fail. Different for every part

Predictive Test Set (PTS) - The Test set applied to gather information for prediction of future behavior of the IC.

Adaptive Test Set (ATS) - The dynamic test set used to target specific defects or parametric variation based on results from the PTS

Etest – Electrical Test usually performed on scribe line. WAT is the foundry term for Etest

3. Optimum Test Set (OTS) vs. Minimum Test Set (MTS)

The MTS is the smallest possible set of tests required to ensure that the product tested meets the required quality. If an IC has no defects and meets all the performance requirements at all the specified temperatures and voltages – then it does not need any test. If the IC has a stuck-at defect in the memory only then it only requires a single voltage memory vector targeted for that specific fault. The same concept applies for a stuck-at defect in the logic circuitry. For subtle defects, the situation is more complex. To screen an IC with a resistive defect, a binary search routine and a delay fault test pattern may be required to ensure defect coverage. For bridging defects an IDDQ pattern or multiple detect stuck-at pattern may be required. For performance tests, including I/O, memory, mixed signal, DSP and processor performance, extensive at-speed testing at specified frequencies is required only when the ICs are marginal to the specification. The Minimum Test Set (MTS) necessary to screen all of these defects with traditional (non-adaptive) test techniques requires application of the complete test suite with all the necessary vectors, binary searches, IDDQ screens, and performance tests. The optimum test set is the set of specific tests or vectors required to target and screen the defects on each IC. If no defect is present then minimal testing is required. The optimum test set represents an absolute lower bound on the test time that would be required to capture all bad die, and is not being suggested as an actual testing methodology but merely an illustration of the power of adaptive test. Wafer test time for MTS and OTS can be characterized by (1) and (2).

Wafer Test Time (MTS) = Full Test Time (passing die) + Time for Passing Tests preceding the Failing Test (failing die) + Time for Failing Test (failing die). (1)

Wafer Test Time (OTS) = Time for Failing Test (Failing Die) (2)

Test	Die Fallout	Test Time	Cum. Time	MTS Time (s)	OTS Time (s)
Test 1	906	0.21	0.21	193.88	193.88
Test 2	925	0.05	0.26	240.50	42.55
Test 3	6448	0.18	0.44	2856.46	1179.98
Test 4	372	0.03	0.47	175.69	11.16
Test 5	368	0.12	0.60	219.70	45.63
Test 6	467	0.18	0.78	364.73	85.93
Test 7	7	0.07	0.85	5.98	0.51
Test 8	93	0.16	1.02	94.67	15.25
Test 9	2	0.03	1.05	2.09	0.05
Test 10	66	0.16	1.20	79.40	10.43
Test 11	13	0.13	1.33	17.26	1.63
Test 12	2	0.16	1.49	2.98	0.33
Test 13	2	0.07	1.56	3.12	0.14
Test 14	304	0.70	2.26	687.04	212.80
Test 15	272	0.17	2.43	659.60	44.88
Test 16	0	0.60	3.02	0.0	0.0
Test 17	0	0.19	3.22	0.0	0.0
Test 18	0	0.32	3.53	0.0	0.0
Pass all tests	7003	0.00	3.53	24741.60	0.0
Total				**8.43 hours**	**0.51 hours**

Table 1: MTS and OTS test times for sample population

To demonstrate this model, a sample of parts was tested with full override testing. Both the MTS and OTS test times are calculated and the results presented in Table 1. The first column shows the different tests being applied and the second column has the fallout for each test. The associated test time and cumulative test time are broken out by test application. The MTS time is the product of the die fallout and the cumulative test time. The OTS time is the product of the die fallout and the test time for only the test that was failed. From the table it is shown that the MTS requires over 8 hours whereas the OTS would only take 30 minutes. A simplifying assumption was made in this table for ease of readability: the OTS time is based on the first test that fails, not the fastest test that fails. By only conducting the fastest test that marks a die as fail, the time can be driven down to 20 minutes. Another assumption is that a test takes the same amount of time to complete whether the die fails or passes. This assumption leads to another overestimate of the actual OTS time because many tests stop after they fail the first vector.

Even with these assumptions, the test time for the OTS is only 6% of the test time required for the MTS.

4. Adaptive Test for Parametrics

Performance testing to specifications is very expensive due to the hardware costs and test time costs of applying the tests at the required voltages and frequencies and at the temperature guaranteed for that product. For Mixed Signal, I/O and RF testing the situation is even more complex due to the vast variety of specifications that need to be met and the complexity of the hardware necessary to support these tests.

Avoiding or reducing the need for these tests is critical in reducing test costs, however a failure to screen performance tests can be catastrophic for end customer quality if the performance is out of specification. A solution to this dilemma is to apply adaptive test methods using parametric prediction as an input to the adaptive test decision process. Examples of data sources that can be used for parametric prediction include:

1. In-line Fabrication Measurement Data;
2. Scribe Line Electrical Test data;
3. Parametric Test Chip Data;
4. Correlated Parameters from the same IC [2];
5. Correlated Parameters from similar tests on other ICs in production;

Parametric performance is generally measured in Cp/Cpk. These are measures of the capability of the process to meet the specification window. Cpk compares the parametric (6 sigma) distribution to the specification window such that if the Cpk is greater than 1.0, the six sigma variation is less than the specification window. Cp measures the centering or targeting of the distribution to the specification limits so a Cp > 1 means that the process is well centered with respect to the target. The relevance of Cp/Cpk to at-spec testing is that if the Cp/Cpk of the process is greater than 1, the need for performance testing is vastly reduced.

An example of the application of adaptive test for parametrics is the scribe line Etest measurements made on all wafers at the end of Fabrication Processing. This is a sample test where many measurements are made on 5-9 sites on a wafer to validate the correct processing of the wafer. Typically these measurements include Threshold Voltages (Vt), Drive Currents (Idsat), Via and Metal Resistances, Oxide Breakdown, leakages and mixed signal parameters. Based on these scribe line measurements and their correlation to the Product Performance, a good prediction can be made for the need to apply performance tests on ATE for each lot, each wafer and even each region of the wafer. Silicon with good predicted parametric performance can be targeted for defect based testing only or low cost/low pin count structural testers whereas silicon that has been identified as high risk based on the Etest data, can be targeted for full at-spec testing. Obviously there are many other options where silicon that has been identified as high risk for certain parameters (e.g. mixed signal, high speed I/O) or combinations of parameters (e.g. transistor drive current and metal resistance) can be targeted for at-spec testing of these parameters only.

Assume a process with a Cp and Cpk of 1.0, a full at-spec test cost of $300 a wafer, a low cost/structural only test cost of $50 a wafer and a volume of 10000 wafers per month. If wafers outside 2-sigma (97.7%) of the process target are considered high risk and require full at-spec testing and wafers within 2-sigma are targeted for structural defect based testing only, then a saving of $2.4M per month can be realized. Also higher defect coverage may be possible by applying more test vectors on the structural test systems at lower cost.

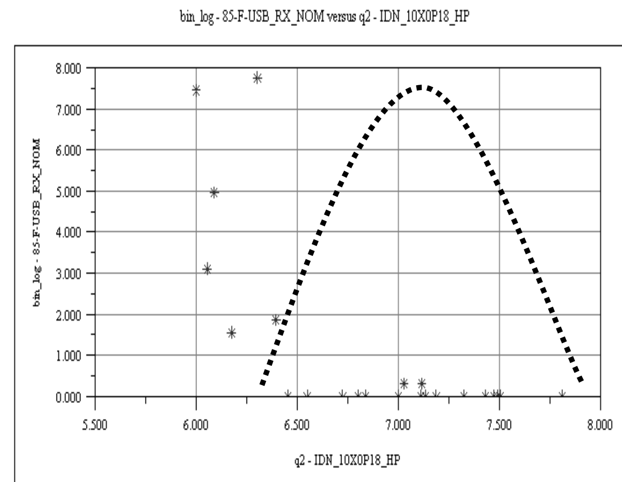

Figure 1: Showing fail rates (*) for parametric functional test vs. median N-channel transistor drive current. Manufacturing frequency distribution for N-Channel Drive Current is also shown (dotted line).

Figure 1 shows an example of functional parametric fail rate for a 0.18µm ASIC showing a clear correlation to Etest parametrics (N-channel Drive Current). The only functional fails are seen at the very tail of the manufacturing distribution. Figure 2 shows a simplified flow chart for a parametric adaptive test flow. In this case wafers are targeted for low cost structural tests if the Etest data shows wafer medians < 2 sigma from target and full functional if wafers are > 2 sigma. This methodology can be expanded and improved to allow for across the wafer variation so that wafer neighborhoods can be targeted for adaptive parametric test based on die location. In this application, the adaptive test would be at final/package

test using Die Tracing or by special binning at Wafer Sort using Statistical Post-Processing based on die location.

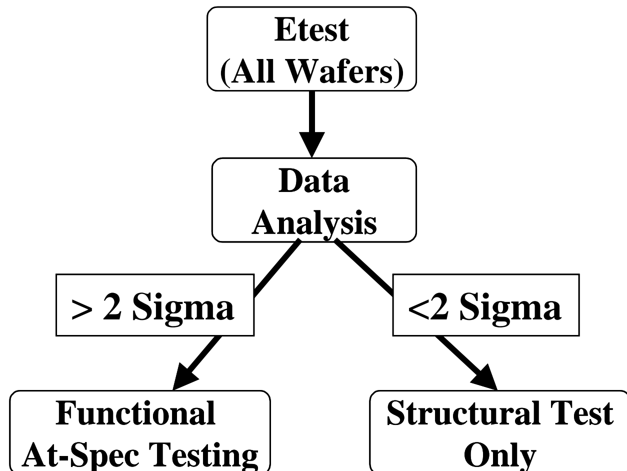

Figure 2: Showing an example Adaptive Test for Parametrics test flow where wafers are targeted for different test systems based on Etest data variation.

5. Adaptive Test for Defect Coverage

One of today's biggest test challenges is the ever-growing number of test vectors required to meet fault coverage goals. This is driving test costs and the need for vector compression and embedded test. Several types of patterns are included in order to get high coverage of as many different kinds of defects as possible (N-detect, TDF, etc.). The conventional approach has been to apply all the patterns that are available until the tester memory is full or the test times required to execute the patterns becomes prohibitively expensive. Adaptive test for defect coverage seeks to maximize the test coverage for the actual defect mechanisms plaguing a wafer while minimizing tests that would have little or no fallout.

The minimum test set is used for all parts being tested to ensure adequate test coverage for fabrication defect fluctuations. For systematic and design dependent defects this is more important because of the very high fail rates that can be experienced when they occur. For example, resistive vias caused by systematic underetching will lead to high fallout in TDF patterns. However when the problem has been isolated and rectified the TDF fallout may dwindle to zero. Another example is node-to-node bridges caused by photoresist residue. These bridges are best screened by use of an N-detect pattern, yet when only the baseline defectivity affects a part it may be preferred to maximize stuck-at coverage. The defect Pareto for a product can change from lot-to-lot and wafer-to-wafer. Adaptive test for defect coverage uses information from various sources to try and predict the systematic defect issues and adapt by varying the tests being applied.

Defectivity prediction for latent defects has shown good correlation to the results on silicon [10]. However prediction of killer defects has not been investigated as much but should show similar behavior due to the clustering nature of the defects. Depending on the defectivity of the silicon some prediction of defectivity needs to be available. Potential predictors of defectivity include:

1. In-line Fabrication inspection results
2. Test Chip defectivity results
3. Electrical test results
4. Failure rate of ICs on material from the same fabrication site
5. Failure rate of ICs on the same fabrication wafer, lot, or product

While all five methods should be highly effective for defectivity prediction, the focus of this paper will be on 4 as it is the simplest for data analysis and educational purposes.

There are many possibilities for determining the PTS and applying the ATS for minimum test cost and maximum defect coverage. Some of these possibilities are discussed below.

1. Wafer Level Adaptive Defect-Based Testing: Here the wafer would start testing using the PTS and the fail rates for each vector type would be recorded and calculated. As the fail rate of any vector increases, the ATS would proliferate the failing vector for maximum defect coverage and possibly, eliminate the vectors showing no fails. This method could also be implemented using a re-test method, so that certain die locations on the wafer are re-tested using the ATS after analysis of the results from the PTS. This method is the ideal method for systematic defects.
2. Lot Level Adaptive Defect-Based Testing: In this method, the PTS would be used for certain tested lots (e.g. For a new foundry or new product or new workweek) and the fail rates would be calculated so that the ATS is optimized for maximum coverage and lowest cost. The PTS could be performed at different temperatures to check for temperature dependent defects. Ideally this is automatic but could also be performed manually.

3. Feed-Forward Adaptive Defect-Based Testing: Using die-tracing capabilities, results of the PTS at wafer sort could be fed-forward to package testing for the ATS to be applied [13].

The remainder of this section offers a couple examples of how adaptive test for defect coverage can be leveraged. The first example is a discussion on screening for differing types of defects and can be applied at the wafer level, lot level, or have the results fed forward to final test. The second example uses cumulative statistics from previous lots on the same product to try and estimate areas of high defectivity.

One major advantage we have with our test vectors is that, if ordered correctly, the vast majority of defects are identified within the first few hundred vectors. Previous work has shown this to be true for stuck-at defects as well as frequency dependent defects [11]. This is leveraged in adaptive testing of many defect types using small but targeted vectors and then adaptively increasing or decreasing the vector sizes depending on the fail rate of these targeted vectors. The test set including these small, targeted vectors is called the Predictive Test Set (PTS) and the test set used for maximum defect coverage is the Adaptive Test Set (ATS). Figure 3 is an illustration of the Predictive Test Set. It is a subset of all possible vectors using only the first few vectors with the highest coverage. Figure 4 illustrates an example of the Adaptive Test Set. In this example the PTS declared the best defect coverage comes from mostly stuck-at coverage, equal parts inline resistance fault (IRF) and transition delay fault (TDF) coverage, and the least coverage on N-detects [14][15].

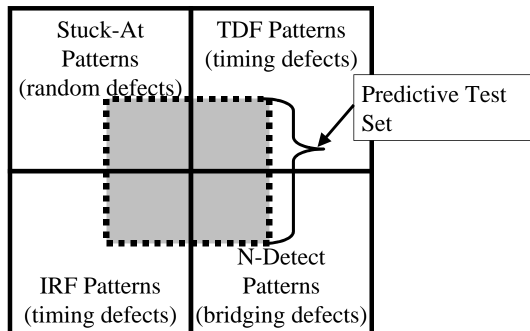

Figure 3: Predictive Test Set

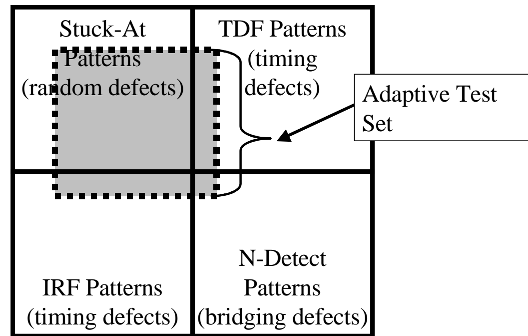

Figure 4: Adaptive Test Set

The second example uses lot level adaptive defect-based testing. A yield stackmap was generated using data from the stuck-at scan pattern of 1659 wafers. A subset of the pattern (first 5% of the original pattern) is used as the predictive test set. It reveals, from figure 5, a spatial correlation in which lower yields were found at the edges and center of the wafers (dark regions on the stackmap). Figure 5 shows the yield stackmap of the PTS where the darker areas are regions with higher fallout. Areas of higher yield fallout have long been known to also be areas with higher escape rates. Using cumulative lot level statistics and the predictive test set the adaptive test set could be the first 5% of the scan pattern on the whole wafer and the entire pattern (100%) on the edges and in the center.

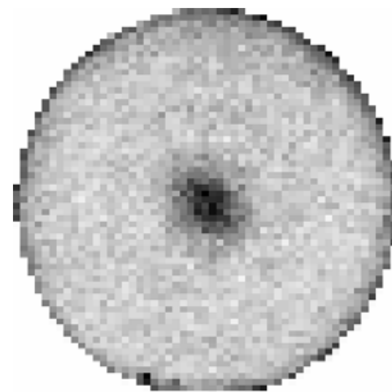

Figure 5: Cumulative count of die failing in the first 5% of the scan pattern

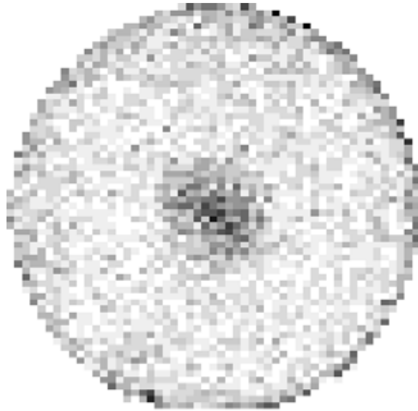

Figure 6: Cumulative count of die failing only in the last 95% of the scan pattern

Looking back at only the test escapes (5% - 100%), the darker areas in Figure 6 reflect higher numbers of escapes which on average occur more frequently at the edges and center of the wafer, justifying the use of the ATS.

6. Adaptive Test for Outlier Screening

Adaptive Test methods have been successfully applied to outlier screening using on-tester and off-tester IDDQ and minVDD limits setting [7-9]. However using adaptive test to screen more aggressively is not just about when and how to apply more tests. For some tests, just the way they are applied may have a significant impact on product quality. MinVDD and Fmax testing have proven to be invaluable in screening a variety of defect mechanisms including resistive vias and metal shorts [9]. Often these types of defects are not purely random but systematic in nature. Throughout a product's lifetime excursions in minVDD defect behavior are often observed. An example of this type of behavior is shown in Figure 7. The figure shows memory minVDD versus delay for two wafers from the same production lot. One of the wafers has experienced an excursion such as that discussed above while the other has not.

Two methods are commonly employed to screen defects with this type of behavior, a 2-voltage test and a binary search. The 2-voltage test runs a pattern at nominal and low voltage in order to verify outlier behavior. In the case shown in figure 7, the voltages are 1.8 and 1.62V (10% less than the 1.8V nominal). The benefit of this approach is the small test time and the ability to conduct all tests on-tester. The downside is reduced resolution of the defects. This approach is ideal for Wafer 275 in Figure 7, as it may be argued that the test time cost associated with performing a binary search exceeds the cost of a small number of escapes.

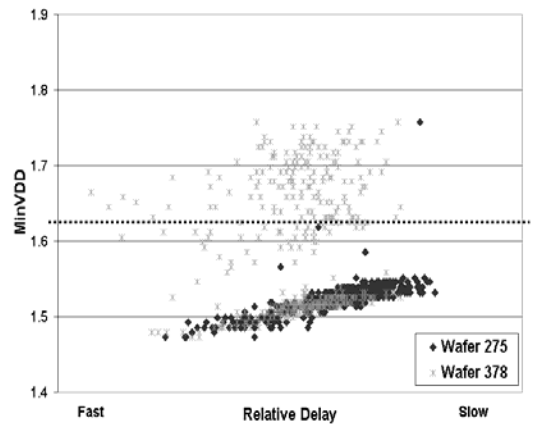

Figure 7: MinVDD Characteristic (2 wafers)

The other approach uses a minVDD binary search and performing Statistical Post-Processing of the data. This technique gives the resolution shown above and is able to expose all outliers to the intrinsic distribution. This is the approach taken by the MTS and is designed to capture defects detectable by memory minVDD. The downside to applying SPP is that it will add the most test time by requiring a binary search and not allowing stop on first fail. Wafer 378 in Figure 7 is an example that requires a minVDD search and SPP in order to achieve an acceptable rate of test escapes.

Adaptive test is a tuning knob that enables an engineer to optimize test cost against outlier identification. The decision rule will be based on the cumulative count of die on a wafer that fails the memory pattern at the low voltage test but passes the test at nominal voltage. By conducting adaptive test optimized for test time reduction, the flow would follow the chart shown in Figure 8. By default, the PATTERN is always tested at a low voltage called VDDL. If PATTERN has a high occurrence of fails at VDDL, the flow switches to a binary search for the remainder of the wafer. The cumulative count that is required for the switch (called TRIGGER) allows for the traditional tradeoff between test time and stringency. This approach is adaptive to excursion behavior while minimizing test time for parts that don't need the additional resolution to satisfy quality requirements.

In the case presented here, any die that has a data point above the 1.62V limit is tallied. For wafer number 275, 169 parts fail the low voltage memory pattern. In contrast, "Cumulative Fails" = 1 on wafer 275.

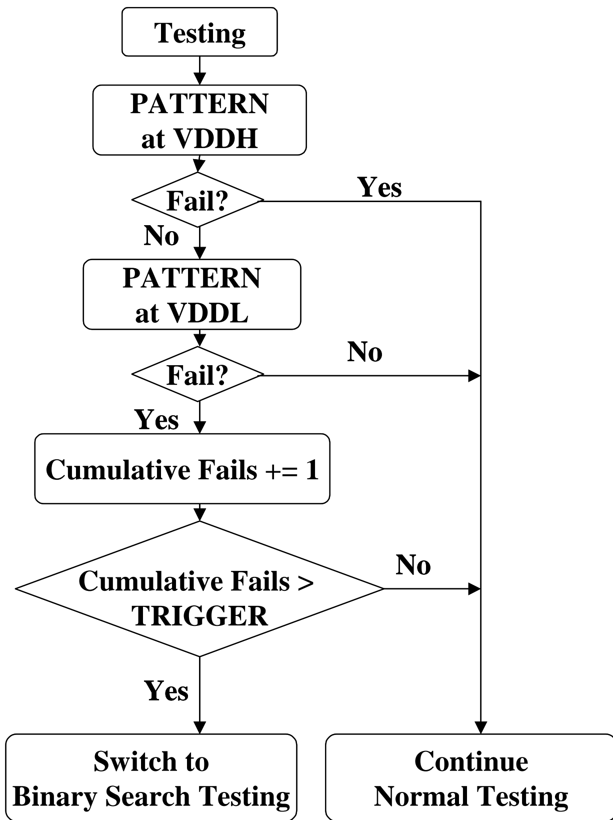

Figure 8: Flow for Adaptive MinVDD Testing

Assuming the outliers are randomly distributed, 3.3 parts are tested in order to find 1 outlier on Wafer 275. If a TRIGGER of 10 die is required to trigger a switch to a binary search, only 3.3*10= 33 die will be tested without the additional information provided by minVDD testing. In contrast, using adaptive test methods on Wafer 378 will never be subject to the additional expense of full minVDD testing.

	Wafer 275	Wafer 378
Total data points	553	514
Pass @ 1.8V, fail @ 1.62V	169	1
Additional Captures from binary search	38	3

Table 2: Results from Figure 3

When applying adaptive test, parts are randomly sampled and tested using an exhaustive test set including per pin Fmax and per pin minVDD testing. If a scenario arises such as the one above, adaptive test would cease to test the entire pattern and only screen based on the pin associated with the most defects. When the fabrication cycle is shifted and the scenario is no longer an issue, adaptive test would turn to applying the method deemed optimal given the most recent data.

7. Adaptive Test for Test Cost Reduction

7.1 Adaptive Test and Test Pattern Re-ordering

As test cost becomes a significant percentage of the manufacturing cost, the test vectors order promises to provide reductions in both test vector application time and test pattern volume, which are important for holding the line on pattern memory requirements. Figure 9(a) is a histogram plot of the first-failing-vector for an on-tester sample of a single TDF-test on 25 wafers. With some ATE support for the first-fail data is a relatively low cost addition to a test program. The total pattern size is 6,000 vectors. A few observations about this test highlight the potential of adaptive vector order. Typical of most tests, the first ten percent the test pattern (vector 600) detects a large number of the faulty parts (≈90%). The remaining vectors generally constitute a large fraction of the test set, but identify few faulty parts. In a total pattern of 6,000 vectors, four percent of the pattern (255 vectors) failed the 2,099 parts in the TDF-test. For the 255 vectors 67% screened a single faulty die. These statistical characteristics are common. However, defectivity randomizes the pattern of first failing vector. The next 25 wafers will have the similar statistics but not the same failing vectors and not the same failing vector pattern.

Vectors in patterns are ordered for fault coverage. In the context of test pattern re-ordering a pattern to put the highest fault coverage patterns first is an adaptation however, the ordering is static. Pattern ordering at ATPG can not reflect the defectivity of a particular lot. This section concludes two, simple demonstrations to provide some food-for-thought about the potential benefits and challenges of adaptive reordering. A summary of the test statistics for the two demonstrations can be found in Table 3.

Test Statistics	Actual	Simulated
Scan Yield for 1 Lot	15151	12651
Defective Die (DD)	2099	4599
First Failing Vectors (FFV)	255	259
Good Die Test Time per Die	0.3 S	0.3 S
Good Die Test Time per Lot	4545 S	3795 S
DD Test Time per Lot	16 S	611 S
DD Test Time per Lot after Pattern Re-ordering	8 S	16 S

Table 3: Statistics for test pattern Re-ordering

For the test fail pattern in Figure 9(a) the total test time to screen all the defective parts is 16 seconds. For simplicity assume that each failing parts only fails the first-failing vector. In other words, if the pattern is reordered the same parts fail the same vectors, only the timing of the pattern execution changes. If test pattern is re-ordered such that the vectors are sorted from highest fail count to the lowest the test time for the lot reduces to 8 seconds.

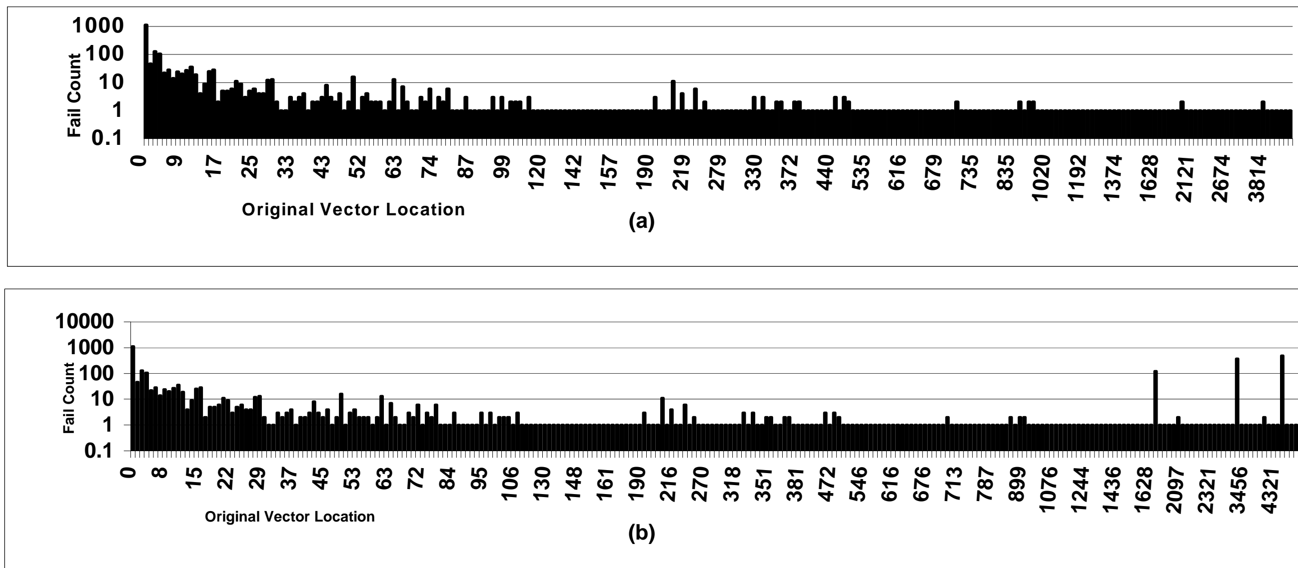

Figure 9: Fail Count per Vector (a) Actual; (b) Simulated

Although the 50% reduction in defective part test time for the lot is significant it has to be put in context of total test time (healthy + faulty) and even with the aid of initial static fault coverage ordering the number of possible permutations is enormous.

The choice of fault model for vector ordering and random defectivity influence the observed first-fail characteristics in Figure 9(a). Vectors are ordered based on the assumption that all faults are equally weighted and the defectivity is random distribution (e.g. Poisson or negative binomial). The vector that detects the largest number of faults will indeed capture the largest number of failing die if the two assumptions hold. A signature of these conditions holding is the gradual decline in the first-fail count from the first vector in the pattern to the last.

The second example is a simulation based on the data from the on-tester data collection and demonstrates the potential value of incorporating dynamic re-ordering based on the observed first-fail rates. To simulate this example, four vectors are added towards the end of the pattern. Figure 9(b) shows the plot of fail counts per vector for the simulated pattern. These four vectors are assumed to identify a repeating, systematic defect on the wafer, 2,500 parts on the twenty-five wafers. By inserting the detecting vectors near the end of the 6,000 vector pattern the 2,500 additional systematic failures increased the faulty part test time for the lot to 611 seconds. The first-fail plot characteristic signature changes from the gradual roll-off to a boat shaped pattern. Such a pattern is very unlikely to occur for random defectivity and uniform distribution of faults. Using the same assumptions about single vector fails when this pattern is re-ordered, defective die test time drops to 16 seconds. The benefits of this large test time reduction are an artifice of the simulation.

The reduction of this demonstration is an artifice of the simulation. However, benefits of large test time reduction can be realized in practice however at least two challenges must be addressed. First, the success adaptive reordering of test patterns is closely tied to characterization of the faults and defects each vector is testing for. Second, ATE requires an efficient mechanism to capture and store the first-fail data.

7.2 Adaptive Binary Search

This section presents an adaptive approach towards test cost reduction. MinVDD and Fmax outlier screens can lead to customer quality improvement with reduced yield loss and less overkill [11]. The regular binary search routines require 8 to 10 tests before finding the search target. These search routines make it cost prohibitive to implement the minVDD and Fmax screens in production. Adaptive binary search routines can reduce this number to 2 or 3 tests using predictive data from previous die. The computational complexity for a regular binary search is given by:

$$n = 3 + \mathrm{int}\left(\frac{\log\left(\frac{R}{r}\right)}{\log(2)} \right) \qquad (3)$$

Where, n is the number of searches taken to find the target value. R is the range of VDD values for search and r is the resolution of search.

Figure 10, explains the algorithms' search criteria. The search regions marked on the plot represent the search points for both the approaches on 1st iteration of the search. The regular binary search algorithm assumes a linear CDF (solid line) for minVDD distribution. The search starts at 50% point on the distribution and depending on the pass/fail decision of this point goes to 25% or 75% point on the CDF. In case of linear CDF, the 25% and 75% points also represents the 25th and 75th percentile point on VDD range. Therefore, the algorithm takes more steps searching points about the target value before reaching the target value. The actual minVDD distribution is represented by the dotted line on the plot. The adaptive search algorithm makes the searches based on distribution of actual minVDD values. For the given distribution the 25th and 75th percentile point of search will operate at 69% and 71% of the VDD range. Searching more points in the region where probability of finding target values is higher, gives lesser of number of searches and smaller VDD voltage steps per search.

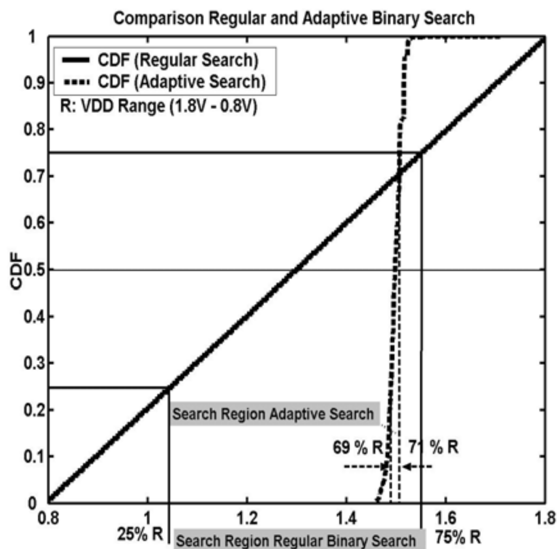

Figure 10: Search Regions for Regular and Adaptive Binary Search Algorithms

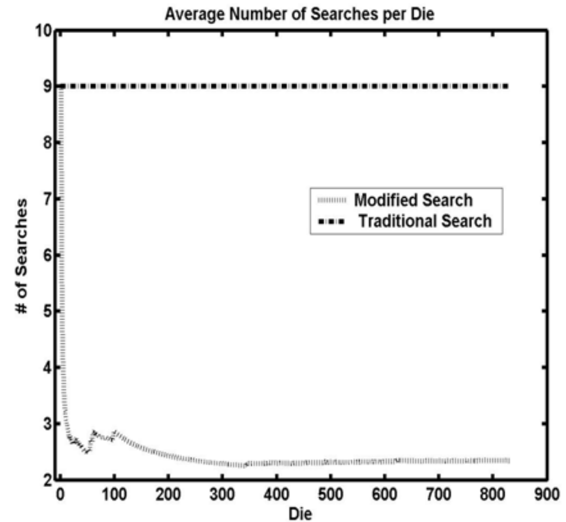

Figure 11: Average Search Loops per Die

Figure 11 shows a comparison for average number of searches per die for both the cases when the suggested adaptive search algorithm was applied on 2 wafers for 0.18µm process ASIC. From (3) for a search range of 1V and resolution 10 mV regular search takes a constant 9 searches per die. The adaptive search starts at 9 searches for the first few dies when the algorithm does not have enough values to learn the distribution. As more dies are tested, the algorithm is able to successfully estimate the expected minVDD value of the next die and the search eventually averages down to 2.5 iterations.

The results in this section show that by using the adaptive search algorithm the total search time for minVDD searches can be reduced by at least 50% of that taken by the regular binary searches. Excessive test time added by the binary searches to the minVDD and Fmax screens today prohibits their implementation in production. Adaptive approach to these searches reduces the cost overhead associated with them while promising an improved test quality.

8. Conclusions

The object of this paper is to introduce and analyze some new concepts and expand on some older ideas in the area of Adaptive Test. Override testing and first failing vector data collection and analysis from varies ASICs has shown that traditional, non-adaptive test methods vastly over-test and do not have the ability to target changing defect mechanisms. Adaptive test methods show the ability to utilize predictive data from other data sources or from shortened vectors from the same test set to significantly reduce test times and target the dominant defect mechanisms even as they change from lot-to-lot or foundry-to-foundry. Adaptive test also show large cost reduction possibilities by utilizing low cost structural

testers rather than full-functional testers based on the parametric distributions from the foundries. Adaptive outlier screens demonstrate the ability to target subtle defect mechanisms only when they occur and adaptive binary search methods have been shown to improve search time by 50% using predictive data. The combination of all these methods may only get us to around 70-80% of the ideal Optimum Test Set but this is an important and necessary step in the paradigm shift away from full testing of every IC in the production flow.

9. References

[1] W. Maly, A.Gattiker, T. Zanon, T. Vogels, R.D.Blanton, T. Storey, “Deformations of IC Structure in Test and Yield Learning” *Proceedings International Test Conference,* Oct. 2003, pp 856-865.

[2] S. Benner, O. Boroffice, "Optimal production Test Times through adaptive Test Programming," *Proceedings International Test Symposium,* Oct. 2001, pp. 908-915.

[3] W.B Jone, W.S Yeh, C. Yeh, S.R. Das, “An Adaptive Path Selection method for Delay Testing,” IEEE *Transactions on Instrumentation and Measurement,* Oct. 2001, pp 1109-1118.

[4] E.F. Cota, M. Megreiros, L. Carro, M. Lubaszewski, “A New Adaptive Analog Test and Diagnosis System,” *IEEE Transactions on Instrumentation and Measurement,* Apr. 2000, pp 223 – 227.

[5] D. Zhao, S. Upadhyaya, “Adaptive Test scheduling in SOC’s by dynamic partitioning,” *Proceeding IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* Nov. 2002 pp. 334 – 342.

[6] C.Thibeault, “On New Current Signatures and Adaptive Test Technique Combination,” *Proceedings of the VLSI Test Symposium,* Apr. 2004, pp.59-64.

[7] R. Daasch, K. Cota, J. McNames, R. Madge, “Neighbor Selection for Variance Reduction in IDDQ and Other Parametric Data,” *Proceedings of the International Test Conference,* Oct. 2001, pp. 1240-1248.

[8] M. Rehani, R. Madge, K. Cota, R. Daasch, “Statistical Post Processing at Wafersort,” *Proceedings of the VLSI Test Symposium,* Apr. 2002, pp. 69-74.

[9] R. Madge, B.H. Goh, V. Rajagopalan, C. Macchietto, R. Daasch, C. Schuermyer, C. Taylor, D. Turner, “Screening MinVDD Outliers Using Feed-Forward Voltage Testing”, *Proceedings of the International Test Conference,* Oct. 2002, pp. 673-682.

[10] A. Singh, T. Barnett, V.Nelson, “Burn-in failures and local region yield: An integrated Yield-Reliability Model” *Proceedings of the VLSI Test Symposium,* April 2001, pp 326 – 332.

[11] B. Benware, R. Madge, C. Lu, R. Daasch, “Effective Comparisons of Outlier screening Methods for Frequency Dependent Defects,” *Proceedings of the VLSI Test Symposium,* April 2003, pp 39-46.

[12] K.M. Butler, J. Saxena, “An empirical study on the effects of test type ordering on overall test efficiency,” *Proceedings of the International Test Conference,* Oct. 2000, pp. 408 – 416.

[13] A. Cabbibo, J. Conder, M. Jacobs, “Feed Forward Test Methodology Utilizing Device Identification”, to be published *Proceedings of the International Test Conference,* 2004.

[14] B. Benware, C. Lu, J. V. Slyke, P. Krishnamurthy, R. Madge, M. Keim, M. Kassab, J. Rajski “Affordable and Effective Screening of Delay Defects in ASICs using the Inline Resistance Fault Model”, to be published *Proceedings of the International Test Conference*, 2004.

[15] E. J. McCluskey, C.-W. Tseng, “Stuck-fault tests vs. actual defects”, *Proceedings of the International Test Conference*, Oct. 2000, pp.336-342.