Evaluating the Effectiveness of Detecting Delay Defects in the Slack Interval: A Simulation Study

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Abstract

A new delay testing scheme that identifies abnormal delays in the slack interval by comparing switching delays in neighboring dies on a wafer has been recently proposed and validated on experimental circuits. In this paper we evaluate the effectiveness of this new approach through the simulation of injected delay faults in the ISCAS benchmark circuits. The simulations are performed using a simple switched RC (resistor-capacitor) switching delay model. The results indicate that the new delay testing approach is orders of magnitude more effective in detecting and diagnosing smaller delay defects that increase circuit path delays by 10-50%. The new methodology can address increasing concerns that failure to detect such small delay faults during test may be the cause of significant unreliability in emerging nanometer technologies.

1. Introduction

With the rapid development of semiconductor technology, delay testing has become a critical problem. In Deep Sub-Micron technology (DSM), commonly observed failure mechanisms such as resistive opens in vias and interconnects, gate oxide punch through, etc, can all lead to excessive delays on signal paths. There is growing concern [3] that many of these small delay defects that often escape detection at test do not accelerate sufficiently in burn-in to be detected, and can cause reliability problems in the field. While traditional delay testing has primarily focused on gross delays, it is becoming clear that “smaller” delay defects, including those on short paths, cannot be ignored. Indeed, in a 6-7 level circuit, each gate, on average, contributes about 15% of the path delay. A resistive via that increases the path delay by an additional 15% is a serious defect, even though the 15% increase in delay may be well within the timing margins employed at test, allowing the defect to pass undetected. The doubling of delay at the output of some gate because of a resistive via implies (based on a simple lumped RC model) a via resistance comparable to the driving transistor resistance, typically 1-3 Kohms. Such a large resistive defect is quite likely to degrade due to metal migration and cause early life failure. Other defects, such as open gates and “tunneling” opens [9] (caused by oxide contamination of vias) can often cause very different delays depending on circuit state and input conditions. This can result in a circuit failing in the field after successfully passing test, unless the “tight” timing tests are performed to detect such faults. Thus, it is becoming increasingly important to detect and diagnose small delay defects. Such a test capability is particularly needed early in the production cycle to improve the process and ramp-up yield. Whether extensive delay testing can be carried into volume production depends on the cost effectiveness of the new techniques being developed.

The difficulty in testing for small delay defects in CMOS circuits arises from the fact that signal delays are significantly dependent on input conditions, and the internal circuit state. For example, the switching delay of a simple 3-input NAND or NOR gate can vary as much as 300% based on the input signals. Furthermore, propagation delays are impacted by crosstalk, voltage droop in the power supply grid from switching activity, partial charges on internal nodes, clock skew, etc. Sensitive delay testing requires setting up *input conditions to cause worst-case delay propagation* through the gate, or along the path being tested, to check if the output switches within the desired period. In practice, it is extremely difficult to find such absolute worst case input patterns that can ensure that “small” delay defects (10-25% of the path delay) can be detected. In fact, because of the significant variation in fabrication parameters over a production window, such worst case input patterns can even vary from lot to lot even for the same design. To allow for this parameter variation and avoid unnecessary yield loss, circuits are usually tested with 10-20% timing margins beyond the typical expected delay for critical paths. This timing margin alone already precludes the detection of many small delay defects. Recently, some statistical techniques have been proposed that can minimize the impact of timing margins in delay testing [5,6].

We have recently proposed a new delay testing method that overcomes many, if not all, of the problems in detecting small delay defects outlined above[1]. In the new Delay Detection in the Slack Interval (DDSI) approach, extra delays, including those on short paths, are observed by sampling outputs *within the nominal clock interval.* Thus, unlike the traditional delay test method, *the new approach does not require the setting up of worst-case signal propagation conditions for a fault to be detected.* As long as the fault is active along the signal path, it is detected. For a combinational circuit, this is done by observing the outputs at multiple time intervals, each progressively shorter than the nominal switching delay of the logic block. For practical scan based circuits, this translates to capturing the test responses to a delay test pattern at multiple fast clocks, each higher than the nominal operational clock rate. To normalize for parameter variations from the fabrication process, the *test results are not evaluated against any predetermined expected response, but by comparing them with those for matched neighboring circuits from the wafer that can be expected to display similar performance.* This comparison has the important additional advantage of canceling out any undesirable impact of power rail variations, noise or cross talk during test, since the neighboring circuits are tested under identical test conditions. Of course, only true fabrication defects will be detected by such a technique; common mode timing failures that are the result of design errors or fabrication parameters outside the acceptable window, will go undetected because they will affect all the circuits in a neighborhood. The basic technique is reviewed in more detail in Section 2. Experimental results [2] for small test circuits fabricated in a 0.5 micron technology have shown the significant potential of the new method; delay defects that increased path delay by as little as 5% were reliably detected.

A serious practical concern with any test methodology that detects defects by observing signals outside the normal functional environment is yield loss. The DDSI technique will identify many circuit anomalies causing small delay faults that may not necessarily cause functional failure. Furthermore, not all such defects will further degrade over time to cause reliability failures. Discarding all such circuits can lead to unacceptable yield loss. Fortunately, the DDSI technique also provides a measure of the magnitude of the extra delay due to the defect. This allows a trade-off between test sensitivity and yield loss. In practice, only those circuits (that fail only the DDSI test) displaying the largest delay defects will be discarded, while keeping the yield loss at an acceptable level. This is akin to what is done in practice with IDDQ tests, where failing current thresholds are set to ensure that the *additional* yield loss from IDDQ only fails is in an acceptable range (typically 1-2%). Of course, the sensitivity of the DDSI test can increased as needed to assist with diagnosis during process ramp-up, and to ensure product quality early in production (at the cost of additional yield loss) before the process is mature.

In this paper we evaluate the effectiveness of this new DDSI approach for testing and diagnosing delay defects of various sizes, and compare the results against those for the traditional delay test technique where test responses are captured at the nominal clock time. The study is performed through timing simulation of injected delay faults in the ISCAS benchmark circuits. The test sets comprise of a collection of two-pattern test vectors. Fault coverage for the two schemes over a range to injected delay fault sizes is evaluated. Our simulator employs a simple switched RC (resistor-capacitor) switching delay model for fast circuit timing simulation.

The rest of the paper is organized as follows. Section 2 reviews the DDSI technique. Section 3 provides an overview of the simulation program. Simulation results are presented and discussed in Section 4. We conclude in Section 5.

2. Review of the Proposed Delay Test Method

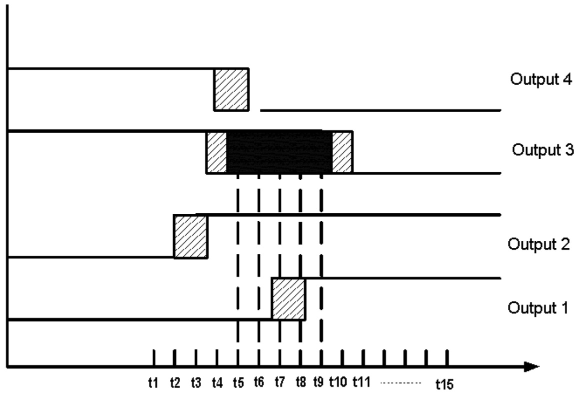

Figure 1: Detecting Delay Faults in the Slack Interval Using Multiple Higher Frequency Clocks

Figure 1 illustrates the basic DDSI technique. The figure shows switching transitions at multiple outputs of a circuit under test (CUT) resulting from the application of a two pattern delay test <v1, v2>. The hashed area about each transition represents the possible variation in the exact timing of the switching transition compared with its “expected” value. The dark area shows some extra delay on one signal line because of a delay fault. As proposed in [1], we compare switching delays in corresponding signals between the CUT and a matched known good die that is physically located adjacent to the CUT on the wafer at manufacture. Because the electrical parameters of components in local regions of a wafer track quite closely, the variation in switching delays for the same signals on adjacent dies is expected to be small (1-3% for the experiments reported in [2]). In contrast, this variation for two random die from diverse production lots and wafers can be much higher. Now suppose the difference in switching delay for any two signals *between two neighboring matched good die* is observed to be *less than* Δd for a production lot. Then if we sample the output signals at incremental intervals of time Δt during the test, for a given signal, the difference in the observed switching delays between two good circuits cannot be more than $\Delta d + \Delta t$. In other words, if the faster circuit switches in some interval starting t_n, a defect free slower circuit is still expected to switch during the test interval that occurs at time Δd later. A greater switching delay indicates a delay fault. Thus a delay fault, such as the one shown on Output 3 in Figure 1, can be detected by capturing and observing the circuit response at multiple capture intervals, each shorter than nominal switching delay for the logic block. (Observe that the magnitude of the extra delay can be estimated by counting the number of additional sampling intervals before the defective output switches.) In scan based designs, this can be achieved by capturing and analyzing the test responses to the same delay test pattern at multiple clock frequencies, each higher than the nominal clock rate. It is shown in [2] that if the sampling rate is kept sufficiently high, any hazards on the output signal lines can be correctly identified, and will not invalidate the test.

It is important to note here that the delay test scheme employing multiple clocks recently presented in [6], is fundamentally different from our DDSI approach. In [6] the fast clocks are only used to screen out potentially defective chips; all fail/pass decisions are made in a subsequent confirmation phase using the operational clock frequency. In our DDSI approach, test results captured by the fast clocks are used to make pass/fail decisions based on delays comparisons with results from matched neighboring die.

3. Simulation of benchmark circuits

Simulation of the ISCAS benchmark circuits to evaluate the effectiveness of the DDSI approach involves three major steps: fault free circuit representation, fault injection, and timing simulation. Delay faults of varying sizes are injected one at a time at each circuit node for a delay test vector pair <V1, V2>. Signal propagation delays to the primary outputs are then evaluated through timing simulation. The fault free circuit delays are also simulated to allow the detection of extra delays on signal lines though comparison. Based on the observed output switching delays, a decision is made whether each delay fault is detected by the DDSI approach and the traditional delay test approach. A fault is detected by the DDSI approach (which can observe the switching time for signals in the slack interval by repeated sampling) if any output in the faulty circuit experiences a delay larger than the expected inter-die timing variation (typically taken to be 5%). On the other hand, the fault is detected by traditional delay testing only if is causes some signal to be delayed beyond the expected clock period. The clock period is chosen to be the critical path delay plus an appropriate timing margin.

Our circuit timing simulator is based on simple switched resistor-capacitor (RC) models as described below. The objective is to capture input dependent CMOS timing details missed by gate level simulation, without the computational expense of full SPICE simulation. Since the simulation generates continuous analog values, and both the fault free circuit, and the circuit with the injected delay faults are simulated and compared to decide if a fault is detected, inaccuracies in time and scale common to both simulations will not cause any serious errors in the statistical evaluation of fault coverage for this study.

3.1 Models for circuit representation and simulation

As mentioned above, resistor-capacitor (RC) approximations were used to model circuit gates. Figure 2 shows the RC model for a 2-input NAND gate. Four resistors represent the transistors, with Rpx, Rpy (PMOS effective channel resistances) in parallel comprising the pull up P-network, and Rnx, Rny (NMOS effective channel resistances) in series making up the NMOS pull down network. The capacitor CL represents the total effective capacitive load at the gate output. Inputs X and Y control the states of the switches.

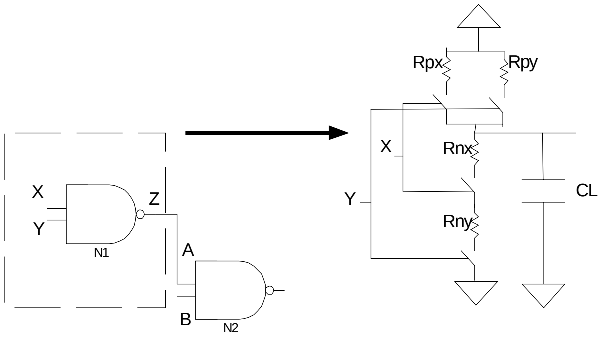

Figure 2: NAND gate RC model

We assume a standard cell design approach. Thus the effective channel resistance for all NMOS (and similarly PMOS), transistors is taken to be the same value. The small intra-die variation in these values is ignored; more detailed analysis shows that the effect of this variation can be accounted for in the inter-die parameter variation, and does not significantly impact the results. In our simulation, the values of Rp, the PMOS channel resistance, and Rn, the NMOS channel resistance, were chosen to be 10K and 5K ohms respectively. Note that this is an arbitrary choice. Changing the values only scales the resulting simulated timing by a constant factor and does not affect the fault coverage results. However, because the routing between standard cells usually results in significant variations in the interconnect capacitance, the capacitive load CL at each gate output is generated based on a random statistical distribution. A normal distribution with a mean value at 0.1pF and standard deviation of 0.025pF was used. This capacitance was further multiplied by the fan-out factor, if any, to account for the extra capacitance arising from multiple loads.

Similar RC models are constructed for NOR gates. AND, OR, BUFFER and XOR/XNOR gates in the benchmark circuits were implemented from a combination of NAND and/or NOR gates. Although those “composite” gates are not primitive, they were treated as indivisible elements in our simulations. Delay faults were only simulated at the inputs and outputs of these composite gates.

3.2 CMOS timing simulation

Figure 3 shows the timing analysis of a 2-input NAND gate using the RC models. The signal transition (rising or falling) time is defined to be the time for completion of 90% of the voltage swing. Rising and falling transition times are indicated as T_{rise} and T_{fall} in figure 3(a). Note that ideal switches used in gate models are turned on/off in the middle of the transition of the input signals. The time difference between the middle points of output transition and input transition is defined as the gate delay for that input event.

Notice in figure 3(b) that the inputs to NAND gate have different slopes and start to transit at different times. This corresponds to the situation that transistors are turned on/off at slightly different times. To simplify the simulation, the multiple switches are all activated at the same time when multiple input transitions overlap within their 10% - 90% switching window. Else each transition is treated as individual event. The effective transition time of multiple input transitions is chosen to be the earliest input transition time.

The 90% output fall time in figure 3 (a) is given by:

$$T_{fall} = RC\ln\left(\frac{V_{DD}-V_{n-1}}{V_{DD}-V_{n-2}}\right)$$

where $R=2R_n$, C=CL, $V_{n-2}-V_{n-1}=90\%*V_{DD}$, VDD is the power supply voltage. If the power supply voltage is 5V, and the signal is low when it is less than 0.5V, then the 90% falling transition time T_{fall}=RCln((0-5)/(0-0.5))=RCln(10). If R=5Kohm, C=0.1pF, then the fall time T_{fall}=10Kohm*0.1pF*ln(10)=2.3 ns. Figure 3 (b) shows another case with the output transiting from low to high. The 90% rise time can be calculated using the equation above to be T_{rise}=RCln(5-0/5-4.5)=RCln(10)=1.15 ns. Note that R=Rp/2, which is the effective resistance of two parallel PMOS resistors. Recall that the effective gate delay is the time difference between the two middle points of the output and input transitions. The gate delay is RCln(2)=0.69 ns.

A complete combinational circuit can be modeled by linking the RC models defined by circuit netlist. For a test vector pair <V1, V2> applied to the primary inputs

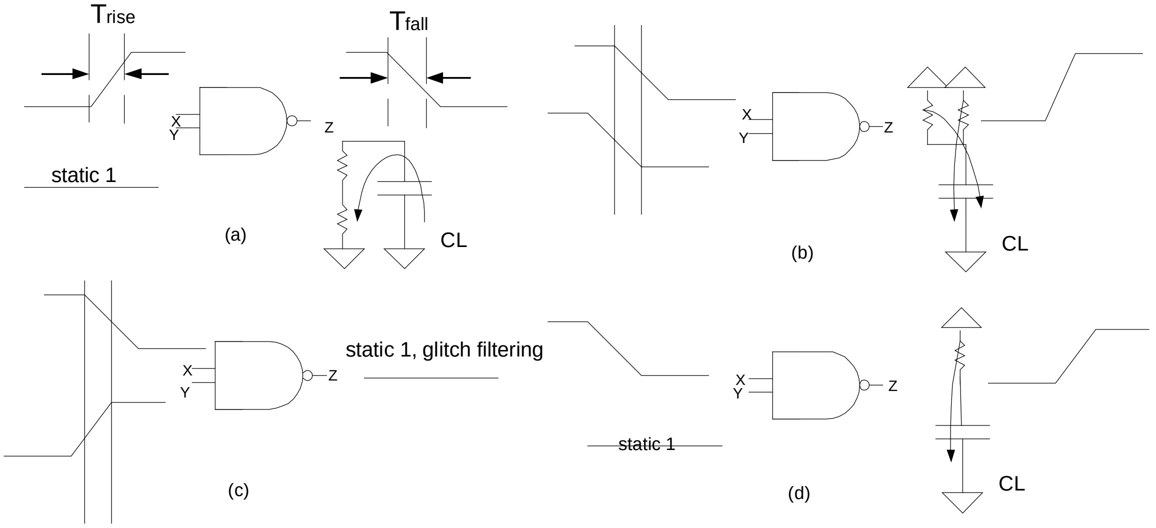

Figure 3: NAND gate delay analysis

of the circuit, we simulate the transient responses of each gate starting from the input to the primary outputs. For every gate, the output transitions are simulated and the rise/fall times as well as the starting points for all the transitions are recorded. The gate outputs serve as the inputs of the succeeding gates, and the simulation process goes on until the primary output is reached. In this way, a simple transient simulation is accomplished by only recording the “critical” timing points without detailed information, such as shape of the waveforms.

3.3 Fault list, Fault Injection, and Fault Coverage

Delay faults of different sizes are injected in the simulations as extra timing delays on rising and falling transitions on each circuit node. The delay fault size is measured as a fraction (percentage) of the critical path delay, which is also the (most aggressive possible) clock period for that circuit. Rising and falling delay faults are considered individually since some defects (such as a resistive via in the pull up network) may affect only the rising (or falling) transition, while other defects such as bridges can affect both transitions, although not necessarily by the same value of increased delay. Thus, the total fault list for a circuit is of size 2N, where N is the number of circuit nodes. The delay fault coverage for a given delay fault size is the percentage of these 2N delay faults that are detected by the test set.

3.4 The Simulation Procedure

To perform the simulation, the RC model of the benchmark circuits is first constructed. The MatLab program is used to generate random load capacitance values based on a normal distribution as described earlier. These random node capacitances are used with the estimated transistor channel resistance values to construct the electrical model of the benchmark circuit. The critical path delay ($T_{critical}$) for the circuit is then extracted by simulating the fault-free circuit for a large number of <V1, V2> patterns; the maximum observed output transition time was taken to be $T_{critical.}$ The nominal operation clock period (T_{clk}) is then taken to be the critical path delay plus an appropriate timing margin T_{margin} (for example an extra 15% of the $T_{critical}$). For each vector pair in the test set, timing delays to the circuit outputs are then simulated with and without injected delay faults at each node. Based on the observed output switching delays, a decision is made on whether each injected delay fault is detected by the DDSI approach and the traditional delay test approach. A fault is detected by the DDSI approach (which can observe the switching time for signals in the slack interval by repeated sampling) if any output in the faulty circuit experiences a delay larger than the expected inter-die timing variation (typically taken to be 5%). On the other hand, the fault is detected by traditional delay testing only if is causes some signal to be delayed beyond the expected clock period. The process is repeated for all vector pairs in the test set to obtain the delay fault coverage of the test.

4. Simulation Results:

This Section presents simulation results for delay fault coverage for the new DDSI approach and traditional delay testing for ISCAS benchmark circuits for a transition delay fault test set. Recall that the delay fault size is measured as a fraction of the critical path delay. Rising and falling delay faults are handled individually; the total fault list for a circuit is of size 2N, where N is the number of circuit nodes. The delay fault coverage for a given delay fault size is the percentage of these 2N delay faults that are detected by the test set. For each benchmark circuit, the transition delay fault test set was generated based on a combination of fault simulation and targeted test generation.

4.1 Fault Coverage for Small Delays

Figures 4, 5 and 6 show simulation results for delay fault coverage versus delay fault size for a selection of the ISCAS85, and ISCAS89 benchmark circuits. Five plots are shown in each graph to compare the effectiveness of the new DDSI approach, which detects delays in the slack interval, with the traditional delay testing approach, where delays are only observed at the end of the clock period. The plot for the DDSI test assumes an intra die timing variation (between matched neighboring die on the wafer) of 5%. This is more pessimistic than the 2-3% variation observed in our experiments presented in [2], but is expected to be typical for larger circuits. Our simulations show that even if this neighboring die timing variation increases to a quite pessimistic 10%, the results do not change significantly. The plots for traditional delay testing include a range of timing margins. These margins are typically added to the expected critical path delay for a circuit in determining the nominal clock period. This is to allow for parameter variations over the production lot, and minimize yield loss from somewhat slower but defect free circuits being declared faulty. This timing margin, however, reduces the effectiveness of the traditional test approach in detecting small delay faults. Indeed, delays less than the timing margin cannot be detected. Figures 4-6 shows defect coverage for the traditional delay test method with 10% and 20% timing margins. While such margins are typical (even optimistic) in practice, we also plot coverage for an idealized 0+% timing margin (Fmax) to show the best case possible with the traditional delay test approach. Finally, the plots also show the classical transition fault coverage for the circuits, which is the best possible delay test coverage attainable for any test set, since it assumes an infinite delay from the delay fault. Observe that all the plots converge to this transition fault coverage value as delay size increases to cover an entire clock period.

It is readily apparent from the plots in Figures 4-6, that the new DDSI delay detection approach is significantly

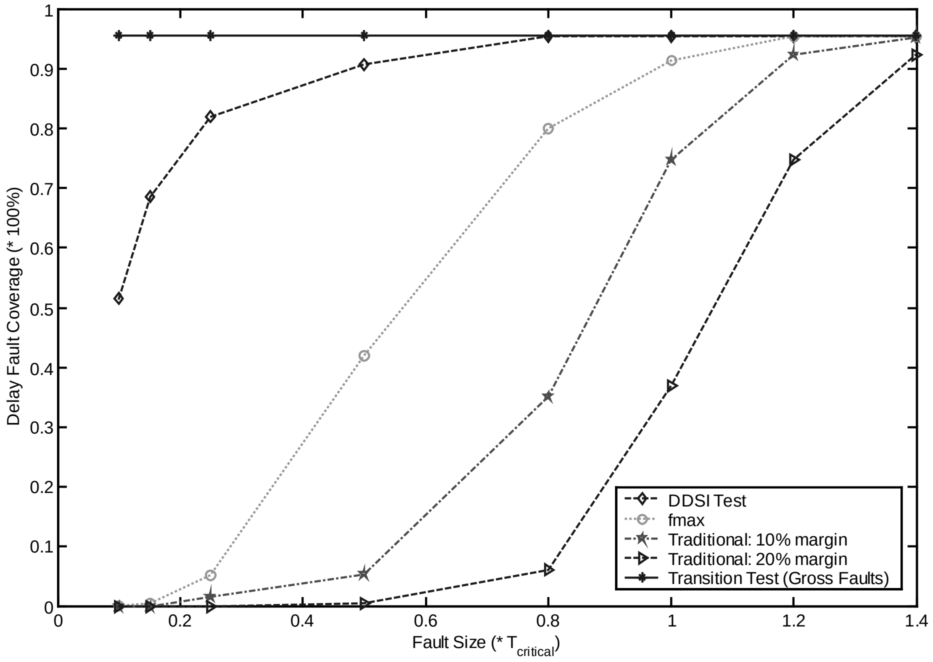

Figure 4: C6288

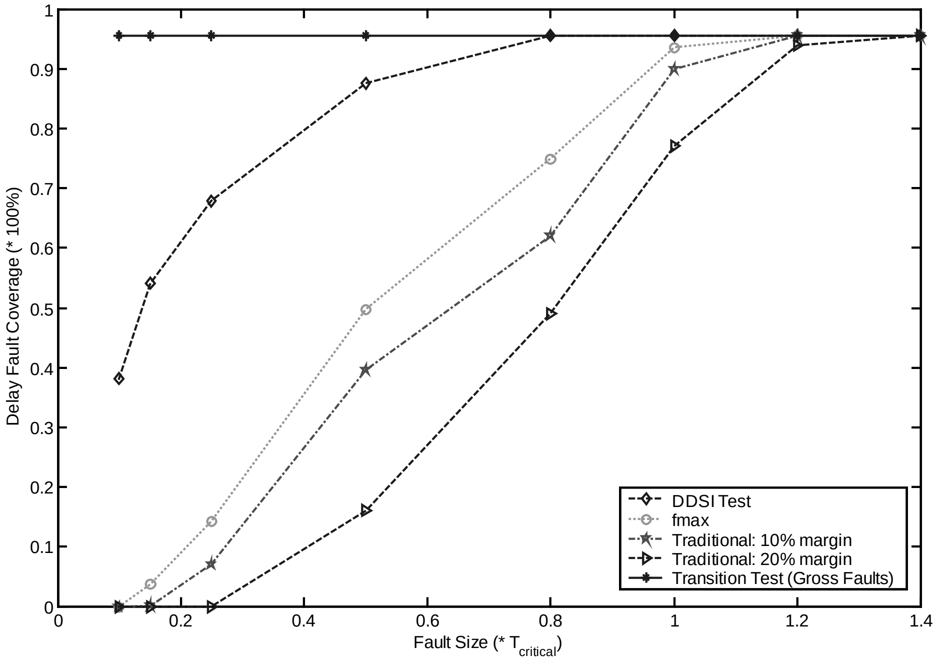

Figure 5: C7552

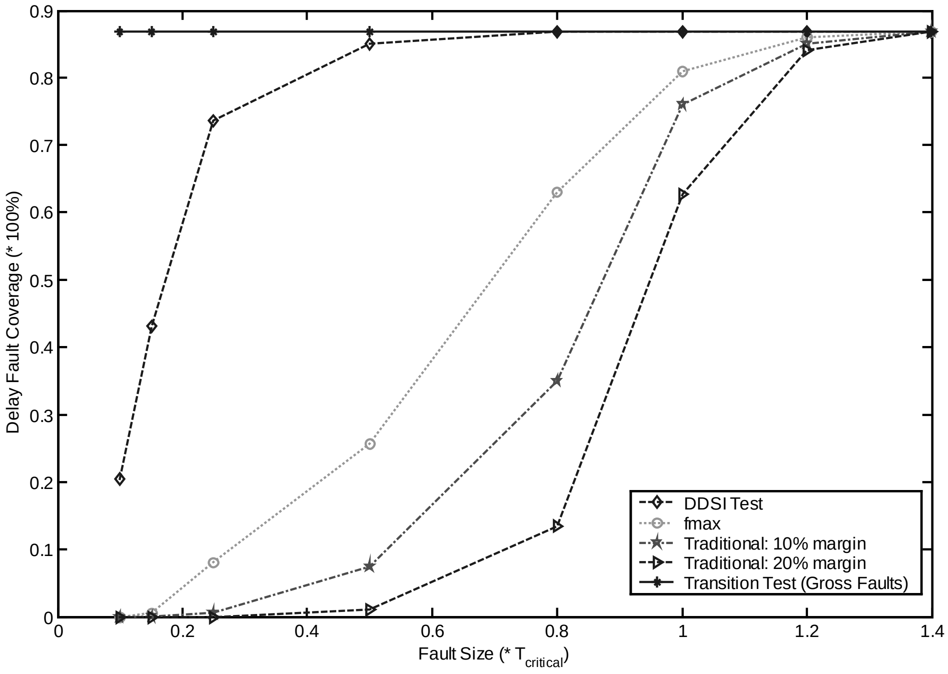

Figure 6: S38584.1

more effective in detecting faults smaller than 50% of the critical path delay than the traditional delay approach. For defects 10-20% of the critical path, the improvement is an order of magnitude, or greater; indeed the traditional approach is virtually ineffective in detecting small delay defects. We have already argued earlier that such defects, equivalent to an additional gate delay, cannot be ignored by testing in DSM technologies.

Observe that the traditional delay testing method does somewhat better for small faults in the C7552 benchmark, Figure 5. This is because propagation paths for C7552 are better balanced with a many delays close to the critical path delay. Thus, extra delays of 20-40% on any path are more likely to be detected, especially if captured by a clock with only a small margin over the critical path delay. However, even so, the DDSI scheme has significantly higher coverage for small defect sizes.

More complete simulation results for the ISCAS85 benchmark circuits are presented in Table 1. The table shows delay coverage results for defect sizes of 10%, 15% and 25% (of the critical path delay). The results indicate that, for a defect size of 25%, the new DDSI approach exceeds an 80% delay coverage for most circuits, while coverage for the traditional method (with an optimistic 10% timing margin) is generally less that 10%.

ISCAS85 Circuit	Size of Fault List/ Size of Test Set	Delay Fault Size (% of $T_{critical}$)	DDSI Test Coverage	Traditional Delay Test Coverage		Transition Test Coverage
				0+% Timing margin	10% Timing margin	
C432	864/27	10%	43.4%	0.7%	0	99.2%
		15%	78.7%	8.8%	0.4%	
		25%	83.7%	13.7%	7.4%	
C499	998/68	10%	55.7%	1.3%	0.1%	99.5%
		15%	77.2%	7.4%	1.6%	
		25%	85.1%	28.6%	6.3%	
C880	1760/47	10%	41.5%	0.6%	0	98.7%
		15%	75.4%	1.5%	0.6%	
		25%	83.0%	16.3%	1.6%	
C1355	2710/60	10%	53.8%	1.9%	0	96.6%
		15%	81.7%	8.0%	2.0%	
		25%	87.3%	10.1%	8.1%	
C1908	3816/35	10%	35.0%	5.1%	0	97.1%
		15%	79.6%	18.1%	4.9%	
		25%	86.4%	35.6%	18.2%	
C2670	5340/38	10%	34.3%	0.4%	0.1%	95.1%
		15%	77.4%	4.2%	0.5%	
		25%	85.3%	26.9%	5.0%	
C3540	7080/37	10%	39.2%	0.2%	0	96.0%
		15%	78.3%	1.7%	0.3%	
		25%	93.1%	11.1%	1.8%	
C5315	10630/18	10%	38.5%	0.1%	0	96.8%
		15%	70.3%	0.9%	0.1%	
		25%	84.7%	2.7%	1.8%	
C6288	12576/21	10%	51.6%	0.1%	0	95.3%
		15%	68.6%	0.4%	0	
		25%	81.9%	5.1%	1.6%	
C7552	15104/19	10%	38.2%	0	0	95.6%
		15%	54.0%	3.7%	0.1%	
		25%	67.8%	14.3%	6.9%	

Table 1: Simulation Results for the ISCAS 85 Circuits

4.2 Scan Based Delay Testing

One of the important possibilities for the new DDSI test approach is application to scan based delay testing. Table 2 presents some results for the two methods employing a launch-on-shift scan test approach. To be consistent with the launch-on-shift test methodology, the first vector of the test vector pair was picked randomly, while the second vector was a "one-shift" of the first vector. This structural limitation on the choice of the second vector is known to significantly limit the effectiveness of delay tests in a scan environment.

Observe from Table 2 that traditional delay testing with a 10% timing margin achieves minimal coverage of timing defects of size 25% or less, while the new DDSI approach does much better. For a 25% delay defect size, the DDSI test coverage is, on average, only 15% less than the best possible transition fault coverage. This clearly indicates the potential of using DDSI in scan based delay testing targeting relatively small delay defects, which cannot be detected using traditional test methods. Another significant concern in scan based delay tests in noise and power induced variations on circuit timing, since conditions at test can differ greatly

ISCAS89 Full Scan	Size of Fault List/ Size of Test Set	Delay Fault Size (% of $T_{critical}$)	DDSI Test Coverage	Traditional Delay Test Coverage		Transition Test Coverage
				0+% Timing margin	10% Timing margin	
S13207.1	26414/67	10%	45.7%	0.2%	0	85.1%
		15%	53.3%	2.8%	0.3%	
		25%	76.0%	14.3%	2.6%	
S15850.1	31700/53	10%	43.9%	0	0	92.5%
		15%	56.3%	6.7%	0.1%	
		25%	68.5%	21.2%	6.5%	
S35932	71864/66	10%	25.2%	0.1%	0	84.5%
		15%	41.3%	0.9%	0.1%	
		25%	54.7%	12.6%	1%	
S38584.1	77168/197	10%	20.4%	0	0	86.8%
		15%	43.2%	0.5%	0.1%	
		25%	73.6%	8.1%	0.5%	
S38417	76834/158	10%	37.1%	0	0	91.4%
		15%	54.6%	0.2%	0	
		25%	70.4%	5.4%	0.2%	

Table 2: Launch-on-shift simulation results for ISCAS 89 Circuits

from operation [11]. Fortunately, these variations do not impact the DDSI scheme since circuit timing delays are evaluated relative to a matched neighboring circuit that is tested under identical conditions.

4.3 Diagnosis

An early adoption application for the DDSI approach is projected to be delay defect diagnosis for process improvement during yield ramp-up. Test costs are the major concern in adopting new test methods; these are somewhat less critical for diagnosis, which is an extremely difficult problem and must take advantage of all known test techniques.

Effective delay defect diagnosis (location) requires (i) high fault coverage, (ii) that the defect be detected by as many different test vector pairs as possible, and (iii), for a test that detects the fault, the fault should be detected at as many circuit outputs as possible. While a comprehensive diagnosis methodology based on the DDSI technique is under development and will be the subject of subsequent work, in Table 3 we present some early results on the potential of the proposed method based on these measures that support delay fault diagnosis. It is clear from the table that the new approach is likely to be much more effective in supporting diagnosis of delay defects in DSM circuits. In addition to high fault coverage and the multiple detection of most faults, the ability of the DDSI technique to observe delays within the slack, allows the effect of a delay fault to be observed at multiple outputs, including the short paths. This makes it much easier to trace back to the source of the extra delay.

Ckt	C432		C880		C1355		C1908	
	DDSI	Traditional	DDSI	Traditional	DDSI	Traditional	DDSI	Traditional
# Faults detected	717	65	1406	24	2159	219	3281	687
Average # Detecting Vectors per Fault	115	16	119	8	102	7	160	5
Average # outputs fault is observed	3.6	1.2	9.0	1.1	13.4	1.0	10.2	1.5

Table 3: Test results for 1000 vector pairs with fault size of 25% critical path delay.

5. Conclusion:

The simulation study presented here convincingly establishes the significant potential of the new DDSI delay testing approach in detecting delay faults down to a size that is virtually undetected by the traditional defect testing approach. We have also shown the potential of its application to scan based delay testing. We expect this new approach to be initially employed to assist with the difficult problem of diagnosing delay faults for process improvement early in production. Future research is focused on a pilot study of this technique on volume production circuits. This will help us better address the cost and implementation issues that need to be resolved before the methodology can find widespread application in industry.

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