

Systematic Defects in Deep Sub-Micron Technologies

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Abstract

Defects due to process-design interaction have a systematic nature. Therefore they can have a profound impact on yield. The capability to detect (and correct) them is a requirement to continue to follow Moore's law. Most of the systematic defects are detected during the process development. These defects are detectable with test structures or visual inspection tools. However some process marginalities will only show-up in the topology of 'real' designs. Moreover, these defects are often not detectable with stuck-at testing. We show two examples of process related defects which could only be detected with more advanced test methods such as transition fault testing and low voltage testing. To correct systematic problems, however, one should not only have the capability to detect defects but also to identify them. Our examples show that other tests would have been far more sensitive in detecting systematic issues. Therefore the detection of systematic defects gives new requirements to test suites and can only be achieved with a shift in the position of manufacturing test.

1 Introduction

The three main reasons for digital circuits to move to the next technology node are performance, power and cost (area, yield). It was taken for granted that all these aspects improve if one moves to the next node. It meant that the same design would become cheaper, faster and more power efficient. However, these reasons are not that obvious anymore for the coming nodes. The performance improvement is not something one can take for granted anymore since interconnect delay becomes more dominant [1]. The same holds for the power efficiency. DSM technologies are increasingly more leaky and it is predicted that stand-by power and active power consumption become comparable [2]. So two out of three reasons to go to the next technology node are already threatened. Moreover, also the yield improvement is not that obvious anymore. For random defects a size distribution is predicted which scales as:

$$\frac{D}{D_0} = \left(\frac{CD}{CD_0} \right)^{-n}, \quad (\text{EQ 1})$$

with D/D_0 the ratio of the defect densities, (CD/CD_0) the ratio of the critical dimensions and n a number between 2 and 3 [3][4]. So by reducing the critical dimension we become more sensitive for smaller defects, however, a smaller critical dimension also means that the same logic function can be implemented in a smaller area. This reduction in area more than compensates the increased sensitivity for defects. Therefore, the move to the next technology nodes gave an improvement in yield. This assumption is, however, only valid for random defects (often particle related defects). This is not true anymore if systematic or feature-related defects become dominant. These systematic defects cause an additional yield loss. So if we cannot get systematic yield loss under control then we will lose one of the major drivers of Moore's law.

Additionally to the systematic yield loss one could argue that new technologies will introduce new defect types. One of the panels at ITC'00 [5] discussed these new defect mechanisms and what kind of test methods are required to detect them. The general agreement seemed to be that we will see all the problems we used to see and that there is no magical new test method to catch all the problems. In our experience this is indeed true. In deep sub-micron technologies we see shorts due to particles, silicidation problems, open vias, etc. like we used to see in pre-DSM technologies. Of course shifts in importance of specific defect types can and will occur, however, the basic test methods that we have, e.g. stuck-at testing, transition-fault testing, current-based testing and testing under different conditions, are sufficient to detect these faults. This seems true for both random defects as well as for systematic defects. The big difference between the two defect classes is that systematic problems can be very topology specific and can have very specific defect characteristics. Therefore a small test coverage deficiency for random defects can result in a giant loop hole for systematic defects. This makes it important to have a good defect coverage to ensure the quality level. Furthermore, it is important to identify and solve systematic yield loss for economical reasons. Often only small adjustments in the processing are required to resolve them. Therefore it is important to have the proper set of tests and tools which

enable us to identify these systematic defects.

We will show in this paper two examples of systematic defects which are missed by test structures and could only be detected in a real designs. The defects were detected with existing test methods such as low voltage testing and delay-fault testing but other test methods would have been more efficient in identify the defects as a systematic issue. The capability to detect and identify systematic defects becomes a key requirement for the economical use of deep sub-micron technologies and will require a shift in the use and purpose of manufacturing test.

The remainder of this paper is organised as follows. Section 2 investigates the characteristics of systematic defects and its relation with design for manufacturability. In Sections 3 and 4 two cases of process related defects are described. Section 5 describes the lessons learned with respect to testing in DSM technologies. How this affects the position of test is investigated in Section 6. The paper is concluded in Section 7.

2 DfM and systematic defects

Nowadays, one of the first associations with design for manufacturability (DfM) is often the use of additional tricks to make a design resistive against random defects and thereby improve the manufacturability. Examples of these techniques are via doubling or wire spreading. The most important rule, however, for design for manufacturability is to comply to the design rules to avoid systematic faults. These design rules are prescribed by the process developers/engineers to ensure a high manufacturability of layout features. During the process development phase, dedicated test structures, such as via chains, comb structures, dense lines etc., are used to check this.

A misconception of designers is often that as long as they follow the design rules the manufacturability of their design is ensured. This is of course not the case. Likewise it is not true that if a design rule is violated with a small amount this always results in an incorrect structure. For each design rule there is a probability distribution as function of the design parameter, e.g. the clearance to the next structure, that predicts if the feature ends up correctly on silicon or not. So even for structures that obey the design rules there is a (very) small chance that something bad happens during the processing. This applies to both old and new technologies. The big difference between the two is that the processing in advanced technologies becomes more complex and that therefore structures have to comply to more rules. For example, the metal density per area was not very important before the introduction of chemical mechanical polishing (CMP) in the manufacturing flow. With the introduction of CMP a minimum metal density became a necessity in order to avoid dishing. This

led to the introduction of artificial tiles to comply to the design rule. To make life even more complicated the latest technologies do not only require a minimum density but also a maximum density. As a result large metal regions, e.g. pads, should have slots.

The metal density constraints are just one of the examples of how rules evolve over process generations. Each of the new process steps in DSM processes introduces additional design rules. As a consequence a single structure has to comply to several rules nowadays. Such a structure should have a high manufacturability on a per rule basis but could have a poor manufacturability if one would consider all the rules together. These kinds of issues are missed by the dedicated test structures because these only check for a few design rules at a time. This is especially true for random logic in which the environment of a structure is not well determined (in contrast to memory elements for example). The only way to check for these issues is to 'test' standard cells and real designs for systematic faults.

Another aspect of process related problems is that they can cause defects with very specific characteristics. For example, let us assume a process problem that causes metal stringers. This creates shorts of which the resistance depends on the stringer's length and cross section. The typical length is often related to the critical dimension of that technology while the cross section depends on the process issue and can be quite small. Therefore these stringers often have a high resistance. If this resistance is above the critical resistance for the detection with stuck-at testing, one needs another method to catch them (e.g. IDDQ testing or very-low voltage testing) [6][7][8].

So, in conclusion, the more complex processing indicates that systematic faults become more important which requires more effort to identify and solve them. The two main properties in which systematic faults distinguish themselves from random defects are the topology dependency and specific defect characteristics. In the next sections, we describe two cases of process related defects to highlight these aspects.

3 Case 1: salicidation problem in 0.13 μm

Our first example is a problem that showed up in a yield ramp-up vehicle processed in a 0.13 μm technology. This yield ramp-up vehicle contains among others DSP-like cores, designed in a static standard gate library. The first indication for the problem was the large number of delay-faults with respect to 'stuck-at' faults in these cores. This difference could not be explained by the defect distribution as determined by test structures. Fault localisation was performed with the aid of the program *Faloc* which is part of the Philips' test tools. *Faloc* identified flip-flops in the majority of the cases as the location

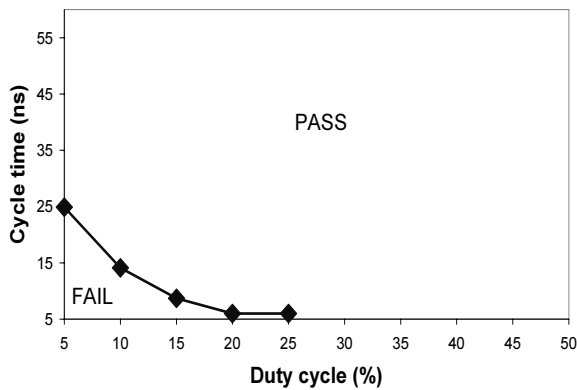


Fig. 1: Pass/fail boundary (Shmoo plot) of the scan continuity test as a function of the duty cycle of the clock and the clock period for a good IC.

of the fault. This was unexpected. Delay faults often indicate the presence of open vias, however, if it was just a problem with the vias one would expect that it is picked up by the via chain test structures. Furthermore, one would not expect that only the flip-flop is affected. This all pointed to a process problem in the flip-flop.

The next stage was to perform failure analysis and determine the root-cause. Unfortunately localisation only to the gate level of a flip-flop is seldom sufficient for failure analysis. The flip-flops belong to the largest and most complex standard gates. It is a hard task to find a subtle process problem just by grinding and cutting the flip-flop. Additional information, which pin-points the location within the flip-flop, strongly improves the success rate of failure analysis. Therefore more thorough measurements were performed. These additional experiments showed that the fault is not only detectable with a delay-fault test but also in a fast scan continuity test (flush test). The typical pattern used in a scan continuity test within Philips is 00010111 embedded in zeros. Above a certain speed we only observe zeros in defective ICs.

To further investigate the problem we made Shmoo plots. Shmoo plots [9][10] belong to the most powerful tools to obtain additional information about the defect behaviour. This information helps to understand and thereby localise the defect. For this particular case we made a Shmoo plot in which the cycle time and the duty cycle are varied. Figure 1 shows the result for a good IC. The Shmoo plot shows fails in the lower left-hand corner. This is as expected since short duty cycles in combination with a short cycle time make the total clock high period too short for this design. The minimum clock high pulse is given by the pass-fail boundary and we observed that below an externally applied clock high signal of 1 ns all scan chains start to fail simultaneously.

Figure 2 shows the results for a bad IC. As expected

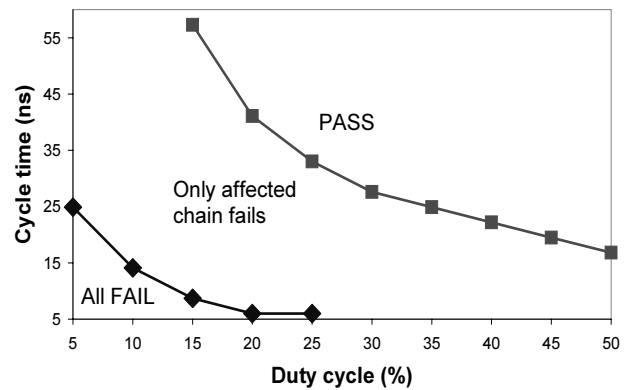


Fig. 2: Pass/fail boundaries of the scan continuity test as a function of the duty cycle of the clock and the clock period for a bad IC. In the region between 'pass' and 'all fail' only the chain with a defect fails.

the majority of the chains fail only in the lower right-hand side corner as was the case for the good IC. However, additionally the scan chain with the defective flip-flop fails much sooner. For this defective flip-flop a clock-high period of 8 ns is required (this time is of course defect dependent).

Delay-faults in static CMOS circuits are most often associated with an increased resistance. Typical examples of defects that cause this increase in resistance are incompletely filled vias or mouse bites in interconnects. Due to the increased resistance a transition takes more time to propagate. The impact of a resistive defect in general only depends on the cycle time and is independent of the duty cycle of the clock. In Figure 2 this would show itself as a horizontal pass/fail border, this is clearly not the case for this defect type. Apparently the defect causes the flip-flop to require a longer clock high period. Since this condition is also not fulfilled in the delay-fault test the IC failed this test although it is not a classic delay-fault.

The next step would be to look at the layout of the flip-flop and find the most likely spots that can cause the observed problems or perform a complete inductive fault analysis [11]. In both cases the defects are modelled in the netlist and the defect behaviour is simulated. If the simulated behaviour matches the observed behaviour it becomes a candidate to look at with failure analysis. In this case we can obtain even more information about the electrical response of the flip-flop. This yield ramp-up vehicle has as an advantage over normal chips that it contains 'observation pillars' for each flip-flop. This observation pillar connects the output of the flip-flop via a via-stack to a small pad on top. This pad can be observed with an e-beam. This allows us to measure the response of the output of the flip-flop. In principle this information is also obtainable for chips without these observation pillars but this would require circuit modifications with the aid

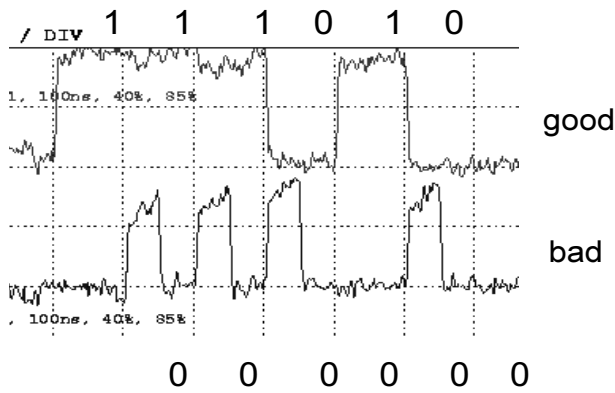


Fig. 3: Response of the output of the flip-flop measured with an e-beam. For a good flip-flop and a bad flip-flop. (Horizontal divisions are half V_{DD} steps, vertical divisions one clock period).

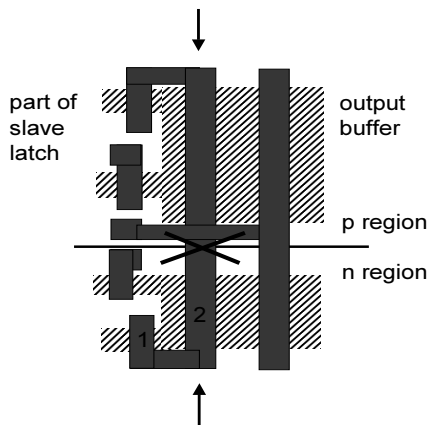


Fig. 4: Schematic layout of a part of the slave latch and the output buffer of the affected latch. Filled areas mark poly gates while the hatched areas mark active. The cross is the suspect location of the open that disconnects the gates of transistors 1 and 2.

of a focused ion-beam. In these modification an additional pad is created and connected to a signal wire stemming from the flip-flop. Although this is in principle possible, it is certainly not an easy task in modern technologies with 6-9 layers of metal.

Figure 3 shows the measured response with the e-beam for a good and a bad flip-flop. The applied pattern is a scan continuity pattern. The clock period is 100 ns and represented by one division in Figure 3 while the duty cycle for these experiments was 45%. The top picture shows the response of a good flip-flop which matches with the expected response. The bottom figure shows the measured response of the next flip-flop in the chain which was identified as defective. Expected was the same response but shifted for one clock period. The observed response is very different. Although one sees a response we also see

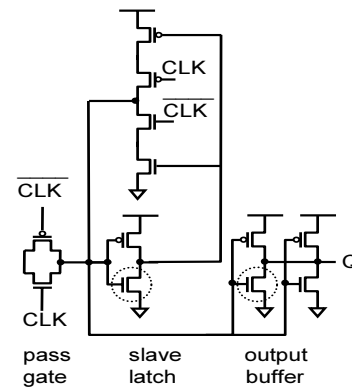


Fig. 5: Schematics of the pass-gate, slave latch and output buffer of the affected gate. The encircled transistors are the affected transistors 1 and 2 of Figure 3.

that when the clock becomes low this output drops to zero indicating that the data is not latched in the slave. As a result only zeros are observed. A single response can be separated in two parts. It starts with a very fast initial response which rises the output signal within a few nanoseconds to a level above $V_{DD}/2$ followed by a slower second part that takes tens of ns to rise the output to V_{DD} if the clocks becomes low before this reaches V_{DD} level the data is lost and the output drops to zero as is shown in Figure 3.

Inspection of the layout of the flip-flop gave several candidates for the defect location. The slow response of the output points in the direction of the output buffer of the flip-flop. Figure 4 shows this part of layout (slave latch and output buffer). One of the candidates is marked with a cross. The reason this location was a suspect is because poly tracks parallel to the p-n boundary were known to be susceptible for manufacturing issues. An additional interesting feature of this defect is that a single defect affects two transistors (marked 1 and 2 in Figure 4). This makes the defect behaviour more complex. Transistor 2 is part of a parallel output driver. This defect affects the driver strength of the drivers and therefore can cause additional delays. However, this is not the root-cause why the scan continuity test cannot run at the expected speed. The output is still driven by the second part of the parallel output driver and the delay owing to the defective transistor 2 is small. It is the combination of transistor 1 and 2 that causes the fast scan continuity to fail. The increased resistance makes the response to rising pulses of this transistor slower. Therefore it requires more time to latch the data in the slave. If this time is not provided and the clock becomes low too soon then the data is not stored. This effect is what is causing the fast continuity test to fail. When we introduce this defect in our defect simulation we get exactly the expected behaviour. If one

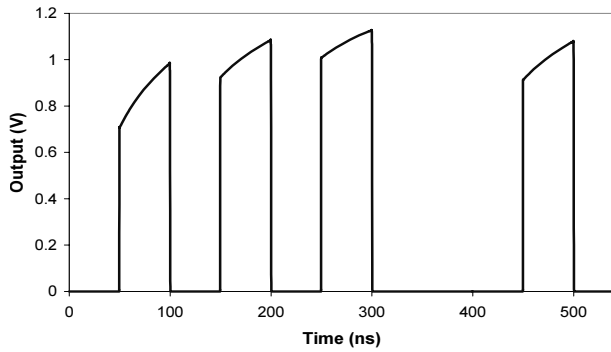


Fig. 6: Simulated response of a defective flip-flop.

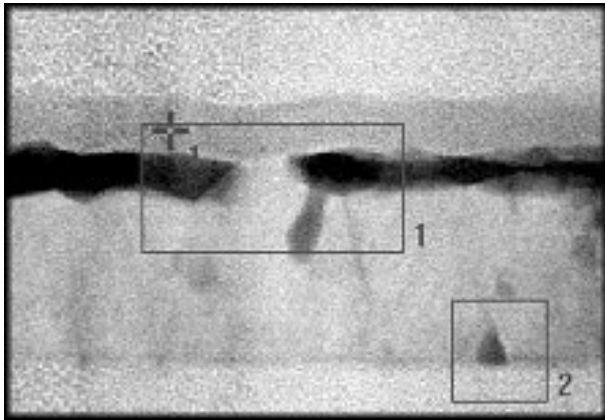


Fig. 7: Cross section of the affected poly track. The dark area region is the salicidation and the area enclosed with 1 is the open defect.

compares figures 3 and 6 one sees a fast initial response followed by a slower second part. Furthermore, if the clock becomes low too soon, the output drops to zero. Moreover, we see that for a series of ones the initial response becomes stronger (0.7, 0.9, 1.0 V for the first three 1's in Figure 6). The same kind of behaviour is observed in the e-beam measurements. Other suspect locations could result in the defect behaviour as observed with the tester but they do not match the behaviour as observed with the e-beam. This made this location our top suspected. Failure analysis confirmed this. Figure 7 shows a cross section along the line marked with the arrows in Figure 4. The dark region in the image is the salicidation. This should run undisrupted from the left to right. For bad transistors this is not the case. In the centre a spot is not salicidated (box 1 in Figure 7). This confirmed our identification. An en-route improvement of the salicidation module solved this issue.

4 Case 2: high-resistive shorts in 0.16 μm

Our second example are high-resistive shorts en-

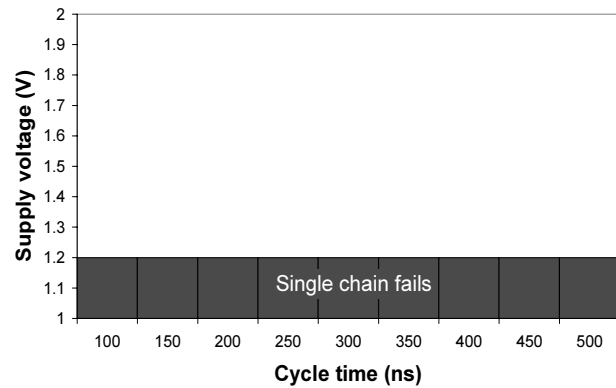


Fig. 9: Shmoo plot of the scan continuity test for a bad IC.

countered in a 0.16 μm technology (nominal supply voltage 1.8 V). The defect is not observable with the common visual defect inspection tools. Furthermore, their high-resistance makes their impact easy to miss with test structures. As a result this process marginality was initially missed. The first indication of a problem was an increased number of stuck-at fails at a reduced supply voltage. A reduced supply voltage makes tests more sensitive for shorts [7][8]. So in itself it is not strange that ICs pass at the nominal voltage but fail at a reduced voltage. However in this case the fraction was too high and therefore a more thorough investigation was initiated.

To localise the problem the fault localisation program *Faloc* was used. In general this program is very successful (as for example in the case of the salicidation issue described in the previous section), however, in this case the results did not make sense. Instead of a single location a large number of flip-flops was marked as suspects. Furthermore, these suspects were not consistent for different fail vectors. This points in the direction of a more structural problem and additional experiments were performed. These experiments quickly pointed out that a scan continuity test at a reduced supply voltage is capable to detect the problem. Instead of the expected 00010111 pattern faulty chips gave a 00111111 response. Therefore we called the problem the 6-ones problem. The faulty responses are only observed below a critical voltage, $V_{DD,fail}$.

For low frequencies good ICs pass the scan continuity and stuck-at test for supply voltages below 1.0 V. For the bad ICs one scan chain fails the scan continuity test at higher supply voltages. Figure 9 shows an example of a Shmoo-plot of a scan continuity test for a bad IC. For this IC the affected scan chain failed at 1.2 V. Typical this $V_{DD,fail}$ voltage of affected ICs is 1.0 to 1.5 V. The fact that the scan continuity test failed under very specific

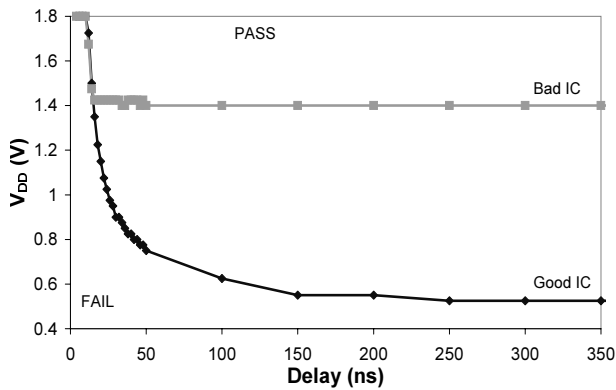


Fig. 10: Another example of a Shmoo plot of defect-free IC (black line) and one with a short (grey line). The lines mark the pass-fail boundary. (After [8])

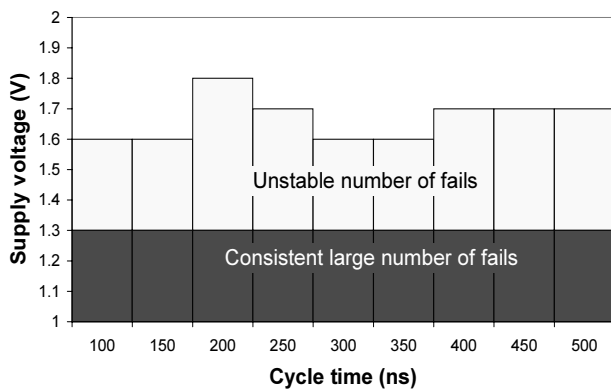


Fig. 11: Shmoo plot of the stuck-at test for the bad IC of Figure 9.

conditions and with very distinguished characteristics points again in the direction of a process problem in the flip-flops.

The behaviour in Figure 9 is typically for a short in a static CMOS technology; the short causes a fail below a specific supply voltage and its impact is independent of the cycle time. Figure 10 shows another example of this behaviour for a different design [8]. A good chip passes even for supply voltages below 0.6 V as long as the cycle time is adjusted. The bad chip starts to fail below 1.4 V and its fail behaviour becomes independent of the cycle time. Above $V_{DD,fail}$ the bad chip performs as a defect-free device as is shown by the identical pass/fail borders in the left-hand side of the figure. The specific value of $V_{DD,fail}$ depends on the driver strength of the involved transistors and the resistance of the short.

The kind of behaviour in Figure 10 is the same as we see in the Shmoo plot of the scan continuity test in Figure 9: defect-free behaviour if $V_{DD} > V_{DD,fail}$ while always

failing for $V_{DD} < V_{DD,fail}$. On forehand one would expect the same behaviour for the stuck-at test, however, this is not the case. Figure 11 shows that we have two different fail regions for the stuck-at test. In the dark gray region we always have a large number of fails. This fail voltage is close to $V_{DD,fail}$ of the scan continuity test. This is as expected since if we cannot scan in the correct stimuli then the test will always fail. However, there is also a second region with a supply above $V_{DD,fail}$ in which the IC sometimes fails. The number of fails is small compared to the number of fails in the first region and not (completely) reproducible.

Apparently even above $V_{DD,fail}$ it is not ensured that we shift in the correct values. This can be explained with a voltage drop due to the increased activity. It is well known that scan patterns can create an activity in a circuit which is factors larger than the activity in functional mode. The power network is designed for the activity in the application and not for the activity during scan. This results in a larger IR drop than during functional mode. In a static CMOS design this is in general not a problem and a reduction of the cycle time is sufficient to handle this power drop. Therefore stuck-at testing via scan chains is often performed at a cycle time below the operational frequency of the IC. However, an exception that cannot handle this power drop, is a defective flip-flop. The local activity in the neighbourhood of the defective flip-flop causes a power drop. $V_{DD,local}$ becomes smaller than $V_{DD,fail}$ and incorrect data is shifted in (0's become 1's). When the local activity is reduced, for example due to the series of ones instead of the stream of 0 and 1, $V_{DD,local}$ rises again and the flip-flop functions properly again. Apparently we can have power drops of upto 0.5 V during scan-in (note that the amount of power drop also depends on the test setup which in this case accounts for part of the IR drop). The smaller drop explains the behaviour in Figure 11, if V_{DD} is below $V_{DD,fail}$ the scan chain malfunctions and we always get a fail; in the region $V_{DD,fail}$ to $V_{DD,fail} + 0.5$ one has unstable behaviour and above $V_{DD,fail} + 0.5$ V we have defect-free behaviour. Furthermore, it explains the strange results obtained with *Faloc*. Partially incorrect data is shifted in and the locations where this data ends up at the normal cycle are marked as suspects.

Before we can start failure analysis we have to localise the affected flip-flop. A simple way to achieve this is:

- scan-in data at the nominal supply voltage
- reduce the supply voltage below $V_{DD,fail}$ at shift cycle #
- continue with shifting and observe the result.

The shift cycle at which the supply voltage is reduced is modified based on the previous result. If the test passed then, # should become smaller, if # failed it should be-

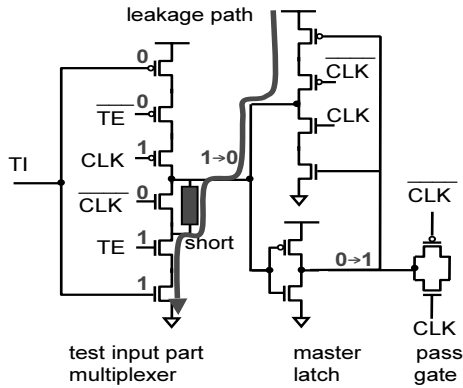


Fig. 12: Schematics of the flip-flop's (TI multiplexer, master latch and pass gate). The short creates a leakage path which can flip the master latch.

come larger. With a binary search the affected flip-flop is localised within a small number of iteration cycles.

Although the localisation of the affected gate is simple, it is not sufficient to find the root cause. Again it is required to pinpoint the exact location within the flip-flop. In the affected fab the yield vehicle with observation pillars was not used and therefore a direct observation of the behaviour of the faulty flip-flops was not possible. So we had to rely on the layout and schematics to find a defect type and location that explains the observed behaviour. The defect behaviour indicates resistive shorts. This already limits the number of options, however, it still leaves a large number of potential suspects. An important breakthrough was the realisation that to activate the defect, the clock edge itself was not important but only the fact that during the clock high period the supply voltage dropped below $V_{DD, fail}$. This limited the suspects to the multiplexer stage of the scan flip-flop. The schematics of the multiplexer stage is shown in Figure 12. The top suspect is the

resistance	1.8V	1.6V	1.4V	1.2V
15k Ω	fail	fail	fail	fail
20k Ω	pass	fail	fail	fail
25k Ω	pass	pass	fail	fail
50k Ω	pass	pass	pass	pass

Table 1: Simulation results for several resistance - supply voltage combinations.

transistor, which is controlled by CLK_bar . If a short exists to ground or between source and drain then a leakage path exists that can flip the content of the slave node. This location is marked in Figure 12 with a grey box and labelled 'short'. The figure shows a simplified schematics of the master latch of a scan-able flip-flop. Only the con-

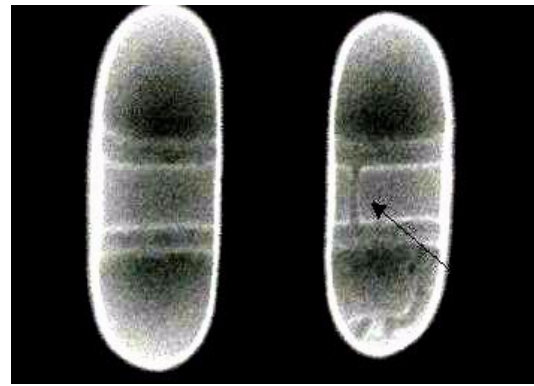


Fig. 13: Micrograph of a good (left hand-side) and an affected (right hand-side) transistor. The arrow points to a small discoloration which is the resistive source-drain short.

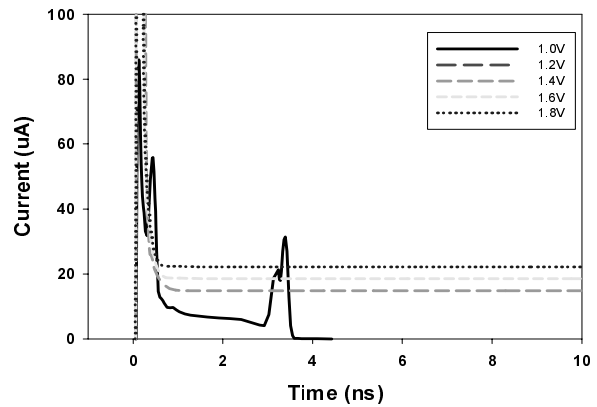


Fig. 14: Simulated I_{DD} behaviour for the flip-flop with a 50 k Ω defect for four supply voltages.

ditions during test are shown but a similar configuration exists for *Data in*. If the supply voltage drops below a critical value the driver strength of the master latch is not sufficient anymore to retain its value. Once it flips it remains in this state. This data is propagated and results in the 6-ones signature. The critical voltage depends on the resistance of the short. Table 1 shows results of the defect simulations. The typical fail range of 1.0 to 1.5 V matches a defect range of 20 to 50 k Ω . Once identified failure analysis had again an easy job to find the root-cause. The defect is visible in Figure 13 as a small discoloration between the source and drain area. Again an adjustment of the processing removed the problem.

This process problem was not only detectable with low voltage testing but also with current-based testing. The leakage path shown in Figure 12 caused an increase in the number of small I_{DDQ} anomalies. An advantage of the use of $(\Delta)I_{DDQ}$ testing is that it is more sensitive than low voltage testing and can detect smaller anomalies. The

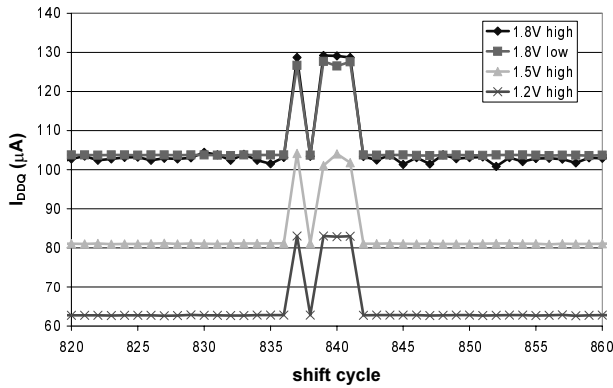


Fig. 15: Measured I_{DDQ} as function of the shift cycle for a 10111 scan continuity pattern and different conditions. The four activations indicate a ‘normal’ defect.

best we could detect in this case with low voltage testing were $V_{DD,fail}$ voltages of 1.0V (or 50 k Ω defects, see Table 1). Delta I_{DDQ} testing was capable of detecting even smaller anomalies of hundreds of k Ω s. An interesting characteristic of this defect is that I_{DDQ} testing can only detect it for supply voltages above $V_{DD,fail}$. Figure 14 shows the result of the defect simulation for current-based testing. In this figure the I_{DD} current is plotted as function of time for several supply voltages. The introduced defect in the simulation is a 50 k Ω short. The fail voltage for this short is 1.0 V. For supplies above 1.0 V an increased I_{DDQ} current of 20 μ A is observed while 0 μ A is expected for defect-free ICs. If we reduce the supply voltage to 1.0 V a different kind of behaviour is observed. After the transient peak at 0 ns we have an elevated I_{DD} level for about 3 ns. After this period the master latch flips and we have a second transient peak. After this second transient there is no additional current flowing anymore. So above $V_{DD,fail}$ the defect is detectable with a static current-based (I_{DDQ}) test. Below $V_{DD,fail}$ no static current is flowing and a dynamic current-based test or I_{DDT} test is required.

The predicted defect behaviour is indeed observed. Figures 15 and 16 show experimental data for I_{DDQ} testing. The I_{DDQ} measurements were performed during scanning-in of the scan continuity pattern to get a selective response of the affected flip-flops. For most cycles no (additional) defects are activated by the 10111 sequence. The two exceptions are the anomalies at cycle 837 and 2655. The first anomaly is a normal ‘short’ somewhere in the cone controlled by the flip-flop. For each of the four 1’s the defect is activated. The defect is active independent of the clock signal (low, high) or the supply voltage (1.2, 1.5 or 1.8V). So this is just a common resistive short and therefore not very interesting. The second anomaly is related to the resistive source-drain short in the flip-flop. Only two vectors activate the defect. These are the 01

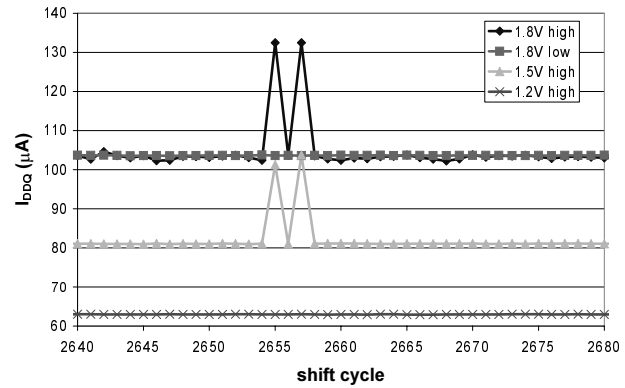


Fig. 16: Measured I_{DDQ} as function of the shift cycle for a 10111 scan continuity pattern and different conditions. The two activations match the behaviour of the source-drain defect in the flip-flop.

parts in the 010111 scan continuity pattern. Furthermore, the defect is not active when the clock signal is low or if we reduce the supply voltage to less than $V_{DD,fail}$ (1.3 V for this IC). In Figure 16 we see that under these conditions the I_{DDQ} anomalies disappear. This is in perfect agreement with the expected behaviour and confirmed the defect localisation.

5 Lessons learned

The two examples in the previous sections were selected to highlight several aspects of testing deep sub-micron technologies which we will address in this section.

5.1 Test structures versus real designs

The two process problems examined in the previous two sections were missed by the process evaluation test structures and could only be detected in a real design. This certainly does not mean that real designs are preferred above dedicated test structures to find systematic defects. These dedicated test structures are used during the process development to evaluate the processing and most of the process related problems are picked up by these structures. Typically they give a very clear signal, which is easy to interpret and therefore results in a fast feed-back to the process engineers. Moreover, the employed set of test structures are continuously refined based on previously encountered problems. Furthermore, the fact that the test structures can be made correctly ensures that the encountered problems are usually simple to solve once identified (as indeed turned out to be the case in our two examples). Although test structures can cover all aspects of very regular structures (such as memories) it is virtual impossible to create test structures that cover all aspects of random logic. Therefore the fact that process evaluation structures do not pick-up a specific problem does not mean that they cannot occur if the topology is

slightly different. This happened for the salicidation issue; only the layout as used in the flip-flop gave a problem while several types of salicidation test structures processed fine. The only way to identify systematic problems is carefully analyse the test results of designs that used the routing tools and which are based on the standard cells. For this reason Philips uses, in its 350 to 90 nm technologies, yield learning vehicles that contains modules that represent real designs.

5.2 Test methods for systematic yield loss

A relevant question is if one needs any special test methods for systematic yield loss. The examples illustrated that this is in general not the case. Defects caused by process-design interactions have open-like or short-like behaviour. This is the same kind of behaviour as we see for random defects. So the existing set of test methods, such as transition fault testing, stuck-at testing, low voltage testing and current-based testing, should be sufficient. The two examples confirm this. Although both could not be detected with stuck-at testing at the nominal supply voltage, they could be detected with either delay-fault testing or low voltage testing.

Although we could detect both defects it is clear that our test suite was not perfect in both cases for the identification of systematic defects. It was no problem detecting the defects with delay-fault testing or low voltage testing but they could have been detected with a more aggressive scan continuity test for very little additional test cost. Aggressive means in this case that a test is not only performed within the specification window but should cover all the corners in which an IC can function. In the first case a faster scan continuity test could detect the problem while in the second case a lower supply voltage during the scan continuity test was sufficient. This aggressive scan continuity test would directly point to the flip-flops as the main source of the problem and, far more important, a smaller defect signal can be detected if one combines it with a normal scan continuity test and compares the results. Especially the capability to detect small yield anomalies will become important to fight systematic defects.

5.3 Static CMOS designs

There is one additional lesson related to static CMOS designs which we want to highlight. The two examples were not only chosen because they show some of the aspects of process problems/systematic yield loss but also because in both cases the flip-flops were affected. In static CMOS designs flip-flops take a special place. Static CMOS is not only very robust against all kinds of disturbances, such as ground bounce, but is also fairly insensitive for resistive shorts. This is in contrast to dynamic CMOS designs in which these resistive shorts can result

in delays. This robustness of static CMOS is an advantage since one only needs to detect these resistive shorts from a yield improvement or a reliability point of view. In dynamic CMOS designs one needs to detect the resistive shorts from a performance point of view but also to detect defects with even larger resistances if one wants to ensure the reliability of the chips.

Static CMOS designs, however, do have a weak spot in the form of the flip-flops. Flip-flops belong to the more complex gates and are dynamic elements. If a defect affects the flip-flop then this robustness is not ensured anymore. On the one hand one could solve this by adding DfT [12]. On the other hand one could solve this by applying better tests. This on its own justifies more attention to improve the scan continuity test. Part of this improvement within Philips is the use of additional scan continuity patterns but with different data backgrounds. For example, a 01 background increases the activity and therefore enhances the detectability in second case study. Moreover, the scan continuity patterns should all fail for the same IC. If this is not the case for a substantial number of ICs then something strange is going on that justifies a more thorough investigation.

6 Position of testing for DSM technologies

The capability to identify systematic defects also means a shift in the position of testing. If one looks at the chain: fab-test-product-customer, manufacturing test had as purpose to minimise the cost down-stream. Testing was only about determining if a chip is good or bad and we were willing to spend this money on testing because we knew that replacing bad ICs in PCBs or products is far more costly. Test gets additional requirements, however, if testing has also to provide feed-back to the process engineers to correct systematic defects. It is not sufficient to tell which ICs are bad and good but it should also tell if the defect is systematic in nature. This is of course not possible on basis of a single event and requires a statistical analysis. The simplest and very common method is to compare the observed yield with the expected yield. This method is only suited to detect large yield anomalies. In future technologies it is likely that yield becomes affected by multiple systematic defects. Each of these defects can have a small impact on their own but combined they can have a profound impact on yield. The detection of small yield anomalies, however, requires more sophisticated methods. Statistical defect localisation [13] is one of these methods. In this method, fail-vector information is used to localise all defects in the layout. If one applies this method to a large sample base then one gets a distribution, which marks the high risk areas. If these areas do not match with those of a yield simulator then it is time to start a more thorough investigation.

For advanced yield analysis it is not sufficient anymore to have only pass/fail information. Methods, such as the statistical defect localisation require additional information. The test results should allow us to classify defects. This means a shift in the kind of information testing should produce. It also introduces new aspects in the cost analysis for test. For example, one single test which is cheap and detects all defects is ideal for removing bad ICs. However, this test is not very helpful for providing feed-back to the yield/process engineers since they have only one metric to compare the yield to. Therefore multiple tests, which could even be partially redundant can be more cost economical for the total product chain than this single test. Examples are: additional stuck-at tests above the commonly applied two or three tests at minimum, maximum and nominal supply voltage and the introduction of additional scan continuity patterns. Especially for the first designs in a new technology this effort is worthwhile.

7 Conclusions

The increasing complexity for new technology nodes makes it more likely that we get systematic defects. Process evaluation structures alone are not full-proof and our two examples show that feed-back based on real designs is required to find systematic problems. If one is not capable to detect and remove these systematic defects, Moore's law is endangered.

The increased importance to detect systematic defects also means a shift in the purpose of manufacturing test. Instead of just providing pass/fail information to optimise cost down-stream it should also provide feed-back upstream for yield improvement. This last feature is possible because our experience learns that once identified and accepted by both test and yield engineers the problem is usually easy to correct. One of main capability of test for yield improvement should be to be able to identify yield anomalies. This extension of the purpose of manufacturing test does often not require sophisticated new test methods but only the implementation of slightly modified tests as was the case in the two examples.

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