On-Chip Mixed-Signal Test Structures Re-Used For Board Test

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Abstract

Analogue clusters on boards are traditionally tested in mass production using a Bed-of-Nails, often combined with functional system tests. In general this approach requires additional board area to create test access, is not very flexible and is hard to re-use. On-chip methods provide a solution to overcome these drawbacks and are already widely used in the form of Boundary Scan for digital interconnections. For analogue interconnections also on-chip solutions are available. We analysed the coverage and application of two on-chip methods, IEEE Std 1149.4 and the re-usage of existing Design-for-Testability for on-chip Mixed-Signal blocks. It was found that a reduction board test costs as well as test development time can be achieved by using, or rather re-using on-chip alternatives.

1. Introduction

Consumer products such as television sets or DVD recorders still contain a large number of analogue clusters on the assembled Printed Circuit Boards (PCB). Most of these clusters consist of 5 to 20 components. Typical functions are filtering, level adjustments or ESD protection, often used between connector pins and analogue IC pins. For consumer products these clusters are normally tested using a Bed-of-Nails (BoN) in combination with a functional test of the system. Both the BoN and the functional test methods have their drawbacks. In the case of the BoN it requires the addition of test-lands to the PCB and it can not be adjusted easily to new product designs. As an example, the PCB in Figure 1 shows the impact of the large number of test lands on the board area. Functional tests are generally hard to generate with sufficient and known coverage and suffer from poor diagnostic capabilities.

To decrease test costs we want to reduce the number of these test-lands and improve the re-usability of the tests. At the same time we want to maintain the diagnostic capabilities, at least to the level of one cluster.

To achieve this it is needed to have a test access through the ICs to the analogue IC pins that are connected to the analogue clusters. Figure 1 shows a concept with two Mixed-Signal ICs that are accessed through an 1149.1 Test Access Port (TAP) [1]. This TAP can also be the 1149.4 ATAP [2]. The first IC is used to generate a stimulus to an analogue cluster. The second IC is used to capture the output signal of an analogue cluster.

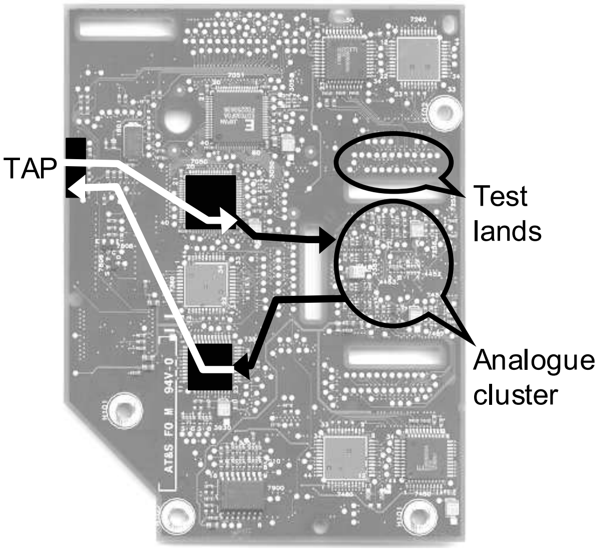

Figure 1: Analogue clusters accessed trough a TAP

An implementation of 1149.4 requires analogue Design-for-Testability (DfT), which involves additional silicon area and analogue design effort. For consumer products the additional costs and efforts so far have been too high to justify implementation of 1149.4.

A new alternative becomes available with the wider usage of core-based testing on ICs. On-chip core-based testing, like P1500 [4], can also provide test access to Mixed-Signal cores. This DfT will primarily be added for IC testing, but allows re-use for board level tests if it provides serial access to the Mixed-Signal cores [5][6][7]. In Figure 2, two Mixed-Signal ICs are shown where the Digital-to-Analogue Converter (DAC) and Analogue-to-Digital Converter (ADC) are both accessed using scan chains controlled by a TAP.

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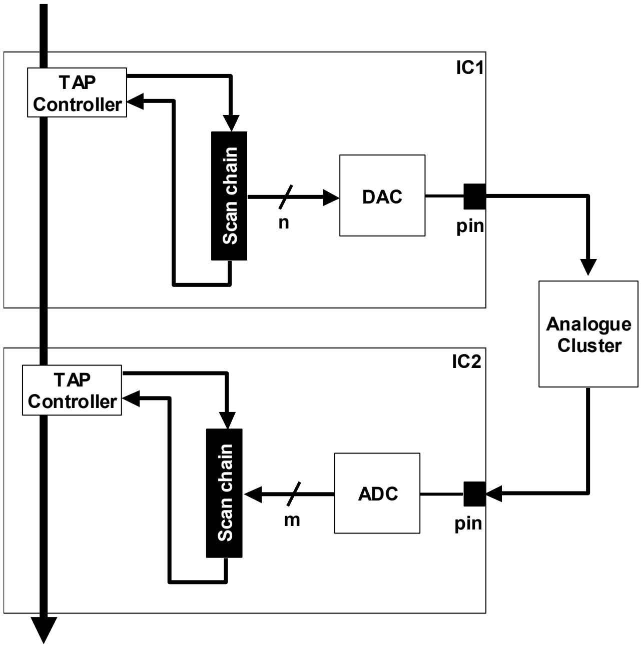


Figure 2: Scan chains provide test access to an analogue cluster

The advantages of this alternative are that it provides test access through the 1149.1 TAP and requires no or very limited additional DfT for board test. In this paper we compare the 1149.4 and on-chip Mixed-Signal DfT (MS DfT) alternatives for PCB production testing of analogue clusters. Before the explanation of the on-chip DfT techniques we describe the analysis we did to find the types of signals that need to be applied and analysed.

This paper is organized as follows: prior work is discussed in Chapter 2. In Chapter 3 the requirements to test signals are analysed using fault simulations. In chapters 4 and 5 the 1149.4 and MS DfT alternatives and their limitations are described. A comparison between the two alternatives and existing test methods is given in Chapter 7. Chapter 8 contains the conclusions.

2. Prior work

A number of publications have addressed test-land minimization or limited access testing. One of the issues is the detection and diagnostic limitation due to device tolerances. In [8] a limited access test method, targeted at using 1149.4 is described, also under presence of device tolerances. It aims at achieving best diagnostic capabilities by selecting the best nodes for measurements. In [9] a method is presented to optimise tests with limited access. This is applied to clusters without active components and can be used with multiple nodes for measurements. The clusters that are subject of this paper have active components as well.

Various publications on 1149.4 describe the features and specifications of IC implementations [11][12] and describe component characterization [10] or advanced on-chip test methods based on 1149.4 [13].

Apart from 1149.1 or 1149.4 also extensions with special cells have been proposed, targeting at detection of interconnection defects [14][15][16][17]. Implementation of these solutions generally adds less costs compared to a 1149.4 solution, but are not standardized and target a specific connection test. They are less suitable to test the interconnections of the analogue clusters analysed in this paper.

3. Type of signals to apply

Before the different methods can be compared, we first determine the type of signals and signal analyses that need to be applied to cover the targeted faults. To do that we analysed the analogue clusters found on a modern high-end television board using statistical and fault simulations. The board contains 93 analogue clusters. Most clusters are found between an IC pin and a connector. The component count per cluster varies approximately from 5 to 20 components. For three of these clusters statistical and fault simulations have been done with an in-house Spice-like simulator. The simulation results have been verified on hardware for the cluster we named cluster #1, depicted in Figure 3.

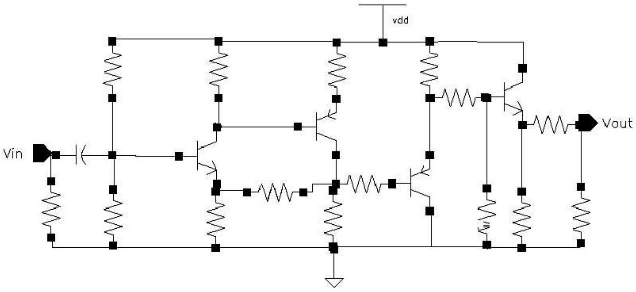


Figure 3: Analogue cluster #1

For the statistical analysis we used a Monte-Carlo simulation with a spread of 10% on the resistors and 20% on the capacitors. Spreads on the transistors have been taken into account, but did not contribute significantly to the total spread. For an AC analysis of cluster #1 the Monte-Carlo results are shown in Figure 4. The AC analysis shows the functional frequency area of approximately 10 kHz to 10 MHz.

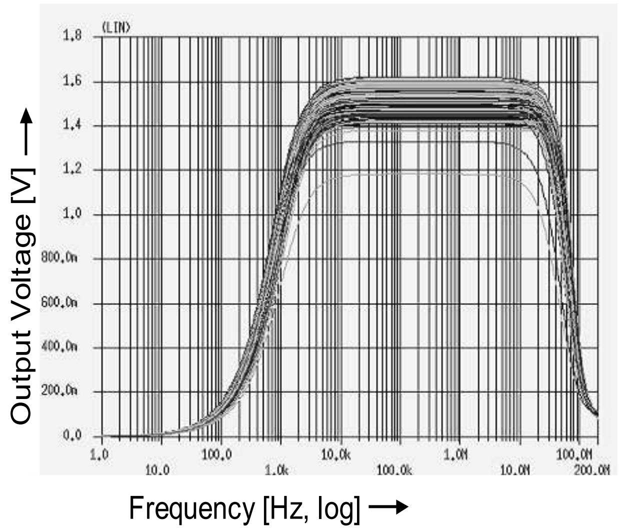


Figure 4: AC Monte-Carlo analysis of cluster #1

The standard deviation (sigma), obtained from the Monte-Carlo simulations, is used to define the upper and lower limits of the production test:

- Upper limit = Nominal value + 3*sigma + 10mV
- Lower limit = Nominal value - 3*sigma - 10mV

The value of 10 mV has been used to account for measurement inaccuracies. Note that the Monte-Carlo analyses are done to find limits that are needed to analyse the applicability of test signals; actual spread on components and measurement inaccuracies might be different in products. This will not result in different test signals.

To create a fault-list for the fault simulations, the netlist of the nominal circuit is taken. The fault-list contains opens on all component pins and shorts between all nodes in the cluster. To simulate an open we insert a resistor of 1 MΩ between the component pin and the original net. For the shorts we connect a value of 1 Ω between two nets. This results in a fault-list containing 120 faults for cluster #1. All faulty netlists have been simulated, using various test stimuli. To determine if the simulated faults can be detected by the evaluated test signal, the resulting simulation values are compared against the upper and lower limits found with the statistical simulations. For test signals we used voltage stimuli and measured the resulting voltage levels. Evaluated stimuli are DC levels, single-tone sine waves of various frequencies, multi-tones and frequency sweeps. For the measurement we used analyses like peak-peak voltage level, Total Harmonic Distortion (THD) and Signal/Noise Ratio (SNR). Current stimuli and analyses have not been used, because for the MS DfT method the signals will need to be applied and measured through the functional DAC and ADC, which are also voltage-based.

For the three clusters it was found that the measured peak-peak voltage from a single frequency in the functional frequency domain provides a coverage of 67 to 86% of the simulated faults. Higher frequencies are less suitable since the higher spread in output voltage at those frequencies results in wider limits. Lower frequencies are either blocked by a capacitor or also have large spread in output levels. With other signals or analyses it was very hard to increase the coverage. An interesting case is the Total Harmonic Distortion (THD). Simulations showed that the THD is usable to detect four additional faults in cluster #1. However, in the simulation the quality of the signal generation, signal sampling and noise floor was not taken into account. Hardware verification using the 8-bits ADC and 10-bits DAC showed that signal quality on the used experiment hardware was not sufficient to detect these faults using the THD.

This implies that better signal and sampling quality potentially allows better coverage. However, noise conditions will also limit the actual improvements that can be achieved; the noise floor must be sufficient low to be able to measure the harmonics. Besides the equipment demands, also the highest possible signal frequency limits the usability of a THD, since the accuracy increases with the number of harmonics that are taken into account.

For the simulated 120 faults the resulting peak-peak voltage level of a 10 kHz sine wave is shown in Figure 5, where also the upper and lower limits are shown.

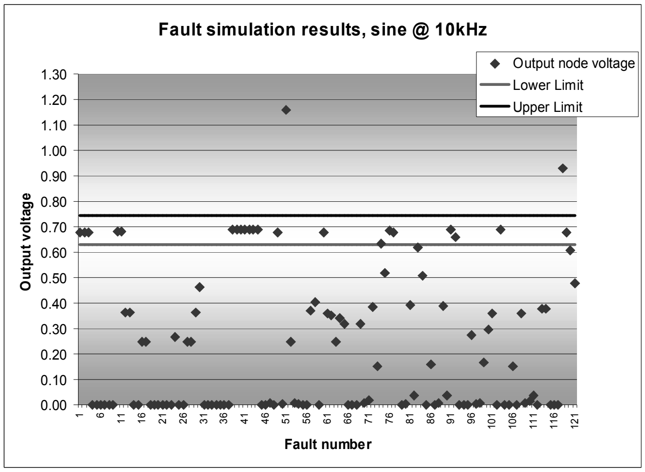


Figure 5: Fault Simulation results

In total 103 faults (86%) result in a peak-peak voltage level outside the limits, and can be detected. A small number of faulty-circuit responses are close to the limits. If a statistical variation on circuits with these faults would be considered, then some of these faulty circuits might change from detectable to undetectable or vice versa. Also, the fault models (other resistance values for opens and shorts) could be varied and the faults could be weighted according layout information. Taking into account these effects is outside the scope of this paper; it is expected that this will not result in major differences for the analysis of suitable test signals.

It was found that a single DC measurement gives 50 to 60% coverage for each of the three clusters. All these faults are also covered by the AC measurement. Figure 6 depicts the overlap between covered faults of the DC and a single-tone peak-peak voltage tests for cluster #1.

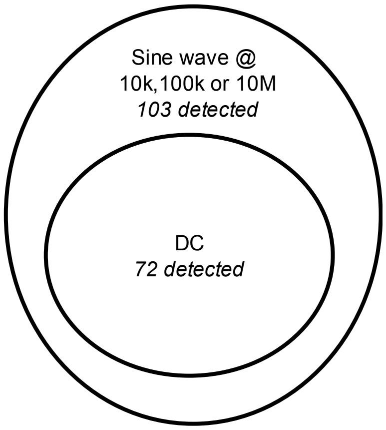


Figure 6: Fault coverage with DC and single-tone AC tests of the 120 analysed faults in cluster #1

For the other two clusters a similar number of faults remained undetected at a frequency of 10 kHz, giving 67% and 70% coverage, respectively.

Using selected components with less statistical spread could allow to tighten the upper and lower limits. In Figure 5 it can be seen that tighter limits would increase the coverage by a few percent.

The faults that remain undetected are typically related to components or parts of the circuit that are added to improve the robustness of the system. In presence of one of these faults, the output signal will still be within specifications under normal conditions. The components typically provide functions like temperature compensation, damping of oscillations, ESD protection, or other additional features. To test these components with a limited access method is hardly possible and only additional test access or non-electrical tests can provide the coverage of those faults. To achieve higher coverage, it is needed to create test access to at least some nodes inside the cluster.

For cluster #1 the fault simulation results have been verified on hardware. All simulated faults have been manually inserted and the coverage of the faults with the selected tests has been verified, using the test limits derived from the statistical simulations. The fault detection on the hardware was identical to the simulated coverage for the DC and AC tests.

For the three analysed clusters it was concluded that with limited test access the functional test can be replaced, and the number of test-lands for a BoN test can be reduced. For the used clusters, a minimal requirement to the test signals is a single-tone frequency in the order of 10 kHz. This minimal requirement depends on the type of clusters. It is very well possible that other clusters require higher frequencies.

These results will be used in the remainder of this paper to verify the feasibility of using on-chip test access for PCB production test.

4. Using IEEE 1149.4 for test access

A standardized method to apply a test signal is through the analogue test bus provided by IEEE 1149.4. Until now we have not seen a wide usage of 1149.4 in production test, which can be explained by several reasons, among which:

- Costs for the additional silicon area and two analogue IC pins.
- Risks of the analogue DfT affecting the functional behaviour of the Mixed-Signal block. The effects of the analogue DfT need to be taken into account already during the design of the Mixed-Signal block.

It has to be noted that 1149.4 can be used to provide access to internal nodes for IC testing. This allows to test circuits that are hard to test with other IC tests, such as RF or High Speed I/O tests. Also for reduced pin-count testing of ICs the 1149.4 infrastructure can be used to allow DC parametric tests [13]. If an analogue test bus is implemented to support IC tests, the additional costs of an 1149.4 implementation for board test are lower.

To verify the bandwidth limitations of an 1149.4 based test of the analogue clusters, measurements have been done on a prototyping hardware set-up using two National Semiconductors SCANSTA400 devices [12]. The measurements were conducted to find the maximal test signal frequency that can be applied to an analogue cluster. This frequency is limited by the routing of the analogue bus on the PCB as well as internal in the IC. Also the switches needed to connect the signal source to the driving pin and the measurement probe to the receiving pin limit the frequency.

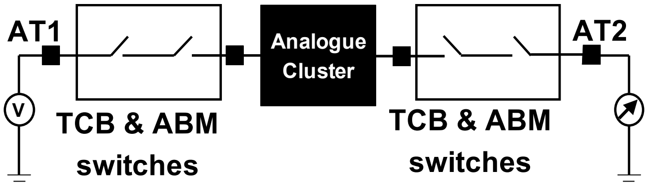


Figure 7: 1149.4 signal path for analogue cluster test

As can be seen in Figure 7, the signal for an analogue cluster test is routed through four 1149.4 switches. In our test set-up we found that frequencies up to several MHz can be used; the –3dB point was at almost 1 MHz. The measured result through the four switches is shown in Figure 8.

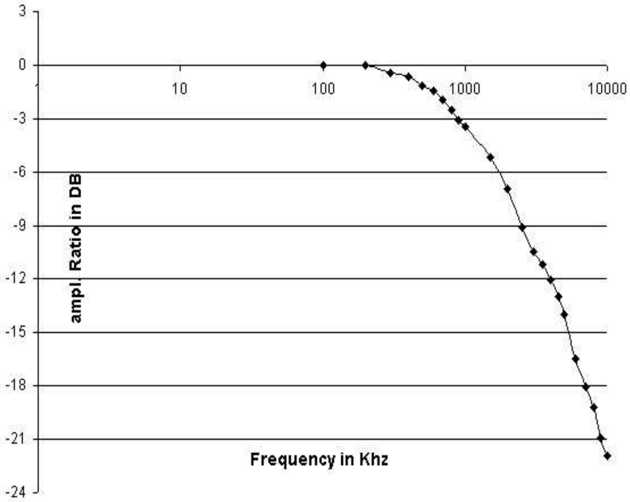


Figure 8: Measured 1149.4 performance through 4 switches

For the targeted clusters the performance is well above the required minimal frequency of 10 kHz.

A feature offered by 1149.4 is the possibility to measure the voltage on the driving IC pin, which could be used in the case of current driven stimulus. This gives one additional test-point. In the case of cluster #1 (Figure 3) the opens on the pins of the resistor connected between the input node and ground are only detected with such a test.

A test based on 1149.4 makes use of external measurement equipment. Consequently there are additional costs involved, while on the other hand the possibility to use high-resolution equipment can be an advantage.

For test preparation with 1149.4 access, the following steps are done:

1. Route the ATAP on the board
2. Determine test signals and measurements by simulation or hardware measurements
3. Select the test equipment
4. Determine test limits, based on simulation or hardware characterization results
5. Verify the coverage of the faults, again either by simulation or hardware experiments

A test sequence based on 1149.4 is as follows:

1. Shift PROBE instruction
2. Shift configure data for the analogue boundary modules and Test Bus Interface Circuit (TBIC)
3. Apply source signal on AT1 and sample the analogue cluster response on AT2.
4. Repeat steps 2 and 3 to select other measurement pins.
5. Calculate the test result from the captured response and verify the value against limits gives the pass/fail condition.

This sequence is repeated for all clusters. One cluster output can be measured at a time, unless multiple analogue test busses are routed on the PCB and multiple pieces of measurement equipment are used.

5. Re-using on-chip Mixed-Signal IC test DfT for PCB test access

We investigated the alternative offered by re-use of on-chip Mixed-Signal test structures for board test. To re-use the existing Mixed-Signal cores connected to the analogue pins we need to have test access to the digital connections of these Mixed-Signal blocks.

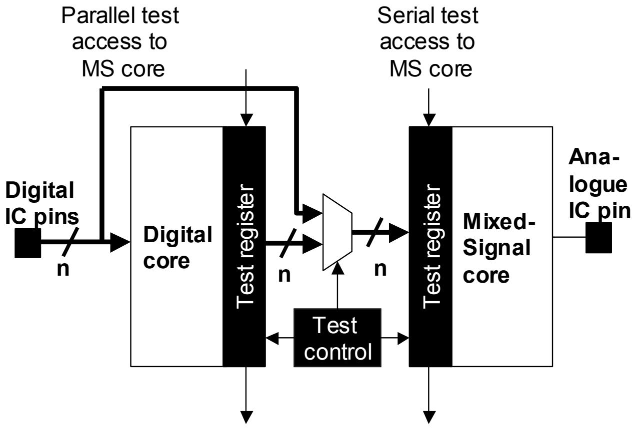


Figure 9: On-chip Mixed-Signal test access

For IC test these pins are often connected to other digital pins during IC test mode, providing a fast parallel test access, see Figure 9. Besides this parallel access also a serial access is used to create access with lower speed requirements and to be able to perform an interconnect test between cores. An IC that is assembled on a PCB does not provide direct access to the multiplexed pins, which makes the parallel access not useable for PCB test. The serial access only requires access to the 1149.1 TAP controller, which makes it useable for a PCB test.

With a serial access method the maximal achievable sample frequency is roughly the TCK clock speed divided by the number of cells to shift. For a 10 kHz signal a sample frequency of 20 kHz or higher is needed. For example, a shift length of 500 TCK cycles or less can be used with a TCK rate of 10 MHz. To allow a higher update and sample frequency, the number of cells to shift must be kept as low as possible. There are a number of possibilities:

- **Pipelining**
  Shift only a part of the serial chain, then update values to a driving block like a DAC, and/or capture values from a receiving block, like an ADC. The number of cells used to access only one Mixed-Signal block roughly dictates the sample rate. Using multiple Mixed-Signal blocks in the same pipeline requires up-front planning of the sequence of the blocks in the scan chain. For example, captured results from an ADC should not overwrite values needed for a DAC further down the scan chain.
- **Dedicated registers for each Mixed-Signal block**
  This gives serial access to only one of the blocks at the time and requires a separate TAP instruction for each Mixed-Signal block.
- **Selectively bypassing cells that are not used.** This allows to access multiple cores simultaneously and requires a configuration register to control the bypasses.

The Philips Semiconductors internal core-based test strategy for Mixed-Signal cores [7] provides the serial access with bypass possibilities.

The on-chip DfT is depicted in Figure 10. Each core is wrapped in a test-shell. Each test-shell provides the test access to one core and is controlled by a Test Control Block (TCB). A TCB, which is also the test control mechanism for digital cores, is a shift and update register. The control bits for one core can be loaded in the TCB, which is comparable with the P1500 WIR [4]. Multiple TCBs can be concatenated into chains that are addressed by 1149.1 TAP controller instructions [18]. Control bits are typically not changed during a test, an example of a control bit is the signal that selects the bypass of the core.

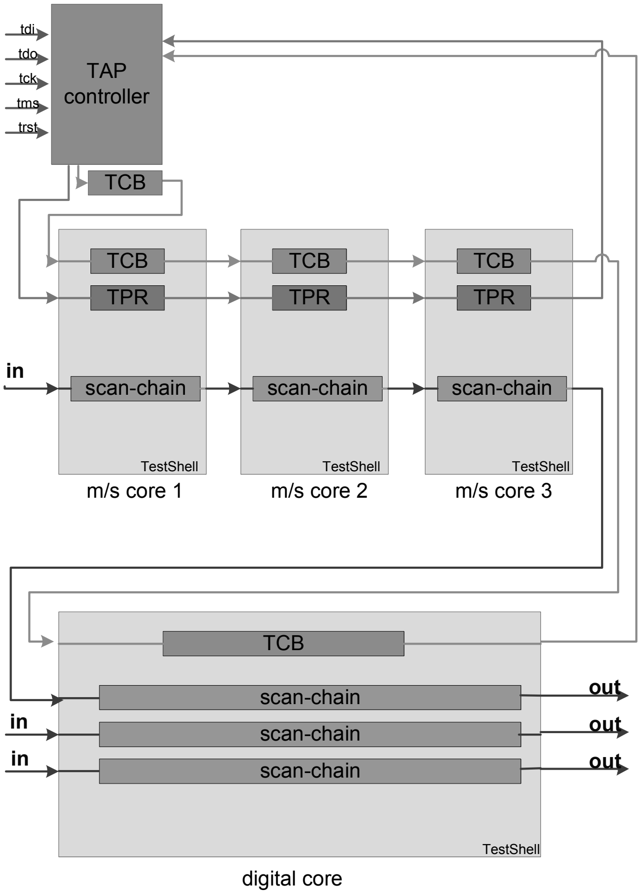


Figure 10: On-chip core-based DfT for Mixed-Signal cores

For Mixed-Signal IC tests a fast, parallel access to a number of ports is needed, which is provided by connecting these ports to IC pins in test mode. Serial and parallel access to the digital ports of the Mixed-Signal cores is done through a Test Point Register (TPR). Mixed-Signal cores are often tested in various modes, which can be selected by shifting a specific word into the TCB. Like the TCB, the TPR registers can be combined in chains that are user registers in 1149.1. One of the default test modes is a bypass mode, where the TPR is replaced by a single-cell register. This allows to adapt the TPR chain length to give an as-short-as-possible serial access to the Mixed-Signal core.

The feasibility of re-using the on-chip mixed signal DfT for PCB test has been verified in a prototyping system. Two ICs have been programmed into an FPGA, both ICs are equipped with a TAP and internal access to the Mixed-Signal cores.

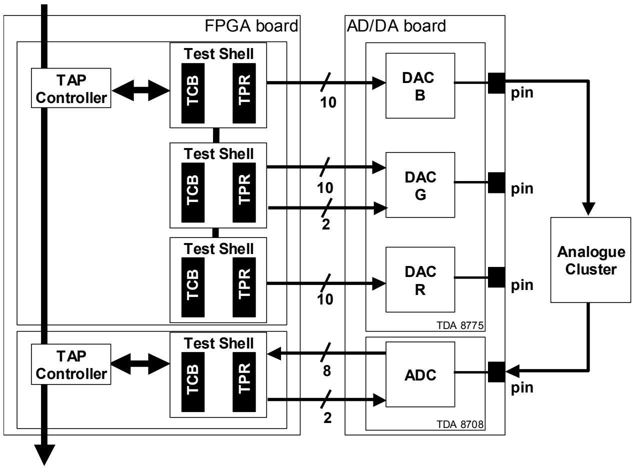
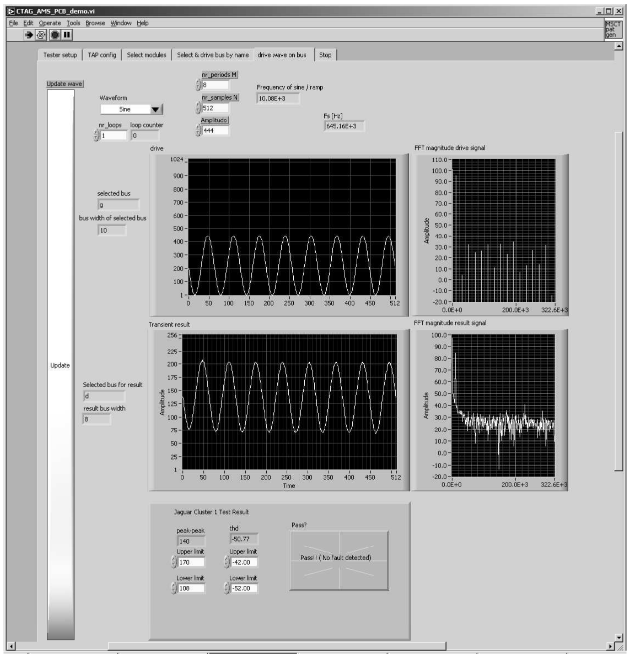


Figure 11: Schematic representation of the verification system

The implementation of the prototyping system is shown in Figure 11. The digital parts of both ICs are implemented in the FPGA, the Mixed-Signal part is implemented with a stand-alone ADC and a triple video DAC IC. One of the 10-bits video DACs is used to drive the input of the analogue cluster, while the 8-bits ADC samples the response. During the test, the Mixed-Signal blocks need to be clocked, in this case the TCK has been used to provide the clock to the DACs and ADC.

In practice these Mixed-Signal cores will be part of larger SoCs, containing a number of digital and Mixed-Signal cores. In such a SoC the control and data registers will be part of larger registers, such as the TCB. Information of the implemented DfT is needed to be able to control, drive and capture the Mixed-Signal cores. With this information the test vectors that contain the test signal waveform can be made and the captured bits can be extracted from the captured data stream.

For the experiment a software tool has been made in LabVIEW, a graphical programming environment from National Instruments. The front panel is shown in Figure 12. The tool reads the DfT configuration from the ICs and allows to select a driving and receiving core in a selected test mode. After the selection a waveform and an analysis method with test limits can be selected. The tool automates the mapping of the calculated bit patterns into the test patterns and runs the test using a standard PC-based Boundary Scan tester. Using standard available routines the application and analysis of various signal waveforms is possible. These signals can be applied and verified immediately, without the need for Mixed-Signal equipment and without probing. This allows fast system debug, test development and fault diagnosis.



Waveform: Sine
nr_loops: 1
loop counter: 0
nr_periods M: 8
nr_samples N: 512
Amplitude: 444
Frequency of sine / ramp: 10.08E+3
Fs [Hz]: 645.16E+3
selected bus: g
bus width of selected bus: 10
Selected bus for result: d
result bus width: 8
peak-peak: 140
Upper limit: 170
Lower limit: 108
thd: -50.77
Upper limit: -42.00
Lower limit: -52.00
Pass!! (No fault detected)

Figure 12: LabVIEW tool to apply and analyse test signals through Mixed-Signal cores

With the experiment set-up a maximal sample frequency of 1 MHz for simultaneous signal generation and sampling was obtained, which is well above the minimum of 2*10 kHz sample frequency for the targeted clusters.

Application of THD analysis depends on the signal and sampling quality of the available Mixed-Signal cores. In our experiment set-up the THD analysis did not result in detection additional faults. We attribute this to the noise floor and limited resolution of the used DAC and ADC in the experiment system.

It is not possible to drive a current and read back the resulting voltage level at the cluster input with the MS DfT based method.

To be able to make use of the existing on-chip MS DfT for board level test, the following requirements are made to the IC:

- A serial access path through the TAP to the digital ports of the Mixed-Signal core
- In test mode the Mixed-Signal cores must be provided with a clock
- DfT information such as configuration register settings and data register settings must be provided for the relevant test modes.

For test preparation the following steps are done:

1. Route the TAP on the board
2. Obtain and apply the on-chip DfT information to

select the relevant Mixed-Signal cores
3. Determine test signals and measurements by simulation or hardware measurements
4. Determine test limits, based on simulation or hardware characterization results
5. Map the test signal waveforms on bit positions in the test vectors
6. Obtain the sampled bits from the captured bit stream and analyse the waveform
7. Verify the coverage of the faults, again either by simulation or hardware experiments

For steps 5 and 6 tool automation is required.

A board test sequence based on internal access is as follows:

1. Select the instruction to program the TCB
2. Shift test control data
3. Select the instruction to program the TPR
4. Repeatedly shift all test data vectors
5. Apply analysis on sampled waveform

Steps 1 to 5 are repeated for all clusters. Multiple clusters can be driven and captured simultaneously.

6. Comparison of the alternatives

In the two previous chapters the usability of 1149.4 and MS DfT based methods have been described. Both have their advantages and disadvantages. As with any limited access method, both alternatives cannot offer full coverage of all possible faults for the analysed clusters. The 1149.4 method offers a slightly higher coverage because it allows to measure at the driving pin. It also gives the possibility to use equipment with better signal generation and sampling properties, which together with the higher bandwidth can be exploited for analyses such as a THD. The MS DfT based method does not have the possibility to use better equipment since it uses the on-chip signal generation and sampling circuits. At the same time this is an advantage since it decreases test equipment requirements. The 1149.4 based method does not give the possibility to test multiple clusters simultaneously, which gives it a disadvantage in test time. A potential bottleneck for re-usage of MS DfT might be the availability of IC DfT information. Since 1149.4 is an IEEE standard the information is standardized in a BSDL extension to be delivered with the IC. To use this information and map the signal waveforms to test vectors, the MS DfT based method requires software tooling, which is to a much lesser extend the case for 1149.4. Since 1149.4 it is an IEEE standard, commercial tooling might become available.

The major difference however is related to IC implementation; while the MS DfT based method re-uses existing circuits, the 1149.4 is really additional, adding silicon costs and analogue design effort.

The advantages and disadvantages of both methods have been summarized in Table 1, where the advantages have been highlighted.

Table 1: Comparison of both alternatives

Item	1149.4	MS DfT
IC level DfT Cost	Limited IC silicon area. Analogue design effort	None or very limited silicon area and design effort
PCB level DfT Cost	Analogue bus	None
Fault coverage	Order of 85% Potentially few % higher	Order of 85%
External equipment	Yes	No
Simultaneous test of multiple clusters	No	Yes
Tooling needed to map waveforms to test vectors	Hardly	Yes
IC information	Standardized	Not standardized

Comparison to other test methods

How do the methods that use on-chip DfT compare to widely used methods like Bed-of-Nails and functional tests?

The two alternative methods, 1149.4 and MS DfT, do not use access to internal nodes but and are not limited to signals in the application area. Therefore they will provide at least equal coverage compared to functional tests. Potentially the coverage of these two alternative methods is slightly higher than a functional test, if signals waveforms outside the functional application area and analyses such as THD can successfully be applied.

Parts of the analogue clusters affect the behaviour of the system only under specific conditions. Defects in these parts do generally not lead to catastrophic failures and under normal conditions they cannot be detected without access to internal nodes of the clusters. The two alternative test methods have limited access to the clusters and as a consequence they will not be able to detect all defects related to these parts. The method using a BoN does provide access to internal nodes of the analogue clusters, at the cost of additional board area for the test lands.

The tests using 1149.4 or the MS DfT can be developed rather easy, using software like the tool described in section 5. Development of a functional test targeted at specific faults can be harder. Generally it is an iterative process, where several steps are needed to generate test patterns with sufficient fault coverage.

The tests using 1149.4 or the MS DfT provide diagnostic information at least to the level of the analogue cluster. It is possible to increase the diagnostic capabilities when information about responses of faulty circuits is used. This information can for example be obtained from fault simulations. The diagnostic capabilities of a functional test are limited; the system either works or not and it is often hard to locate the defect. The diagnostic capabilities of a BoN can be up to the level of individual components and is only limited by the provided test access.

7. Conclusions

The on-chip Mixed-Signal DfT as well as the IEEE 1149.4 based methods are alternatives that can be used to reduce the number, but not eliminate all of the test lands for a Bed-of-Nails test and to achieve better diagnostic resolution than a functional test of the system.

Compared to each other, the IEEE 1149.4 based method has a slight advantage for achievable signal quality and bandwidth. With high quality equipment this advantage can be exploited to detect a few more defects. However, the on-chip Mixed-Signal DfT based method can be used without external measurement equipment and does not require additional on-chip DfT for board test.

The on-chip Mixed-Signal DfT based method can be used at hardly any costs to quickly generate tests for analogue clusters. This makes the method very suitable, initially in design and production ramp-up phases, where design changes are possible. Later on, in high volume production phase, the method allows to reduce the number of test lands.

Acknowledgements

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