

IEEE Std 1149.6 Implementation for a XAUI-to-Serial 10-Gbps Transceiver

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Abstract

The design, implementation and verification of IEEE Std 1149.6 IP for a transceiver manufactured with 90 nm technology and using Current Mode Logic (CML) are challenging because (i) CML has high operating frequency, (ii) CML has very low operating voltage range, and (iii) CML is inherently a differential type of circuitry. This paper describes how major building blocks of IEEE Std 1149.6 IP—such as input test receiver, boundary scan register containing new AC boundary scan cells, output test signal generation circuitry, and modified TAP controller—were implemented and verified. Third-party CAD tools typically used for IEEE Std 1149.1 IP generation were used for this implementation.

1. Introduction

From the last decade, IEEE¹ Std 1149.1TM technology has been successfully used for board level interconnects testing [1]. Through this standard, different vendors incorporate a consistent testing architecture on their components, which allows a system developer to test chip-to-chip interconnects on a Printed Circuit Board (PCB). There are three basic components to this test architecture: (i) a test access port interface consisting of four (optionally five) ports, i.e., TDI, TDO, TMS, TCK and TRST, (ii) a test access port controller (TAP controller), and (iii) a boundary scan register consisting of “shift-and-load” elements (called Boundary Scan cells).

The IEEE Std 1149.1 provides sufficient test coverage of “stuck-at” faults for digital (or DC) interconnects only. For a board consisting of mixed-signal devices, the testing of analog (or AC) interconnects is carried out through some other ad hoc methods. A new standard IEEE Std

1149.4 was developed in 1999 to provide IEEE Std 1149.1 a compatible mechanism to test analog, mixed-signal and digital parametric for an IC and PCB containing these ICs [2].

Many systems designed today contain high-speed serial communication interconnects. These interconnects often use AC-coupling and/or differential signaling. With differential signaling, it is easier to handle the timing by controlling the crossover points than controlling the voltage levels relative to another reference (as in the case of single-ended signaling). In addition, differential signaling enables higher speed for data transfer and better signal-to-noise ratio. AC-coupling enforces compatibility between receiver and driver, which have different common mode voltages, by providing the level shifting capability.

Neither IEEE Std 1149.1 nor IEEE Std 1149.4 provides an effective and simple testing protocol with adequate fault coverage for high-speed serial communication interconnects. A few successful techniques have been developed for testing for these kinds of applications [3,4]. Cisco’s ACJTAG approach, based on IEEE Std 1149.1, provides a systematic methodology for testing high-speed AC-coupled IOs². Intel’s IBISTTM approach is a comprehensive on-line solution covering a broader fault spectrum associated with the testing of high-speed I/Os. Both of these techniques are proprietary and do not offer benefits similar to an IEEE Standard.

Recently, in 2003, a new standard called IEEE Std 1149.6 has been developed, through which DC, AC and high-speed serial interconnects on a PCB can be tested [5,6]. IEEE Std 1149.6 is also built upon IEEE Std 1149.1, using the same test access port interface of four (or five) pins, a TAP controller and a boundary scan register. IEEE Std 1149.6 adds the concept of an “input test receiver” to the input pins that are expected to handle differential signaling and/or AC-coupling. It adds a new set of AC boundary scan cells to be used for the AC pins. Also

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² ACJTAG is the precursor and a major contributor to IEEE Std 1149.6.

added are two new instructions which cause drivers to emit AC waveforms that are processed by test receivers [5].

Like its predecessor IEEE Std 1149.1, this new IEEE Std 1149.6 is going to be the leading test interface for all future PCB containing analog networks with AC-coupled and/or differential interconnections. A proof-of-concept silicon implementation of IEEE Std 1149.6 has demonstrated that this standard has backward compatibility with IEEE Std 1149.1, reasonable noise rejection, and high fault coverage [7].

Intel® LXT35401 XAUI-to-Quad 3.2G Transceiver device has incorporated IEEE Std 1149.6. This paper describes the design and implementation of various building blocks of IEEE Std 1149.6 for this transceiver, such as an input test receiver, output test signal generation circuitry, boundary scan register and TAP controller. The IEEE Std 1149.6 document contains general guidelines on designing these building blocks. The input test receiver examples provided in the IEEE Std 1149.6 are for the LVDS channels only. I. Duzevik in [8] and Eklow *et al.* in [9] have presented a few general but practical design and validation considerations for this new test protocol.

The design details presented in this paper are for a practical device designed with CML and contains very high-speed (3.125 – 11.3 Gbps) differential driver and receiver ports. Very low voltage range (400 mV) of CML and high-speed signaling pose new design challenges. Designing for such rigorous requirements and illustrating those designs in this paper are the major contribution of the work discussed here. This paper also presents brief discussions on the CAD flow used in and the cost associated with the implementation of IEEE Std 1149.6 IP in the transceiver chip.

2. Testing AC Interconnects

Systems containing high-speed interconnects usually have on-chip or on-board coupling capacitors, which prevent a DC value from being driven between a driver and receiver. Thus, an AC testing methodology must use a time-varying signal to pass through AC-coupling. AC-coupling causes signals to decay over time, and it is essential for test data to be captured within a certain time window. In addition, differential AC interconnects can have its specific defects that are not tested by DC technology. It is also desirable to have compatibility between AC testing and DC testing for systems with AC paths using DC-coupling. A mechanism which has the capability to detect both edge change and level change is needed.

IEEE Std 1149.6 addresses all the above stated requirements and thus provides defect coverage for both DC-coupled, AC-coupled single-ended and differential signal interconnects [5]. For a more elaborate discussion on this topic, see References [5] and [6].

3. Transceiver Details

Intel® LXT35401 XAUI-to-Quad 3.2G Transceiver chip encodes and multiplexes the 4 x 3.125 Gbps (10 Gbps aggregate) Attachment Unit Interface (XAUI) serial data streams into a 10 Gbps serial data stream. The 10 Gbps serial interface provides data to the 10GBASE-R PMD in fiber optic module applications. The transceiver provides an IEEE802.3ae compliant interface for both XAUI and 10G serial connectivity and management interface.

The XAUI interface transfers 10 Gbps of information on four 8B/10B encoded, 3.125 Gbps, serial differential pairs in each direction, while the 10 Gigabit serial interface (XFI) transfers 10.3125 Gbps in each direction. This constitutes 10 pairs (5 for transmitter and 5 for receiver) of high-speed differential signals for the overall device.

The transceiver chip is fabricated in a 90 nm CMOS (1.2 V) technology using CML. CML is used because of its reduced dl/dt effects, process and voltage variation immunity, common mode noise immunity, and small switching noise effects on neighboring analog circuitry. CML devices are often ultra-low power consuming devices [10].

4. Implementation

The basic architecture of IEEE Std 1149.6 is similar to that of IEEE Std 1149.1. In IEEE Std 1149.6, the boundary scan register contains both the DC and AC boundary scan cells. The input analog pin-pairs have Input Test Receivers (ITR), the output AC pins (pairs) have “Output Test Signal Generation” circuitry (OTSG). It also contains a modified TAP controller. A schematic view of a device containing IEEE Std 1149.6 IP is shown in Figure 1 on the next page.

4.1 Input Test Receiver (ITR)

The test receiver must reconstruct an original waveform driven either from a single-ended driver or from one leg of a differential driver that is either AC- or DC-coupled and is insensitive to DC offsets that may exist in the driven waveform. It does so by responding to the edges of

the original waveform that are still present despite AC- or DC-coupling.

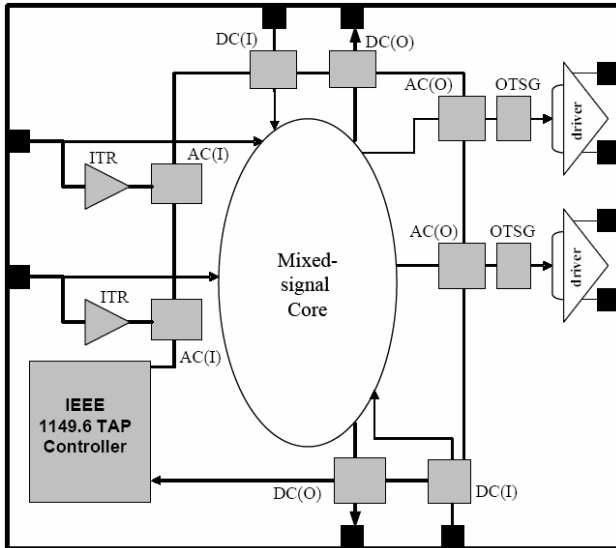


Figure 1 A mixed-signal device with IEEE Std 1149.6 components.

The new instruction called EXTEST_PULSE is implemented to handle the AC-coupled signals. Input test receiver is also compatible with EXTEST (DC mode) instruction. In DC mode, it “turns off” the edge-detecting capability of the test receiver and responds only to the levels.

IEEE Std 1149.6 document presents a typical design of input test receiver which incorporates edge detection as well as level detection mechanisms to handle both the AC- and DC-coupling. The ITR developed here is based on the design shown in Figure 49 of IEEE Std 1149.6. Figure 2 shows the ITR schematics for the transceiver device. Note that each leg of the differential signal has its own edge/level detection circuitry.

Table 1 shows design specification for the I/O interfaces used in the Intel® LXT35401 XAUI-to-Quad 3.2G Transceiver. Since this transceiver has two high-speed interfaces XAUI and XFI, an attempt has been made to find a common set of specifications. Table 2 shows actual values of design parameters used for the implementation of ITR. The same ITR was used for the receiver channels associated with both interfaces. The choice of these design specifications are based on (i) XAUI and XFI interfaces’ requirements, (ii) empirical formulae suggested in the IEEE Std 1149.6, and (iii) the simulation results.

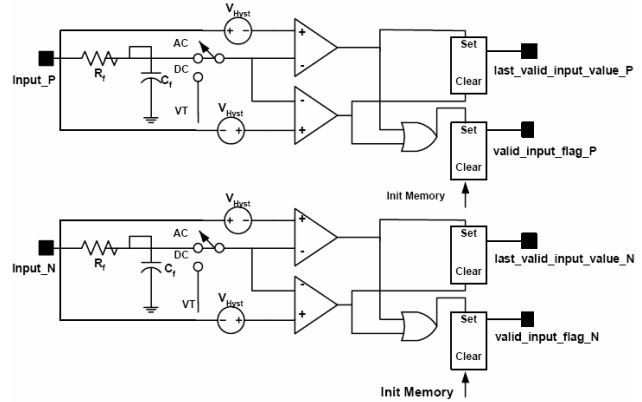


Figure 2 Input test receiver for an input differential pin pair.

Table 1 High-speed I/O specifications for Intel® LXT35401 XAUI-to-Quad 3.2G Transceiver.

| Specification Parameter | XAUI | XFI | Common Spec. | Units |
|-------------------------------------|----------|----------|--------------|-------|
| Driver output swing (differential) | 500-1600 | 450-1125 | - | mV-pp |
| Receiver input swing (differential) | 175-1600 | 110-1050 | - | mV-pp |
| Input common mode | 1.2 | 1.2 | 1.2 | V |

There are two main challenges involved in the designing of the test receiver. First, the receiver must reconstruct the original waveform in no-defect environment, and second, the receiver must manifest syndromes in the presence of various potential defects. The test receiver designed here considers all the potential defects described in IEEE Std 1149.6 (Table 1 on Page 18 of Reference [5]).

It is essential to carry out input test receiver verification for all the potential defects associated with appropriate termination scheme on a PCB for the “device under test.” As shown in Figure 3, the test bench to verify the test receiver consists of a Failure Injection Module modeling the termination scheme and driver test signals. Setting appropriate values in the Failure Injection Module (such as TX1_1 open, RX1_1 short to ground, C1 pin 1, 2 shorted together, R pin1 open, C1 pin 1 short to C2 pin 2, and so on) creates different targeted defects. All these defects create corresponding “test syndromes” in the test receiver. The ITR designed here was verified using all the possible open and short faults in signal paths as well as in passive components used for termination.

Table 2 Design specifications for IEEE Std 1149.6 input test receiver used in Intel® LXT35401 XAUI-to-Quad 3.2G Transceiver.

| Specification Parameter | XAUI | XFI | Common Spec. | Units |
|---|------------|------------|--------------|-------|
| T_{Trans} (Max) | 160 | 48.5 | 160 | ps |
| ΔV_{Min} (single-ended) | 200 | 180 | 180 | mV |
| ΔV_{Max} (single-ended) | 800 | 562.5 | 800 | mV |
| $V_{Threshold}$ | 1.2 | 1.2 | 1.2 | V |
| V_{Hyst_Level} | 40 | 40 | 40 | mV |
| V_{Hyst_Edge} (0.6 of ΔV_{Min}) | 120 | 108 | 108 | mV |
| T_{Hyst}^* | - | - | 2.25 | ns |
| LP_Mult^\dagger | 9 | 9 | 9 | |
| $T_{LP}(min)^\ddagger$ | 7.2 | 2.2 | 20 | ns |
| $HPLP_Ratio^\ddagger$ | 8 | 8 | 8 | |
| HP_Mult^ξ | 72 | 72 | 72 | |
| $T_{HP}(min)^\psi$ | - | - | 160 | ns |
| $T_{Test}(min)^\ddagger$ | $3*T_{LP}$ | $3*T_{LP}$ | $3*T_{LP}$ | |
| Comparator bandwidth (min) | - | - | 30 | MHz |
| Comparator input sensitivity (min) | 10 | 10 | 10 | mV |
| Comparator input offset (3σ) | 10 | 10 | 10 | mV |
| Maximum test input frequency | - | - | 10 | MHz |
| * Values determined through circuit simulation. It has to be $> 5*T_{Trans}$ | | | | |
| † From IEEE Std 1149.6 | | | | |
| ‡ Values determined through circuit simulation. $T_{LP}(min) > LP_Mult * T_{Hyst}$ | | | | |
| ξ $HP_Mult = HPLP_Ratio * LP_Mult$ | | | | |
| ψ Values determined through circuit simulation. $T_{HP}(min) > HP_Mult * T_{Hyst}$ | | | | |

4.2 Boundary Scan Registers

The AC input boundary scan cell of IEEE Std 1149.6 is conceptually similar to the DC boundary scan cell of IEEE Std 1149.1. However, the capture flip-flop (FF) of the AC input boundary scan cell captures the test receiver output and provides the output of capture FF as initial state data to the hysteretic memory inside the ITR. The hysteretic memory is cleared, in accordance with the rule f) in 6.2.1.1 (of IEEE Std 1149.6), by preloading the memory with the capture FF value. The default value will then be recaptured if there are no valid inputs to change it, preserving the capture cell contents in accordance with rule g) in 6.2.1.1 (of IEEE Std 1149.6) and if there are no valid input to change (valid_input_flag signal) [5]. This scheme is shown in Figure 4.

The AC_1 (output boundary scan cell as described in Appendix C of IEEE Std 1149.6) is somewhat similar to the corresponding DC boundary scan cells (BC_1 of IEEE Std 1149.1). This AC boundary scan cell (as shown in Figure 5) has an extra multiplexer controlled by “AC Mode,” which is used to select either the Update register content (for the case of EXTEST) or that same content modulated by an exclusive OR gate with the AC test signal (for the case of EXTEST_PULSE). Note that this implementation differs from AC_1 in two respects. (i) It does not have input multiplexer necessary for INTEST operation, and (ii) it does not have output multiplexer which multiplexes between mission input and test signal. That is because this implementation does not have optional INTEST incorporated and the output multiplexer was placed after the OTSG circuitry (as described in the next subsection).

Also, the optional AC/DC selection boundary scan cells were not included in this implementation.

4.3 Output Test Signal Generation Circuitry

IEEE Std 1149.6 test interface has two new instructions which make the output drivers, on the component incorporating IEEE Std 1149.6 interface, emit AC waveforms (AC test signals) that are processed by the input test receivers at input pins.

Rule 6.3.1.1 (e) of IEEE Std 1149.6-2003 describes, “When any test mode instruction is effective, an enabled output driver of an AC output pin (channel) shall produce on its output(s) a transition matching the levels and edge slew rate of the mission performance specified for the driver.” A simple scheme has been implemented to generate IEEE Std 1149.6 compliant test signals as shown in Figure 6.

The low-frequency CMOS AC test signal (coming out of an output AC boundary scan cell) passes through a buffer chain, a CMOS to CML converter, high-speed differential multiplexer and an output driver. The buffer chain sharpens the edges (the rising and fall times) of the test signal. For example, in the case under discussion, a signal of 10 MHz with rise and fall times of 25ns was translated into a test-signal having the same frequency but with the rise and fall times equal to the 12ps. The CMOS to CML converter transforms the single-ended CMOS test signal into a differential CML signal. In the AC test mode (i.e., EXTEST_PULSE), a high-speed differential multiplexer passes this test signals to the output driver. In Figure 6, high-speed differential multiplexer and output drivers are not shown as components of OTSG because these two

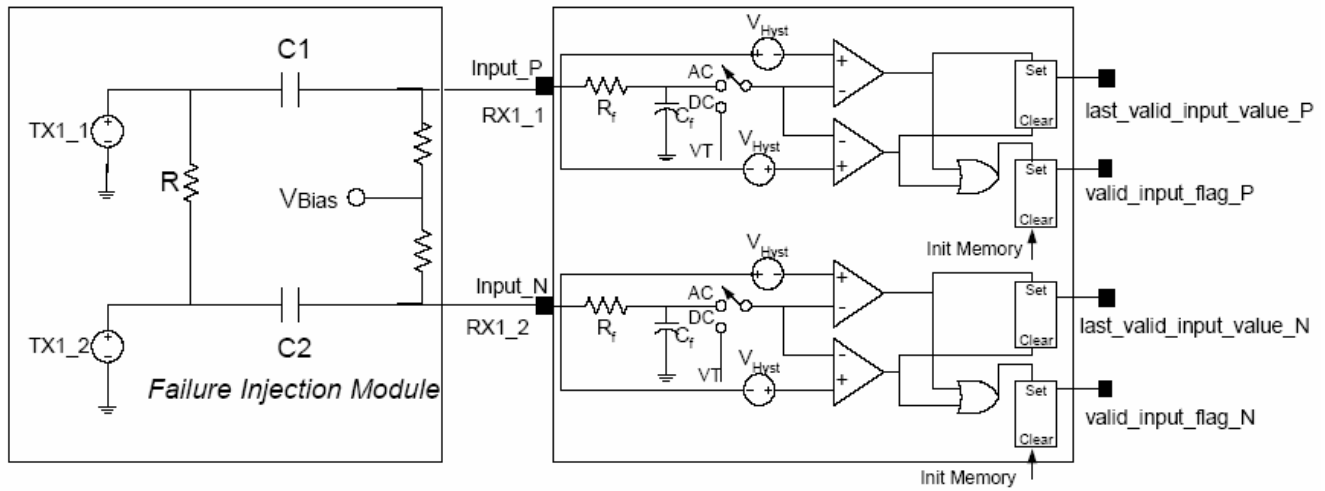


Figure 3 Input test receiver verification scheme to model the potential defects.

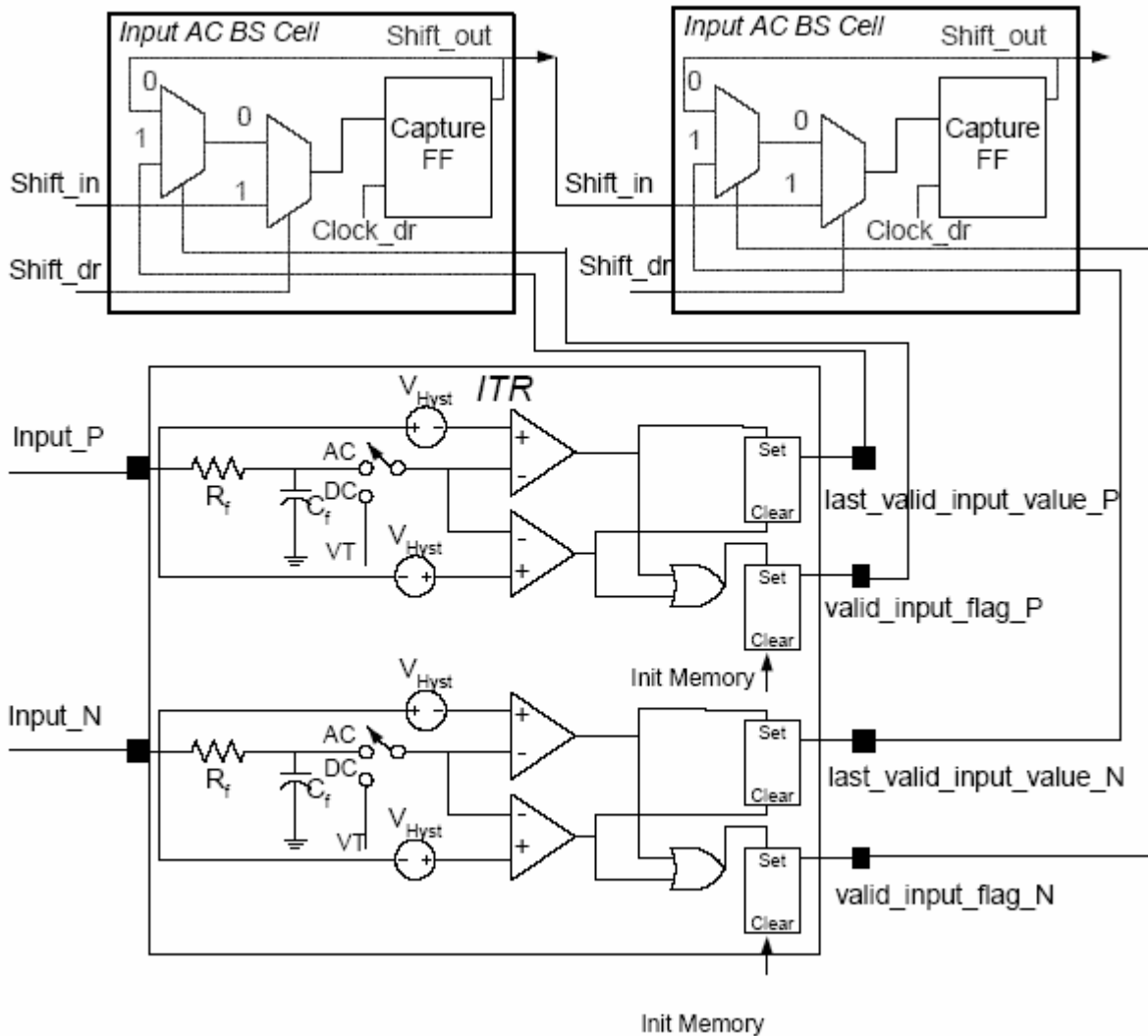


Figure 4 AC input boundary scan cells schematics and its connectivity with input test receiver.

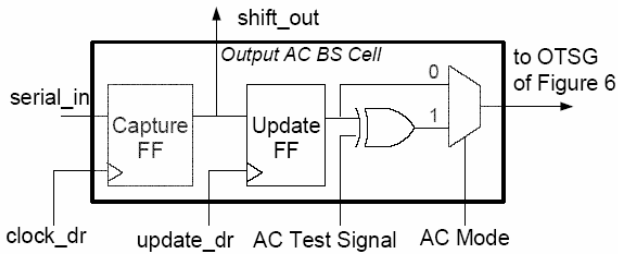


Figure 5 AC_1 like output AC boundary scan cell used in this implementation.

modules are part of the functional circuitry. However, due to the boundary scan, the initial required 2-to-1 multiplexer was redesigned to be a 3-to-1 multiplexer.

Another elaborate scheme which generates mission-data like AC test signal was also considered. This scheme uses a high-speed differential D Flip-flop (DFF) instead of the buffer chain. This DFF samples the converted low-frequency differential CML signal with un-sharpened edges at very high frequency (3.125 GHz for XAUI and 10.5187 GHz for XFI). These high-speed sampling clock signals are available on-chip for the transmitter's functionality. The DFF block was also available as a basic building block of functional circuitry. It therefore does not need to be designed from scratch. This option not only creates a test signal "matching the levels and edge slew rate," but also with the frequency "of the mission performance." This scheme, however, was more costly (in terms of area as well as verification effort) than the one shown in Figure 6. IEEE Std.1149.6 does not require AC test signal to have high frequency; this costly option was not built-in.

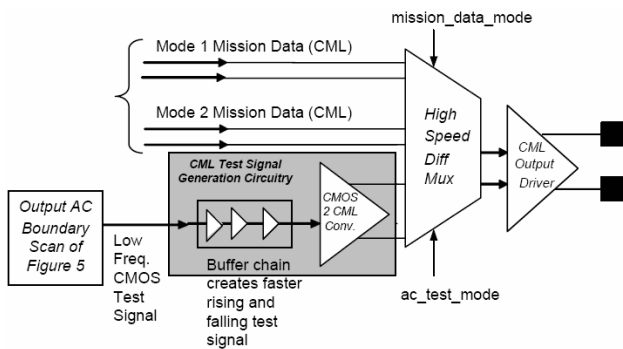


Figure 6 Circuitry for generation of IEEE Std 1149.6 compliant CML test signals.

4.4 IEEE Std 1149.6 TAP Controller

TAP controller for IEEE Std 1149.6 is essentially the same as that of IEEE Std 1149.1. However, control logic was added: to implement the two new instructions, the

AC/DC operation modes of boundary scan register, and the initialization of input boundary scan cells.

5. Cost

All design-for-test solutions incur some cost. The cost is justified by savings made during the production tests of IC and the system that contains the IC. The implementation cost of IEEE Std 1149.6 IP for this device can be analyzed in terms of three aspects: performance, area and design time.

At the receiver side, the mission signal sees ITR in its parallel, and on the driver side, the mission signal sees buffer chain, CMOS2CML and 3-to-1 multiplexer blocks in its series (as shown in Figure 1 and Figure 6). All these blocks provide overhead loading and may degrade the performance of mission signals. To avoid adverse impact on the performance, a 'power down' scheme was implemented to turn these modules off during the functional mode. The 3-to-1 multiplexer was partially (only the AC test signal portion of differential logic) turned off because it is a part of functional circuitry.

This design does not include the optional INTEST signal. Thus only low-frequency signal is propagated through AC I/Os during the test mode. Because of the low frequency of test signal, hardly any performance degradation occurs while it passes through ITR on receiver side and OTSG, CMOS2CML, and multiplexer on driver side.

During the layout, various measures were taken to minimize impact on performance. The LXT12101 XAUI-to-Serial 10G Transceiver is offered in a Ball Grid Array (BGA) package. To minimize the signal integrity issues, (i) the ITR and OTSG modules were placed near the respective bumps/pads, and (ii) signal traces of test logic (where necessary) were spaced appropriately. All the control signals for boundary scan cells and the test clock were balanced to minimize of clock-skew effects.

All the digital blocks (TAP controller and digital boundary scan cells) were automatically synthesized, placed and routed. The test logic (digital and analog) occupied a very minimal area on the chip. Unlike high-speed functional analog cores of the device, the test logic can be placed directly under the bump/pads, as long as the test logic is not routed on the topmost metal layer. The device package was large enough to accommodate the area-overhead associated with the test logic. Thus the effective area-cost associated with IEEE Std 1149.6 IP was zero.

The highest cost paid derived from design time overhead. The design of ITR and its verification were the major tasks which took close to one man-month. In addition, tasks such as the specification of the boundary scan register's architecture and design, the layout and placement of test logic, and the verification of IEEE Std 1149.6 took about 3-4 man-months. It can be safely assumed that for a project like a transceiver, one extra designer is required to implement and verify IEEE Std 1149.6 IP for the entire length of the design cycle.

6. CAD Flow

Several CAD tools for IEEE Std 1149.1 are available on the market today. These tools make boundary scan IP generation process a fairly easy task. There was no third-party CAD tool available to implement IEEE Std 1149.6 IP when it was developed.

Nonetheless, any of IEEE Std 1149.1 IP generation tools which allow insertion of custom boundary scan cells can be used to insert IEEE Std 1149.6 IP. The case under discussion successfully used such third party tool capable of handling custom boundary scan cells to implement IEEE Std 1149.6. Digital wrappers for the custom designed AC input and output boundary scan cells were developed. The behaviors of these custom boundary scan cells and differential pads were modeled, and a custom library was developed. The tool generated the RTL code for TAP controller, boundary scan register with custom digital and AC boundary scan cells. The TAP controller was manually modified to incorporate the two new instructions of IEEE Std 1149.6 and to include the control logic associated with the functionality of AC boundary scan cells.

Compliance checking can be done with the third-party tools as well. BSDL files and compliance test benches generated by third-party (IEEE Std 1149.1 IP generation) tools can be manually edited to allow for the checking of IEEE Std 1149.6 IP. The modified BSDL file included the definitions of new AC boundary scan cells, AC/DC boundary scan register and two new instructions of IEEE Std 1149.6. The new test benches verified the behavior of two new instructions and data flow through the AC/DC boundary scan register.

The verified RTL code files for generated and modified blocks of the IP were automatically synthesized, placed and routed like other random and custom logic using the industry-standard tools.

7. Verification

IEEE Std 1149.6 compliance verification is a little more complex than IEEE Std 1149.1 compliance verification. IEEE Std 1149.6 has two new instructions, which needed to be verified. Due to presence of analog blocks like input test buffers and output test signal circuitry generation, one has to use mixed-signal simulation tools. An alternative way is to model the analog blocks for digital simulator and carry out the verification in digital domain. This would provide overall architecture verification. However, the individual analog blocks must be verified using the mixed-signal simulator. This methodology was used in the verification of this IP.

A silicon validation plan is underway for this device, and results are not available at the time of the publication of this paper.

8. Summary

IEEE Std 1149.6, like its predecessor IEEE Std 1149.1, is gaining more popularity and becoming the leading test interface for all future PCB boards containing AC-coupled high-speed differential signals which was missing in IEEE Std 1149.1. Some elements of IEEE Std 1149.6 architecture are more or less similar to IEEE Std 1149.1 as regards test access port interface, TAP controller and boundary scan register. However, the implementation of the new elements—the input test receiver, new instructions, and the output test signal generation—for various technologies is a challenging task.

This paper presented the implementation of IEEE Std 1149.6 IP for Intel® LXT35401 XAUI-to-Quad 3.2G Transceiver device. This device has very high-speed differential driver and receiver ports and uses the CML—a differential type of circuitry operating with very low voltage range (400 mV). The quality of the PCB test depends upon accurate design of the input test receiver and the output test signal generation circuitry of the device. The implementation details of these critical blocks presented here would be useful for future designers of IEEE Std 1149.6.

This paper also showed that third-party CAD tools available for IEEE Std 1149.1 IP's generation can be customized to implement and verify the IEEE Std 1149.6 design blocks. The only significant cost associated with this DFT technique is in terms of design time over head (one extra designer throughout the development of the project). The area and performance costs were negligible.

9. Acknowledgements

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10. References

- [1] IEEE Std 1149.1-2001, IEEE standard test access port and boundary-scan architecture, 2001.
- [2] IEEE Std 1149.4-1999, IEEE standard for a mixed-signal test bus, 2000.
- [3] J. J. Nejedlo, IBIST™ (Interconnect built-in self-test) architecture and methodology for PCI Express: Intel's next-generation test and validation methodology for performance IO," Proceedings International Test Conference 2003, Sept.-Oct. 2003, pp. 784 – 784.
- [4] S. S. Chung, S. H. Baeg, "AC-JTAG: Empowering JTAG beyond Testing DC Nets," Proceedings Of International Test Conference 2001, Oct.-Nov. 2001, pp. 30-37.
- [5] IEEE Std 1149.6-2003: 1149.6™ IEEE Standard for Boundary Scan Testing of Advanced Digital Networks, Apr. 2003.
- [6] K. Parker, The Boundary-Scan Handbook, Third Edition, Kulwer Academic Publishers, Jun. 2004.
- [7] S. Vandivier, M. Wahl and J. Rearick, "First IC validation of IEEE Std 1149.6," Proceedings of International Test Conference 2003, Sept.-Oct. 2003, pp. 79 – 86.
- [8] B Eklow, C Barnhart, M. Ricchetti, and T. Borroz, "IEEE 1149.6 – A Practical Perspective," Proceedings of International Test Conference 2003, Sept.-Oct. 2003, pp. 494-502.
- [9] I Duzevik, "Design and Implementation of IEEE 1149.6," Proceedings of International Test Conference 2003, Sept.-Oct. 2003, pp. 87-95.
- [10] J. Musicer and J. Rabaey, "An Analysis of MOS Current Mode Logic for Low Power and High Performance Digital Logic," Proceedings ISLPED 2000, Jul. 2000.