Integrating Boundary Scan into Multi-GHz I/O Circuitry

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Abstract

A minimally invasive solution for adding boundary scan to high-speed I/O circuits is described. The insertion of boundary scan registers on the transmit side is done in the lower-speed parallel domain, while the boundary scan registers on the receive side is done using the techniques described in IEEE Std 1149.6 in the high-speed serial domain. Special clocking requirements are described, and results from actual silicon testing are presented that demonstrate negligible impact on functional performance while maintaining compliance with the both 1149.1 and 1149.6 standards.

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1. Introduction

The external interfaces of integrated circuits (ICs) have been experiencing two trends of great interest to test engineers: significantly improved testability due to IEEE standards under the 1149 umbrella, and significantly increased performance requirements as system speeds and bandwidths grow. Unfortunately, the latter trend poses a threat to the former, as designers may be tempted to jettison testability in favor of performance. A prime example of this conflict is illustrated in very high speed interfaces such as SerDes (Serializer/Deserializer) channels which operate in the GHz range. Traditional boundary scan techniques embodied in IEEE 1149.1 [1] and even advanced boundary scan techniques embodied in IEEE Std 1149.6 [2], when applied indiscriminately, can degrade the mission performance of such high speed I/Os. Fortunately, creative application of the 1149 standards is possible, allowing both performance and testability goals to be achieved.

After providing a brief background on both boundary scan and high speed I/O, this paper describes the source of the performance impact of traditional boundary scan, followed by a description of a creative solution which minimizes performance impact while preserving compatibility with the 1149 standards. A description of the actual silicon implementation of this solution is given, along with test results demonstrating the achievement of both performance and testability objectives.

2. Background

2.1 Boundary Scan

The As physical access to the pins of devices and the interconnect between devices on printed circuit boards (PCBs) was reduced with the advent of surface-mount devices and multi-layer PCBs, visionary members of the test community organized a Joint Test Action Group that ultimately led to the codification of boundary scan testing in IEEE Std 1149.1. The principle behind boundary scan testing of a PCB is to add test circuitry internal to the ICs on the board, and to use that test circuitry to exercise the interconnections between ICs. The 1149.1 standard specifies that scan-based control and observe points be added to the I/O pins of the ICs, that these scan registers are connected to form a boundary scan chain, that this scan chain is accessed via a Test Access Port (TAP) with a standard set of instructions, and thus enables chip-to-chip interconnect testing without direct physical access to the pins of a chip. Figures 1a and 1b show a simplified view of a bi-directional I/O pin before (a) and after (b) the addition of 1149.1 boundary scan.

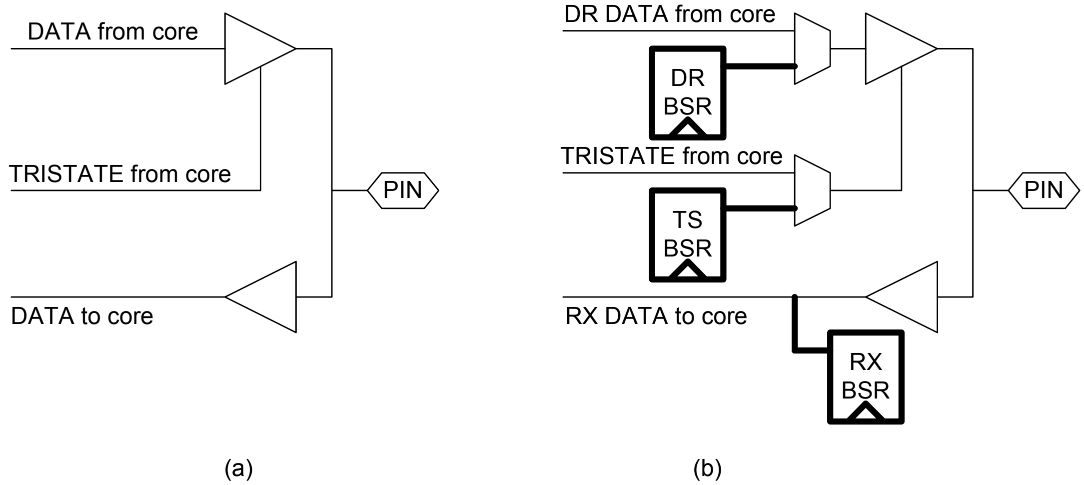

Figure 1 **Adding 1149.1 Boundary Scan to a Bidirectional I/O Pin**

With the added circuitry in Figure 1b, this I/O is now able to:

- Drive either digital value to the pin from the boundary register labeled DR BSR (the EXTEST instruction).
- Tristate the pin via the boundary labeled TS BSR.
- Sample the value received from the pin in the boundary register labeled RX BSR.

Though the pin may have been capable of performing these operations via the functional logic inside the chip, this additional circuitry greatly simplifies the creation of board-level interconnect tests by bypassing the internal logic and using the standard instructions and interface specified in IEEE Std 1149.1.

Two shortcomings of IEEE Std 1149.1 are its inability to handle AC-coupled nets and its poor detection of faults on differential nets. These issues are addressed by IEEE Std 1149.6, which builds upon the foundation of 1149.1 but adds additional circuitry for edge-based testing (beyond DC level-based testing) of AC-coupled nets as well as dual single-ended treatment of differential receivers. Figures 2a and 2b show a simplified view of a differential channel before (a) and after (b) the addition of 1149.6 boundary scan. Note that section 6.2 of IEEE Std 1149.6 specifies the use of dedicated test receivers (labeled "testrx" in Figure 2b) with hysteretic comparators prior to the boundary scan registers; these allow reconstruction of the driven waveform on AC-coupled nets.

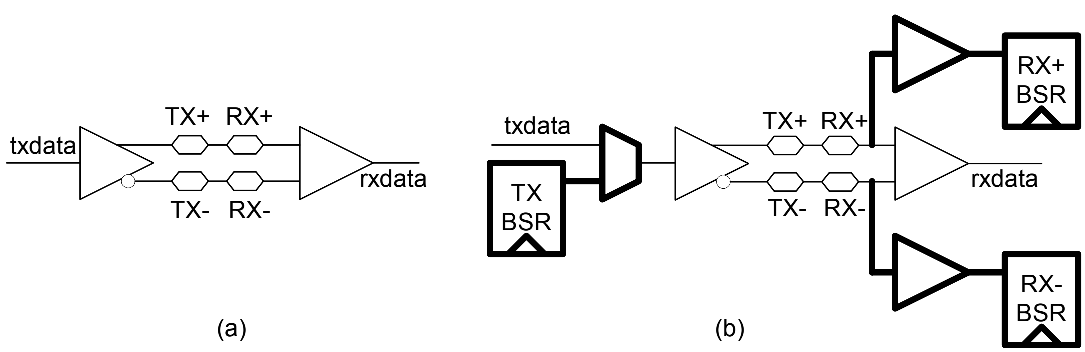

Figure 2 **Adding 1149.6 Boundary Scan to a Differential Channel**

With the added circuitry in Figure 2b, the ends of this channel are now able to:

- Drive either pulse polarity to the TX pins from the boundary register labeled "TX BSR" (the EXTEST_PULSE instruction).
- Drive a series of pulses to the TX pins from the boundary register labeled "TX BSR" (the EXTEST_TRAIN instruction).
- Capture the direction of the last edge (rising or falling) received from the RX pins in the boundary registers labeled RX+ BSR and RX-BSR.

2.2 High Speed I/O

Given the need for high bandwidth communication between chips on PCBs, and in light of the real estate issues associated with large numbers of parallel traces along with the clock synchronization problems at high data rates, it is becoming more common for ICs to employ high-speed serial links running at GHz frequencies with embedded clocking to carry data. These data streams are created by the parallel-to-serial conversion on the transmitting IC, with an associated increase in speed, and resolved by serial-to-parallel conversion on the receiving IC with a complementary decrease in speed. Figure 3 shows a highly simplified view of the parallel-to-serial conversion on the transmit side.

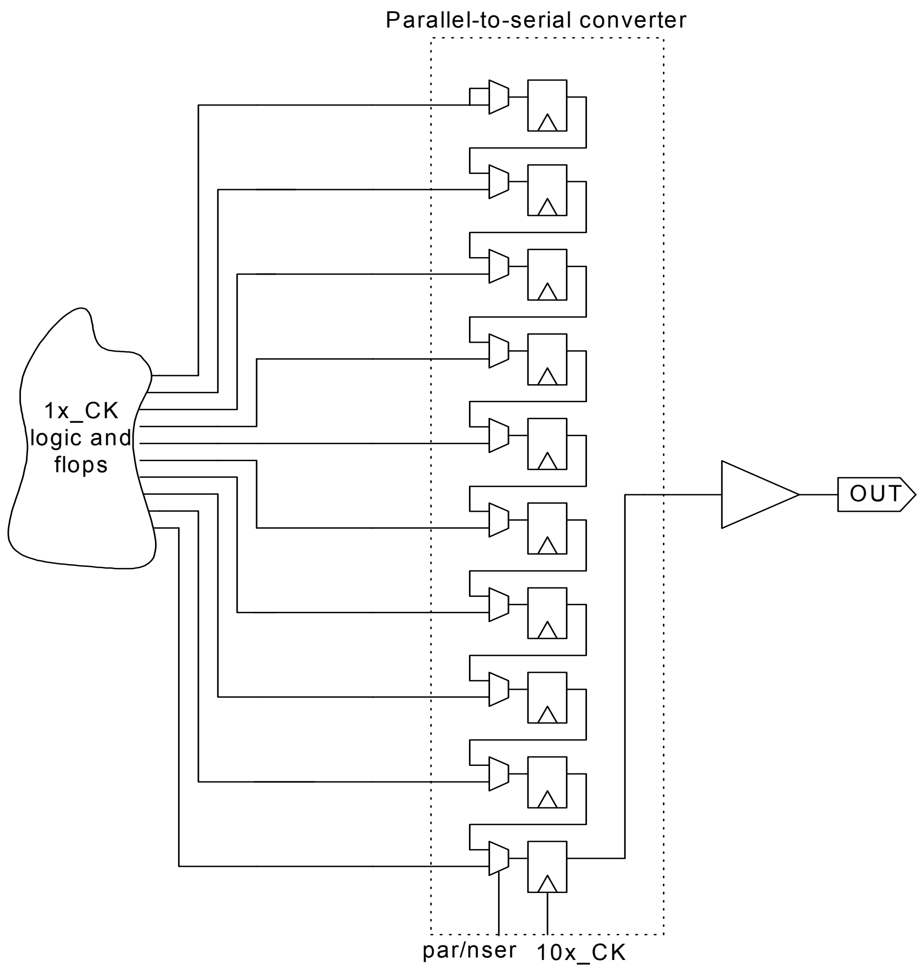

Figure 3 Simplified Schematic for High Speed Serializer Outputl

Particular attention should be paid to the implicit clock domain crossing in the parallel-to-serial converter: the left side of the figure is running in the 1X_CK domain, while the serial shift register inside the parallel-to-serial converter runs, in this example, at ten times the frequency (in the 10X_CK domain). This results in very high speed operation in the serial domain, and thus imposes extreme design constraints which can make the addition of test circuitry unacceptable.

3. Problems with Traditional Boundary Scan Insertion

The addition of the boundary scan hardware to a chip pin, as shown in Figure 1, will unmistakably affect the performance of the original circuit: there is an additional multiplexer delay in series with the driver data (as well as the tristate control), and there is an additional fanout and load on the receiver. Concentrating on the driver side, and keeping in mind the very challenging performance requirements for high-speed serial outputs, it becomes clear that adding boundary scan in the serial domain may impose too large a penalty on the mission mode operation of the output to be practical. For example, a common serialized data rate is 3.125 GHz, with a corresponding period of 320 pS. The delay through a the added multiplexer alone could consume a substantial portion of that period, and the additional logic can only exacerbate problems with jitter. Of course, there are many possible implementations of serial driver circuitry beyond this simplistic example, but the point remains that adding test hardware in the high speed domain is problematic. Fortunately, there is a clever alternative that avoids this issue altogether.

3.1 Driver-Side Boundary Scan Insertion in the Parallel Domain

The placement of the output boundary scan register just in front of the driver is not mandated by IEEE Std 1149.1; it is merely illustrative. The intent is simply that the value placed in the boundary scan register will be reflected on the pin during EXTEST. Indeed, the standard allows for an arbitrary analog circuit to exist between the boundary register and the pin (see Figure 10-7 of IEEE Std 1149.1-2001). Though the parallel-to-serial converter described above may appear to be largely digital in nature, it can be treated as an encapsulated analog circuit for the purposes of creatively applying the standard. Taking that line of reasoning to its natural conclusion results in the idea of placing the boundary scan register in the parallel domain, as shown in Figure 4.

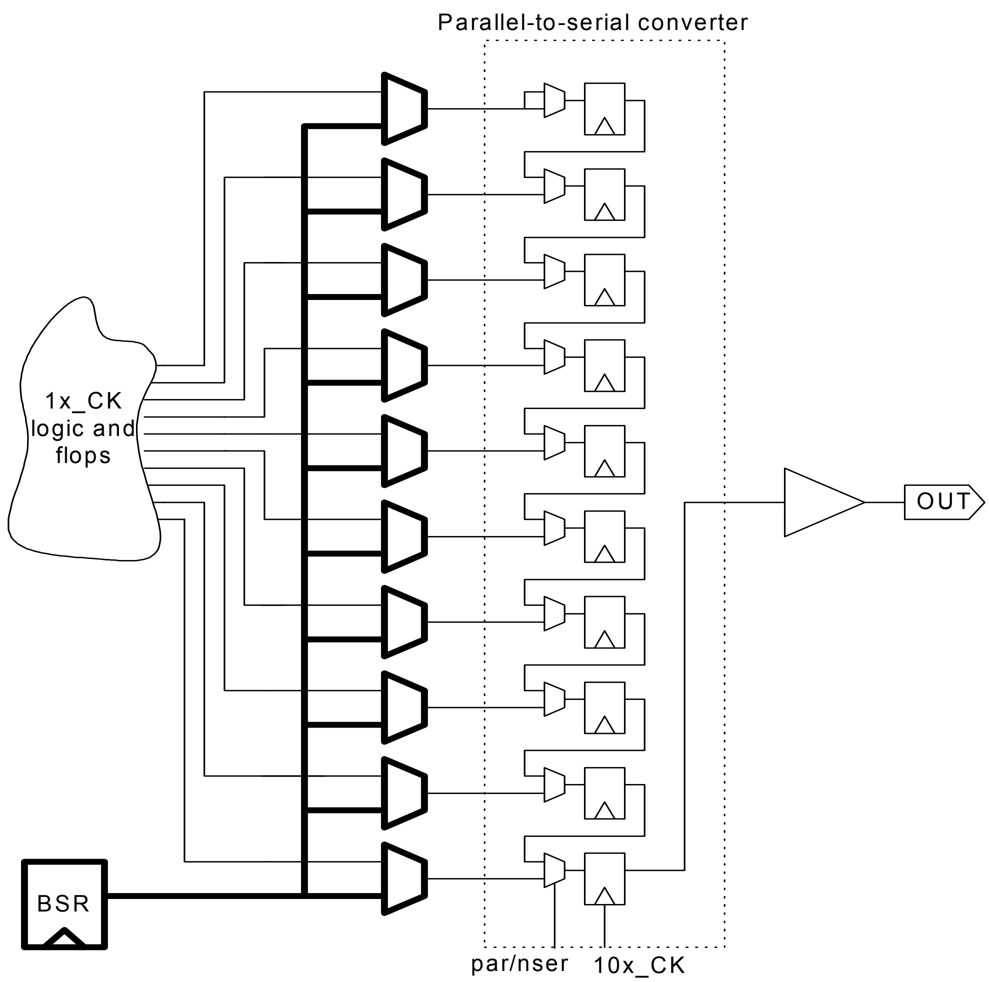

Figure 4 **Addition of Boundary Scan to Parallel Domain of Transmitter**

The fundamental tradeoff here is in space vs. time: adding boundary scan costs 10 times more multiplexers in the parallel domain as it would in the serial domain, but each mux can be absorbed in a clock domain with 10 times the period. It is important to note that there are not 10 times more boundary scan registers: the standard mandates a 1-to-1 correspondence between a boundary register and a pad. The operation of this circuit is simple, though nonsensical in terms of the mission mode: the single value in the boundary scan register is copied to all of the parallel inputs (10 in this example), then serialized and presented as a high-speed stream of (constant) values, cycle after cycle. This high-speed stream of constant values in indistinguishable from DC, and thus satisfies the requirements of boundary scan.

One very important point requires mention here: this placement of the boundary scan register requires the parallel-to-serial converter to be operational during boundary scan testing, which implies that the clocks used in that portion of the circuit must be running. At first glance, this may appear to be a violation of the intent of IEEE Std 1149.1, in that there should be no functional dependencies on the chip to perform an EXTEST operation. However, there are two reasonable responses to this challenge. First, many types of I/O circuits require some pre-conditioning before they will operate, and it is not uncommon to include a "design warning" section in the BSDL for a chip containing such I/Os that spells out the preconditions for performing boundary scan, which, in this case, would include the recipe for providing the appropriate clocking. Second, and more in line with the standard, because most parallel-to-serial converter circuits employ a phase-locked loop (PLL) to generate the high-speed clocks, a free-running oscillator which requires no external clock reference could be used as the source of the PLL reference clock during boundary scan test. Though the frequency and phase of such an oscillator are not precisely controlled and would not work in mission mode, the considerably relaxed data required for boundary scan (namely DC 0 and 1) are frequency- and phase-independent. Thus, no functional dependency on chip logic exists for EXTEST operation; the "analog circuit" allowed between the boundary scan register and the pin includes the autonomous clock generator.

The alert reader will doubtless have realized that the placement of the boundary registers in the parallel domain requires that a considerable amount of circuitry be operational in order to perform the simplest boundary scan test. That is certainly true, but should not be treated as either a violation of the standard (it is not) or as a large weakness of this approach; indeed, it may be argued that a successful boundary scan test demonstrates that not only the interconnect is functional but a sizeable portion of the IC still is as well. Assuming that the IC was fully tested at the component level and has not suffered an early life failure, a failing boundary scan test can still be diagnosed as an interconnect problem, though it is fair to say that there is a marginal increase in the probability that the IC may be suspect compared to a boundary scan implementation closer to the pins.

The final item to note about the placement of the driver-side boundary register in the parallel domain is that the modifications specified by IEEE Std 1149.6 for edge generation are exactly the same as they would be were the boundary register placed in the serial domain.

3.2 Receiver-Side Boundary Scan Insertion via IEEE Std 1149.6

Integrating boundary scan on the receiver side of a high-speed link is a somewhat simpler problem than for the driver side. The arguments that justify the placement of the driver-side boundary scan register in the parallel domain are not symmetrical with the receiver side, nor is the performance penalty (another fanout) as great, nor is the function of the serial-to-parallel converter circuitry as amenable to simulated DC operation. Specifically, one of the key operations performed on an incoming high-speed data stream by a receiver is clock recovery, whereby the (regularly forced) transitions in the data are used to infer the clock used in the downstream serial-to-parallel converter circuitry. With the constant DC values present during boundary scan testing, there is no clock to recover. Though another clock could be injected for this purpose, this is not generally a native element in the receiver, as it was in the driver. Given all this, it is not necessary to place the receiver-side boundary scan registers in the parallel domain; in fact, for differential channels (which are very common in high-speed I/O), it is not even desirable.

Most importantly, the subject of receiver-side boundary scan for advanced I/Os like these high-speed serial links has been thoroughly examined and specified in IEEE Std 1149.6. This new standard details the design of a test receiver capable of both edge detection for AC-coupled nets as well as level detection for traditional DC-coupled nets (as would be tested by 1149.1). These test receivers are placed in parallel with the mission receivers, and are thus in the serial domain for the types of I/Os described here. Simulations and actual silicon measurements indicate that the presence of the test receivers causes negligible impact on mission-mode performance.

4. Silicon Implementation and Results

The complete boundary scan implementation shown in Figure 5 was implemented in 0.13 micron, 1.2V test chip with several differential transmit/receive pairs, first described in [3]. The nodes labeled as TX+, TX-, RX+, and RX- represent the test points measured.

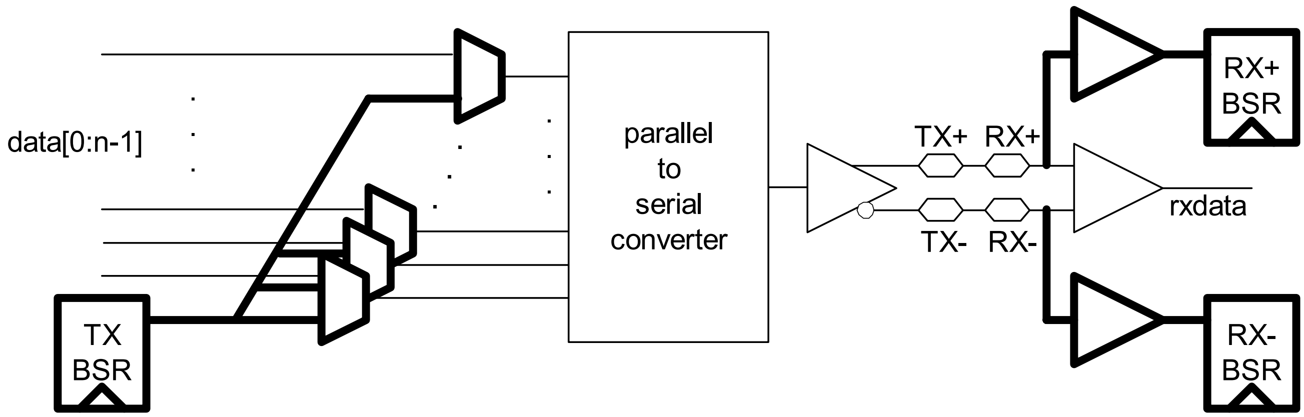

Figure 5 Complete Boundary Scan Implementation for SerDes Channel

The boundary scan test results on actual silicon for level-based DC EXTEST are shown in Table 1, and the results for edge-based EXTEST_PULSE appear in Table 2

Table 1 DC EXTEST –Level Results

Test driving levels TX+ TX-	DC-coupled captured data RX+ RX-	AC-coupled captured data RX+ RX -
01	01	VV
10	10	VV

The "VV" notation in Table 1 indicates that the initialized value (V) in the test receiver was not changed during EXTEST when the driver was AC coupled to the receiver; this is exactly the expected behavior, because the coupling capacitor blocks the DC level.

Table 2 EXTEST_PULSE – Edge Results

Driving TX+ TX- transitions	On-board AC-coupled captured data RX+ RX-	On-chip AC-coupled captured data RX+ RX -
01 to 10	10	10
10 to 01	01	01

In addition to the verifying the correctness of all boundary scan operations (both 1149.1 and 1149.6), the tests also showed that the mission performance of the serial links was as expected and unaffected by the addition of the boundary scan circuitry.

Jitter introduction on the driver side is by definition zero, since the serialized data goes through a retiming process in the 10X_CK domain. As long as the additional multiplexer delay associated with the addition of the boundary scan cell in the parallel domain is accounted for in static timing analysis, there will be no impact on the functional performance of the high speed transmitter. Indeed, the measured jitter on the actual silicon (about 20 pS peak-to-peak worst case) has been traced back exclusively to clock duty cycle and noise issues in the serial domain, which have nothing to do with the boundary scan circuitry. On the receiver side, the high input impedance of the test receivers added a negligible additional load beyond the mission receivers. Overall, the test chip was a resounding success in demonstrating not only the first silicon implementation of 1149.6, but also the workability of placing boundary scan in the parallel domain of the transmitter and adding the test receiver to the serial domain of the receiver.

5. Conclusions

Despite the ostensible impossibility of adding boundary scan to GHz-speed I/Os, this paper has demonstrated not only a viable circuit design for both the driver and receiver portions of such a circuit, but presented successful results from actual silicon. The key innovations were the placement of the driver-side boundary scan register in the parallel domain in order to minimize impact on the high-speed section and the use of 1149.6 test receivers in the serial domain. Not only did this approach achieve correct implementation of boundary scan, it also resulted in negligible impact on the mission-mode operation of the high-speed serializer/deserializer circuitry.

6. References

[1] IEEE Std 1149.1-2001, "IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE, USA, 2001.

[2] IEEE Std 1149.6-2003, "IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks," IEEE, USA, 2003.

[3] Vandivier, Wahl, and Rearick, "First IC Validation of IEEE Std 1149.6", *Proc. International Test Conference*, 2003, pp. 632-639