# Timing Accuracy Enhancement by a New Calibration Scheme for Multi-Gbps ATE

Masashi Shimanouchi
Credence Systems
150 Baytech Drive, San Jose, CA 95134-2302
masashi_shimanouchi@credence.com

## Abstract

*The ever increasing data rate of high speed I/Os has required higher test timing accuracy. In order to keep improving ATE's edge placement accuracy, we have reviewed the traditional timing calibration methods in detail, and studied the timing error mechanism. Then we have developed a new calibration scheme to overcome the fundamental issues in some traditional calibration methods. Our main focus in this paper is on the following three areas: data dependent jitter (timing error), pin-to-pin skew and calibration at DUT.*

## 1 Introduction

As the speed of device I/Os has increased from several hundreds Mbps to multi-Gbps, detailed studies of the ATE-DUT interface have started to move beyond the simple transmission line concept. The subjects of such endeavors in recent years are categorized as follows:

- Loadboard Design
- DUT-path Analysis (ATE + Loadboard)
- Loadboard (+Test Socket) Tpd Calibration by TDR
- ATE and DUT Loading Effect Calibration
- Test Methodology (DV, HVM).

In order to design a high-quality, high-speed loadboard, the use of insertion loss and return loss in frequency domain[1][2] and eye diagram in time domain[2][3] has become necessary for simulation and characterization measurements. Several timing error sources in the DUT-path between the ATE driver/comparator and DUT I/O pin were discussed[3][4][5], and a simple simulation model was proposed[4] to estimate proper calibration values associated with those errors, including ATE and DUT I/O characteristics. Since TDR has been most frequently used for loadboard propagation delay calibration, TDR error was the concern of many authors[4][5][6]. Because overall timing error in device testing is not only due to the ATE-DUT interface but also due to the ATE itself, inherent error sources and their error amount in an ATE was studied[7]. Considering such error sources and currently available test technology, a test methodology was proposed for various test needs such as design validation (DV) and high volume manufacturing test (HVM)[6]. As an extension of the test community's endeavor toward higher test timing accuracy briefly described above, we have reviewed our traditional timing calibration methods in detail, and developed a new calibration scheme to address some of the remaining timing error sources. This paper consists of two main parts and one appendix as follows.

- The basic deskew calibration method is acceptably accurate to calibrate the same speed grade ATE pins at the driver/comparator junctions if data dependent timing error/jitter (DDJ) is negligibly small. DDJ is, however, one of the major error sources in multi-Gbps testing, and, therefore, it needs to be calibrated out for higher timing accuracy[8][9]. For DDJ calibration, at-speed calibration measurement is essentially required, and, therefore, the current calibration method, which necessitates calibration measurements at low speed, is not applicable.
- A propagation delay calibration measurement of the loadboard with test socket by TDR is essentially inaccurate, and, therefore, a new method other than TDR is required for higher timing accuracy. One practical solution today is to use advanced DUT-path component modeling and circuit simulation. Once the calibration values are obtained from the simulation, they need to be combined with the other calibration values obtained by physical calibration measurements to move the calibration reference points to DUT.
- An intolerable amount of timing error could be caused by multiple reflection[3]. Since it could impose a limitation on our currently implemented DDJ calibration method, depending on its location, impedance discontinuities in our timing-critical signal paths need to be small enough not to cause large timing error. However, it is not easy to tell how small they should be, while it is easy to demand too much. An attempt to come up with such requirement specification in frequency domain (i.e. in terms of "return loss") is discussed in Appendix using a simple example to clarify the basic idea.

In the following section 2, we review our traditional calibration method and discuss where and why there are essential limitations for higher timing accuracy, convincing us of the necessity to investigate alternative calibration methods. In the section 3, we discuss two new calibration methods: DDJ calibration, and use of signal path modeling and circuit simulation.

Timing jitter and timing error are interchangeably used in this article. Since timing accuracy in multi-Gbps DUT testing is of our primary concern, 50 ohm termination at both ATE driver/comparator ends and DUT I/O ends is assumed in this article.


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## 2 Traditional Timing Calibration

### 2.1 Traditional Timing Calibration Scheme

To test a device, an ATE uses its drivers to generate stimuli to DUT, and its comparators to evaluate DUT outputs by strobing and comparing them against expected data. As illustrated in Fig.1, a global time zero reference is assumed somewhere in an ATE, and both drive-side data generation timing and compare-side data strobe timing are to be calibrated with respect to the global time zero reference.

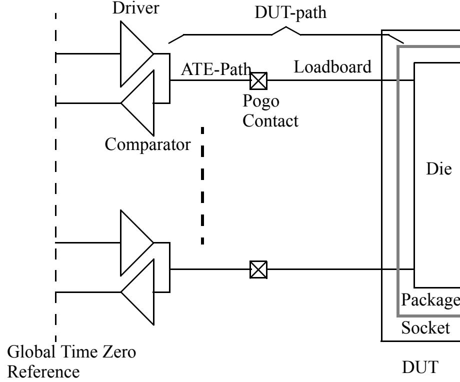



Fig.1 ATE Timing Paths to Calibrate

The architecture of our traditional timing calibration scheme is illustrated in Fig.2. The timing alignment (i.e. deskew calibration) of stimuli generation and data strobing at DUT I/O pins is done in three steps as follows.

- First, drive-side timing and compare-side timing of all the required pins for all the possible event types (drive high/low, strobe high/low etc.) are calibrated at the driver/comparator junctions of those pins.
- Second, the propagation delay between each driver/comparator junction and corresponding DUT socket pin is measured by TDR, and the calibration point is moved from each driver/comparator junction to the DUT pin.
- Third, the propagation delay is further adjusted for drive-side considering driver output voltage swing and DUT input capacitive loading effect.

Several calibration values, each representing a physically different signal path (e.g. loadboard) or different signal integrity effect (e.g. DUT input loading) are algebraically added to provide the final deskew calibration value.

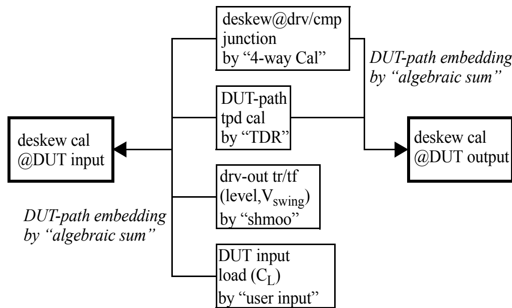


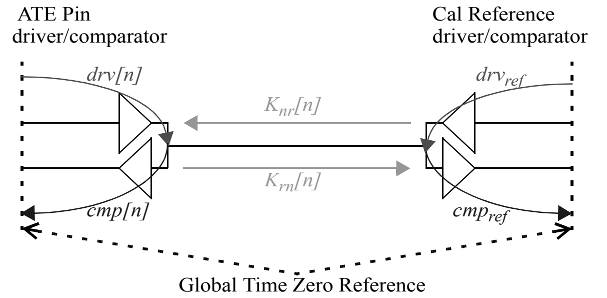

Fig.2 Traditional Timing Calibration Scheme

### 2.2 Timing Error in Traditional Calibration

Driver output impedance is 50 ohm nominal and comparator input is terminated by 50 ohm nominal even if they are not explicitly shown in the pictures throughout this paper.

#### 2.2.1 4-Way Deskew Calibration

Deskew calibration at each driver/comparator junction is based on the four independent calibration measurements as shown in Fig.3, and they are expressed by (Eq.1) through (Eq.4). Each of our EXA family ATE has one dedicated reference driver/comparator for the timing calibration use, and all the other pins are to be calibrated using the reference driver/comparator.




$$\begin{cases} m1[n] = drv[n] + cmp[n] & \text{(Eq.1)} \\ m2[n] = drv_{ref} + cmp_{ref} & \text{(Eq.2)} \\ m3[n] = drv[n] + K_{rn}[n] + cmp_{ref} & \text{(Eq.3)} \\ m4[n] = drv_{ref} + K_{nr}[n] + cmp[n] & \text{(Eq.4)} \end{cases}$$

Fig.3 4-Way Calibration Measurements

Using the calibration measurement results expressed by (Eq.1) through (Eq.4), all the pin-to-pin timing variation with respect to the reference pin can be obtained as expressed by (Eq.5) for drive-side and as expressed by (Eq.7) for compare-side. Assuming that the propagation delay between the driver/comparator junction of each tester pin and the one of the reference pin does not depend on signal propagation direction, all the pin-to-pin timing variation can be completely obtained from the calibration measurement results as expressed by (Eq.6) and (Eq.8).

$$drv[n] - drv_{ref}$$

$$= \frac{(m1[n] - m2[n]) + (m3[n] - m4[n])}{2} + \frac{K_{nr}[n] - K_{rn}[n]}{2} \quad \text{(Eq.5)}$$

$$= \frac{(m1[n] - m2[n]) + (m3[n] - m4[n])}{2} \quad \text{(Eq.6)}$$

*(if $K_{nr}[n]$-$K_{rn}[n]=0$)*

$$cmp[n] - cmp_{ref}$$

$$= \frac{(m1[n] - m2[n]) - (m3[n] - m4[n])}{2} - \frac{K_{nr}[n] - K_{rn}[n]}{2} \quad \text{(Eq.7)}$$

$$= \frac{(m1[n] - m2[n]) - (m3[n] - m4[n])}{2} \quad \text{(Eq.8)}$$

*(if $K_{nr}[n]$-$K_{rn}[n]=0$)*

Since this assumption is not valid in general, calibration error could occur. The primary cause of propagation delay dependency on signal propagation direction is the different capacitive loading at both ends as illustrated in Fig.4. The different rise/fall time of the tester pin driver and the reference driver is secondary. As shown in Fig.5, driver-output edge-speed is slowed by lossy transmission line first, and it is further slowed at each comparator input by the capacitive loading. When the speed grade of the tester pin is not the same as the one of the reference driver/comparator, the amount of the capacitive loading at both ends is different which causes the propagation delay dependency on signal propagation direction to result in calibration error.

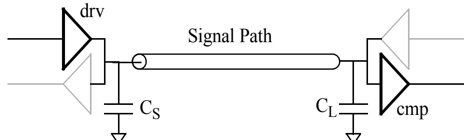



Fig.4 Capacitive Loading at Both Ends

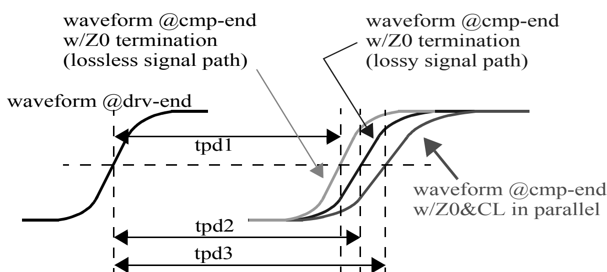



Fig.5 Edge Slowing by Lossy T-line and Comparator Input Loading

Tester pin to tester pin skew, however, is our actual concern. If all the tester pins of our interest have the same amount of error with respect to the reference driver, it does not affect the timing alignment accuracy among tester pins. When the same speed grade ATE pins are to be calibrated, the deskew calibration at the driver/comparator junction becomes acceptably accurate because their capacitive loading variation is small. The real limitation of the 4-way calibration method arises from its implementation. At multi-Gbps data rates, DDJ is one of the major timing error sources. Since all the tester pins need to be connected to a single reference driver/comparator, the frequency bandwidth of those signal paths is not wide enough. Therefore, DDJ occurs in practice.

### 2.2.2 DUT-path Propagation Delay Calibration by TDR

Actual timing error in loadboard calibration using ATE's TDR capability is caused not only by TDR methodology but also by each ATE's inherent error mechanism such as signal path quality, comparator bandwidth, timing measurement accuracy etc. Therefore it is possible to find an empirical rule for a specific ATE such as "Open Pogo Shorted DUT[6]" that seems to minimize the calibration error because error by TDR methodology itself could be accidentally compensated by an ATE's inherent error to some extent. As discussed below, TDR methodology itself is essentially inaccurate, and, therefore, we have to investigate alternative calibration methods. We examine four scenarios as shown in Fig.6 through Fig.9. Actual loadboard with socket calibration is a combination of some of these scenarios.

- Fig.6 Comparator Input Loading: When the reflected signal arrives at the comparator input, the edge is slowed by the capacitive loading, which does not happen in forward signal transmission, and results in measurement error.
- Fig.7 Lossy Signal Path: The incident edge is slowed during forward signal transmission, and it is further slowed in backward signal transmission, resulting in measurement error.
- Fig.8 Open TDR: Since the parasitic capacitance of the socket end (C2) is in parallel with 50 ohm termination during device testing, effectively reducing time constant, open TDR overestimates propagation delay.
- Fig.9 Shorted TDR: Since shorting the socket end to ground removes the socket end parasitic capacitance (C2) during calibration, effectively reducing time constant, shorted TDR underestimates propagation delay.

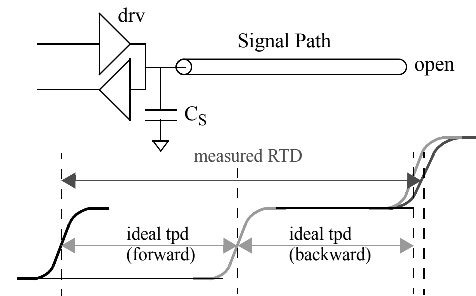



Fig.6 Comparator Input Loading Effect on TDR Accuracy

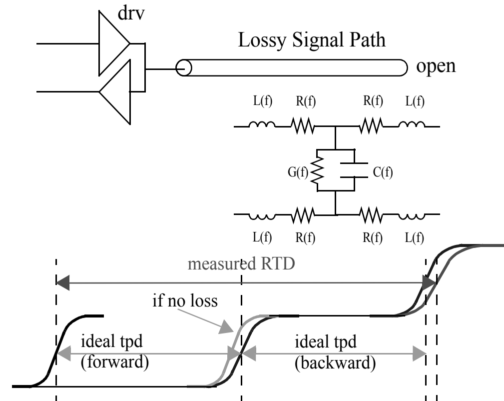



Fig.7 Lossy Signal Path Effect on TDR Accuracy

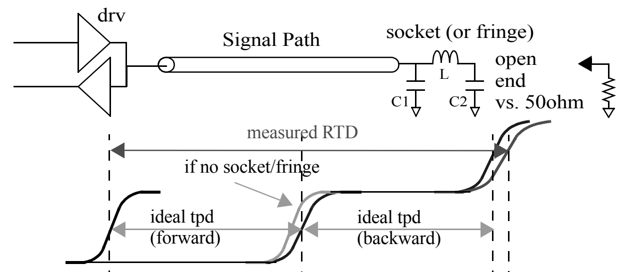



Fig.8 Open TDR Error Mechanism with Socket

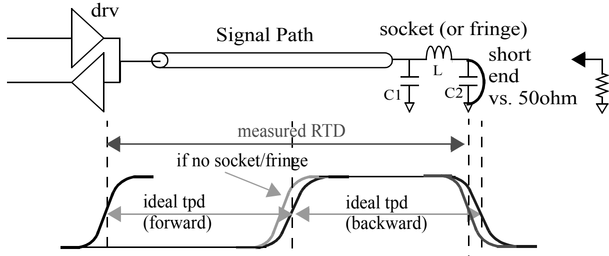



Fig.9 Shorted TDR Error Mechanism with Socket

### 2.2.3 Driver Output Rise/Fall Time vs. Voltage Swing

While timing calibration is done at one voltage swing, tester pin output timing varies depending on its output voltage as illustrated in Fig.10. In order to correct the voltage swing dependent timing error, the rise/fall time of the tester pin output for various voltage swings is measured and used for the calibration. Since this calibration measurement is done by the reference comparator discussed in the section 2.2.1, the calibration error amount depends on the difference in signal degradation between the calibration condition and actual device test environment.

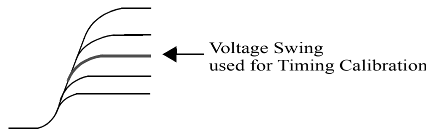



Fig.10 Driver Output Timing Variation vs. Voltage Swing

### 2.2.4 DUT Input Loading Effect

In order to calibrate the timing error due to the capacitive loading at DUT input, a simple calibration is provided as an option asking an ATE user to specify the loading capacitor value. Stimulus waveform at DUT input is approximated by the step response of a low pass filter as illustrated in Fig.11 and expressed by (Eq.9). The additional delay due to the capacitive loading at 50% voltage swing is expressed by (Eq.10) and (Eq.11). Since this method is based on a very primitive "rule of thumb", it's not very accurate.

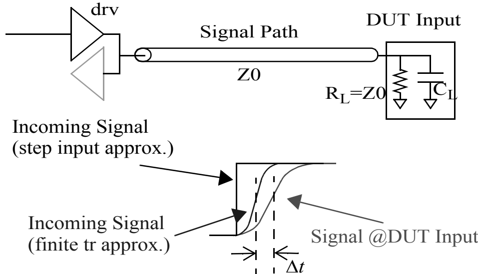



Fig.11 DUT Input Loading Effect on Stimulus Timing

$$v_{DUTin}(t) = V_0\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] \quad \text{(Eq.9)}$$

$$\Delta t = -\tau \times \log_e(0.5) \quad \text{(Eq.10)}$$

$$\tau = \frac{Z0}{2} \cdot C_L \quad \text{(Eq.11)}$$

## 3 New Timing Calibration Scheme

### 3.1 Overview

Utilizing jitter analysis methodologies, we had studied our ATE's timing accuracy from the view point of high-speed serial communication device test and identified various jitter components[7]. In order to further expand it to include timing skew among multiple tester pins and DUT I/O characteristics, the associated timing error components need to be added. These timing error components in testing a wide variety of devices at multi-Gbps are summarized in Fig.12.

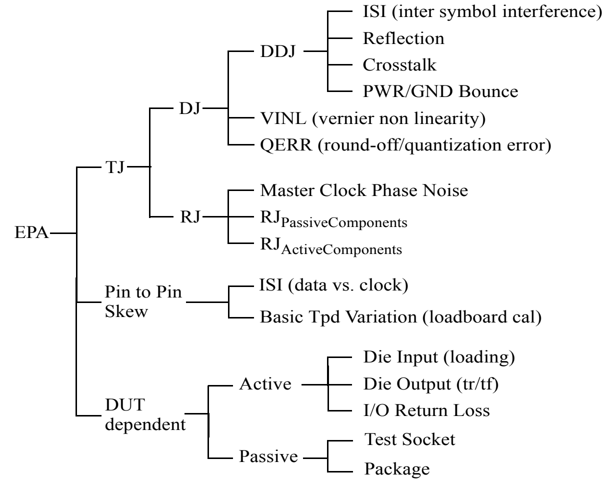



Fig.12 Timing Error/Jitter Categories and Sources

Having considered the timing error/jitter sources shown in Fig.12 and the fundamental limitation in the traditional calibration scheme discussed in the section 2.2, we have developed a new timing calibration scheme as illustrated in Fig.13. This is an additional calibration for higher timing accuracy at multi-Gbps testing. The traditional calibration scheme with incremental accuracy improvement from time to time is still our foundation. The new timing calibration scheme has four distinctive features as follows.

- Pin-to-pin skew reduction is achieved not only at low data rate but also at actual device test speed. This means that DDJ calibration is performed, which requires both HW and SW support for this new calibration implementation.
- Drive-side deskew calibration is done first, using a very wide frequency bandwidth oscilloscope (>20GHz) either at a pogo pin or a socket mounting pad on a DUT specific loadboard. A pogo pin is the default calibration point because of its universal availability, and socket mounting pad is optional depending on the DUT pin assignment.
- Compare-side deskew calibration is done using the already calibrated drive-side signal, reducing the calibration time and the cost of the calibration reference, i.e. a known good pattern generator. The calibration measurement point is limited to the pogo pin for the moment.
- In order to move the deskew calibration point from pogo pin or socket mounting pad toward DUT, propagation delay and DDJ between the physical calibration point and the target calibration point is derived by circuit simulation, and then combined with physically measured calibration values.

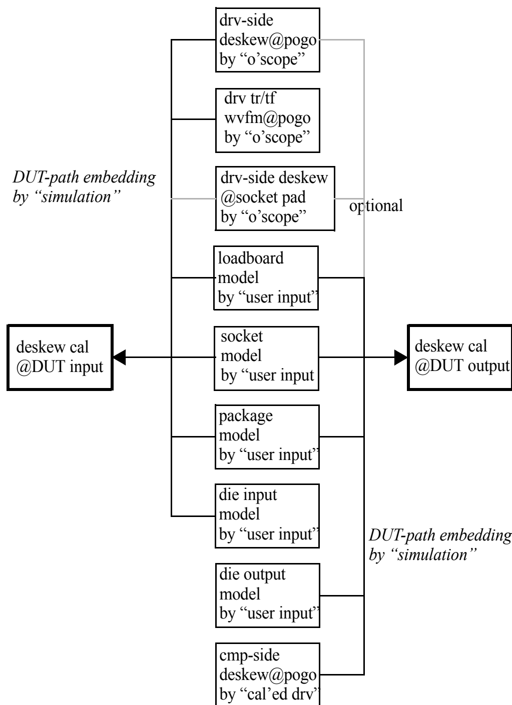



Fig.13 New Timing Calibration Scheme

## 3.2 Data Dependent Calibration

We have developed data dependent calibration (DDC) to reduce data dependent timing error/jitter in our ATE for both drive-side and compare-side considering not only the current event type but also the previous bit patterns.

### 3.2.1 Example Simulation Results with K28.5 Bit Pattern

In order to discuss how DDC works, let us use some simulation results in this paper. The simulated circuit consists of three stages of packaged high speed buffers using bipolar transistor technology with lossy interconnects between them. Since K28.5 pattern[12] is often used for DDJ evaluation of telecom/datacom physical layer components and it contains a variety of bit patterns in only 20 bits duration, we use this pattern for our discussion. The input and output waveforms are shown in Fig.14 where 1 UI is 300ps.

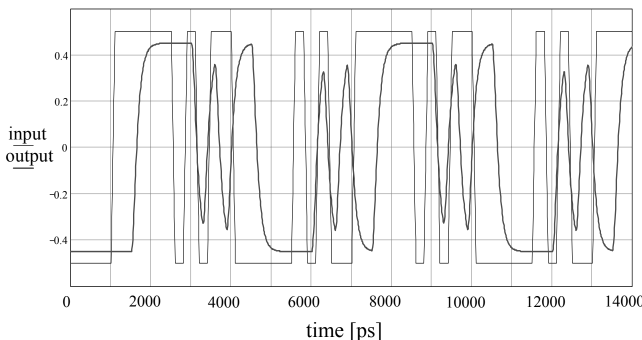



Fig.14 Input and Output Waveforms with K28.5 Pattern

The eye diagram of the output waveform is shown in Fig.15, where one can notice about 35ps DDJ. Note that this DDJ is caused by not a single path segment but a cascading of several stages including both passive and active circuits[7].

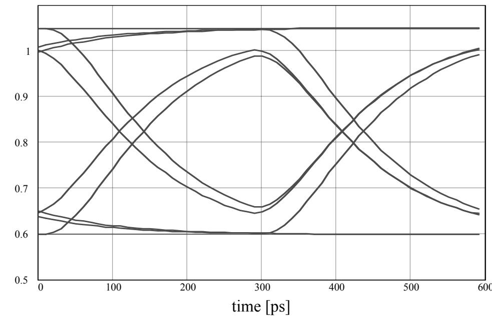



Fig.15 Output Eye Diagram with K28.5 Pattern

### 3.2.2 Calibration Measurements for DDC

Since the DDC implementation on our ATE hardware can take into account three previous bits, there are sixteen bit patterns to consider to determine the calibration value for each event. As DDJ becomes critical only when the current event is different from the previous event, there are only eight 4-bit patterns necessary for the calibration. This is illustrated in Fig.16, where the mapping between the calibration values (cal-1, cal-2,...) and the corresponding bit patterns is shown.

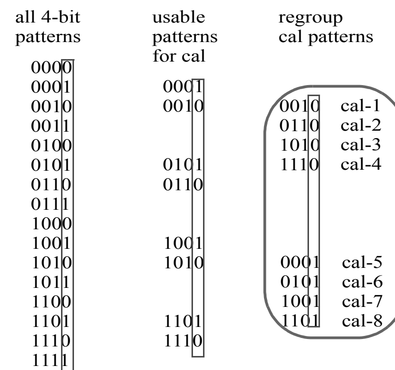



Fig.16 Bit Patterns Used for Data Dependent Calibration

While the hardware takes into account three previous bits, four previous bits are considered in the calibration measurements, using the average of the corresponding two measurement results to determine each cal-x value (x=1,2,...8). Three examples of calibration measurements are shown in Fig.17 through Fig.19. Each figure shows two calibration patterns with the measured (simulated) calibration values used to obtain one calibration value. Negative value means that the actual edge transition timing was earlier than ideal. Therefore, the corresponding edge should be intentionally delayed at the timing generator by this amount for drive-side or strobed earlier for compare-side to compensate for the DDJ.

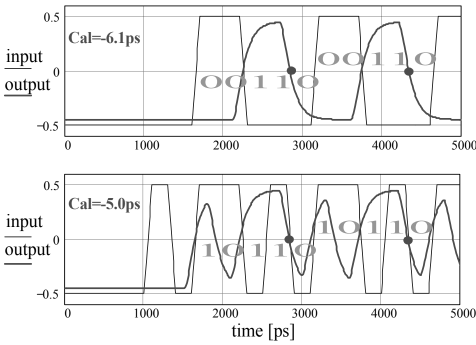


Fig.17 Cal-2 Pattern:0110

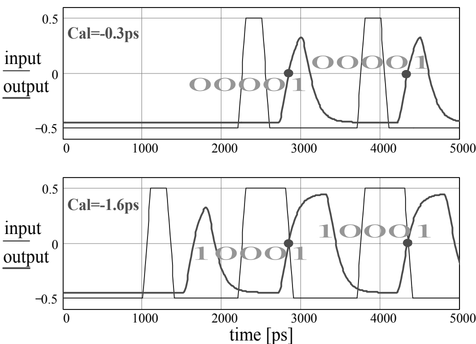


Fig.18 Cal-5 Pattern:0001

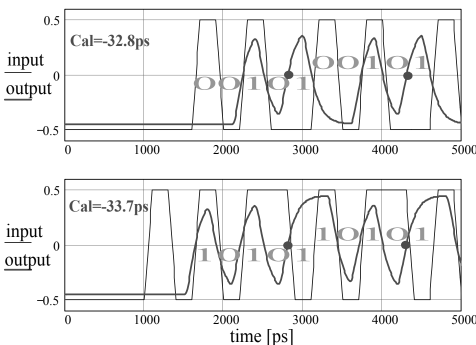


Fig.19 Cal-6 Pattern:0101

### 3.2.3 Eye Diagram of K28.5 Bit Pattern after Calibration

As seen in Fig.20, K28.5 pattern requires all the eight data dependent calibration values.

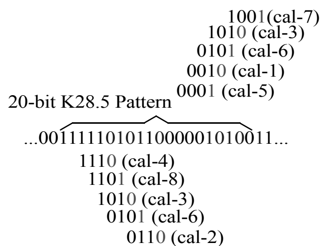


Fig.20 K28.5 Pattern and Data Dependent Cal Pattern

The calibration values obtained in the section 3.2.2 were applied to the input signal, and the output signal was simulated. The eye diagram of the output waveform after the calibration is shown in Fig.21, where one can recognize that DDJ has been almost eliminated. Note that the vertical eye opening does not change much because it is determined by the output circuit characteristic of the final stage buffer.

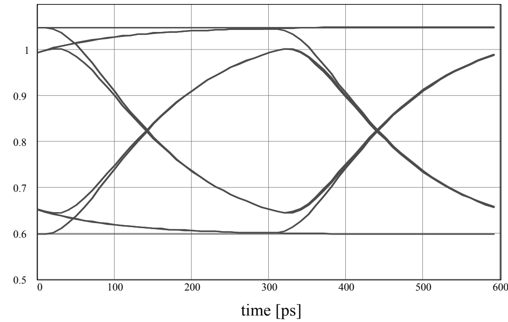


Fig.21 Output Eye Diagram with K28.5 after DDC

## 3.3 Calibration Measurements

As discussed in the section 2.2.1, an at-speed calibration measurement is required to calibrate DDJ. As discussed in the section 2.2.2, the effect of any component between the physical measurement point and the target calibration point (DUT I/O pin for example) needs to be calibrated by some means. We discuss the physical calibration measurements in this section 3.3, and we will discuss how to move the effective calibration point from the physical measurement point to the target calibration point in the section 3.4.

### 3.3.1 Calibration Measurement at Pogo Pin

The DUT input/output signal path in an ATE environment is illustrated in Fig.22 to identify a suitable measurement point.

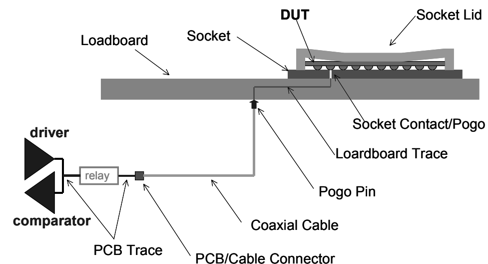


Fig.22 DUT Input/Output Signal Path in Test by ATE

Let's review the candidates.

- *Driver/comparator junction:* The physical measurement point is inside a package, and a high frequency high impedance probe needs to be attached to it. It is not a practical possibility.
- *Somewhere between driver/comparator junction and DUT:* It is difficult to attach a high-frequency high-impedance probe or to insert directional couplers without disturbing DUT I/O signal. Both high impedance probe and directional coupler would require signal amplification, introducing another error source.
- *Pogo pin:* Pogo pin pitch is not too small to develop a robust probe, and a signal pin always accompanies ground pin(s) next to it allowing high quality probing. Therefore, it is a good candidate. In order for a pogo pin to be qualified, the signal path around it must be a good 50 ohm environment because terminating a signal at this point by 50 ohm

load for drive-side calibration or injecting signal there from 50 ohm output impedance signal source for compare-side calibration should not be different from actual signal activity during device test. In order to achieve this condition, we specify the interconnection quality usually using insertion loss and return loss. Evaluating the insertion loss effect on DDJ is straightforward[10][11] and could be intuitively understood. On the other hand, using return loss to specify the tolerable amount of impedance discontinuity for a given data rate (i.e. edge transition speed) with understanding its physical meaning seems to be a big challenge. An attempt to address this challenge is discussed in Appendix.

- *Vias beneath DUT from back side of loadboard:* The issue of using high impedance probe was already mentioned above. Probing from the backside of a loadboard would not be practical for a very high speed application because such an application would use advanced PCB technology such as blind vias or back-side drilling, eliminating the expected probing points for the sake of better signal integrity.
- *Socket mounting pad:* Considering the industry trend toward higher pin counts, it seems to be reasonable to assume BGA packages as DUTs. Almost all the BGA sockets for very high speed and/or high frequency applications today use spring contacts between a loadboard and DUT's solder balls. Such a loadboard has contact pads on the surface, providing potentially good probing points before mounting the socket. However, when there are many high speed signals, especially differential signals, they do not always have ground pads adjacent to them, which prohibits high quality probing at the pads. Therefore, the socket mounting pad cannot be considered as a universal calibration point.
- *Socket pin from top:* In addition to the ground pad problems mentioned above, it is very difficult to make a fine pitch probe tip, especially differential probe tips, which can make reliable contact with the spring contact of the socket while maintaining good signal integrity.

Having reviewed the candidates, the pogo pin seems to be the only point always available for high quality at-speed calibration measurements. To maintain superior repeatability, the probing at a pogo pin or a socket mounting pad is automated.

### 3.3.2 Drive-side Calibration Measurement

With a special probe (single-ended 50 ohm probe and dual 50 ohm probe for differential pair), driver output signal is measured by a high frequency sampling oscilloscope at each pogo pin, requiring no special loadboard as illustrated in Fig.23. The DDJ, timing skew and waveform of each pin at the data rates and the voltage levels of our interest are measured using the calibration patterns discussed in the section 3.2.2.

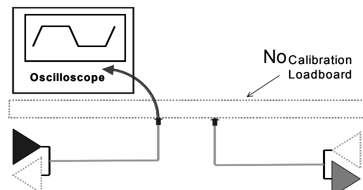



Fig.23 Drive-side Calibration Measurement by Wide Frequency BW Oscilloscope at Pogo Pin

### 3.3.3 Compare-side Calibration Measurement

An already calibrated drive-side is connected to the compare-side, which is to be calibrated, at their pogo pins using a calibration loadboard as illustrated in Fig.24. While propagating from a pogo pin to the strobing point, driver output signal is distorted and DDJ is induced. The signal timing of each calibration pattern discussed in the section 3.2.2 is measured by strobe search as the compare-side calibration measurement.

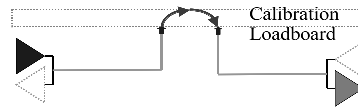



Fig.24 Compare-side Calibration Measurement by Already-calibrated Drive-side Signal at Pogo Pin

## 3.4 Calibration at DUT

No matter where physical calibration measurements are done, the final calibration point needs to be at DUT. There are several active and passive reasons why circuit simulation, which requires modeling the components in the test signal path as illustrated in Fig.25, is used for high speed and high accuracy calibration as follows:

- As discussed in the section 2.2.2, traditionally used TDR is essentially inaccurate to calibrate the high frequency effect of loadboard and test socket (passive reason).
- Modeling and simulation accuracy of passive components has been improving and becoming popular[2] (active reason).
- Although the typical final calibration point used to be at a DUT I/O pin, simulation makes it possible to move the calibration point to the die I/O pad using the package and the I/O buffer models in the calibration simulation (active reason).

The physical calibration measurement point is assumed at a pogo pin in the sections 3.4.1 and 3.4.2.

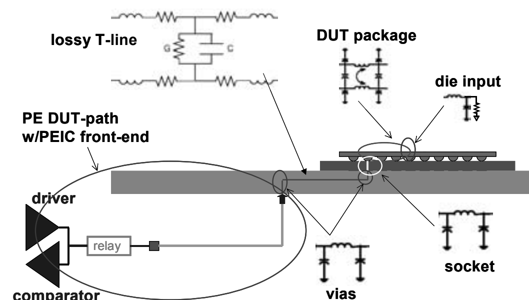



Fig.25 Modeling Components between Pogo Pin and Die I/O of DUT

### 3.4.1 Moving Drive-side Calibration toward DUT

Fig.26 is only for illustration purpose, and actual circuit models should be developed for each loadboard and DUT. The measured driver output waveform after DDJ calibration is modeled by a piece-wise-linear voltage source with a filter smoothing the waveform, and the output impedance is modeled by a 50 ohm resistor. Loadboard traces must be modeled by lossy transmission lines. Vias, test socket and/or a DUT package may be modeled by R-L-C components. Advanced simulators can use S-parameters to model all these passive components, which would result in much higher accuracy when properly used. The input buffer loading can be modeled

by either transistor circuit or approximated lumped element(s) depending on the user's need. Once the circuit model from the pogo pin to the DUT is created, the propagation delay and DDJ with the calibration patterns discussed in the section 3.2.2 are simulated. Then the calibration values derived from the simulation are combined (algebraically added) with the calibration values obtained from the physical calibration measurements, providing the overall calibration values.

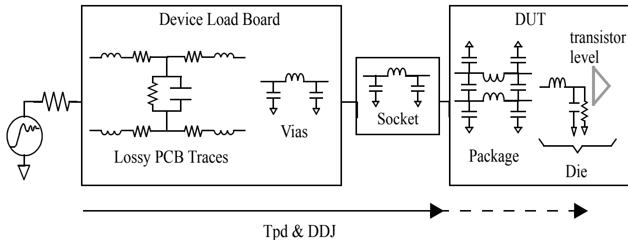



Fig.26 Drive-side Tpd and DDJ Simulation

### 3.4.2 Moving Compare-side Calibration toward DUT

Fig.27 is only for illustration purpose, and actual circuit models should be developed for each loadboard and DUT. The die output buffer would be modeled by either transistor circuit or a piece-wise-linear voltage source with a filter combined with source termination circuitry if necessary. Loadboard traces, vias, test socket and/or DUT package are modeled in the same way as in the drive-side. The loadboard end at the pogo pin is terminated by a 50 ohm resistor to the intended voltage level. Once the circuit model from the DUT to the pogo pin is created, the propagation delay and DDJ are simulated, and the simulation-derived calibration values are combined with the physically measured calibration values, providing the overall calibration values as done in the drive-side.

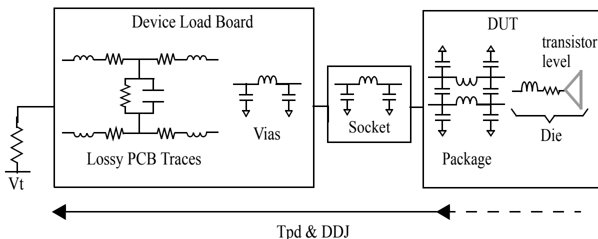



Fig.27 Compare-side Tpd and DDJ Simulation

## 3.5 Future Work Areas

Since DDC, full utilization of circuit simulation, and combining them to calibrate ATE at DUT are new attempts, there are various things to work out such as the ones briefly described below.

- Physically measured calibration values and simulation-derived calibration values are algebraically added for the moment. While this method makes sense for drive-side calibration, there remains timing error in compare-side because the rise/fall time of the reference signal used for the physical calibration measurement is different from the ones of the actual DUT output at the pogo pin. We need to develop a way to correct this error.
- A conceptually straightforward method to achieve the goal above is to develop a compare-side model from a pogo pin, combine it with DUT-specific model consisting of loadboard, socket and DUT, and run simulation to obtain the overall calibration values. There are, however, a couple of problems in this approach. When a transistor-level die model is involved in the calibration, the circuit simulator varies from customer to customer, and it would not be practical to develop accurate ATE models for various simulators. The high accuracy expectation, the complexity of the driver/comparator IC and the DUT signal path including relays, PCB traces, a coaxial cable, etc., requires an advanced simulator.
- DDC needs to be performed at each data rate with each voltage level for the moment, which is very time consuming. We need to study the DDJ mechanism in more detail so that interpolation and/or extrapolation can be used to reduce the number of the physical measurements to cover all the data rates and voltage ranges available for an ATE or a certain range required for testing each DUT.
- Depending on DUT pin assignments, the impedance continuity at the socket mounting pad is not always good for our 50 ohm probing as discussed in the section 3.3.1. This point is, however, a good probing point for the characterization of the loadboard alone, using a vector network analyzer (VNA)[13][14]. Since our probing in time domain currently uses only forward transmission information, utilizing the backward transmission (i.e. reflection) might help address this issue considering the success of the VNA method.
- Although a commercially available oscilloscope is used for drive-side calibration for the moment, a more cost effective dedicated sampling module needs to be developed.
- Although an already-calibrated drive-side signal is used to calibrate compare-side, we need to study how much more timing error reduction can be achieved by using a more accurate pattern source. If it works, a more cost effective dedicated pattern source needs to be developed.

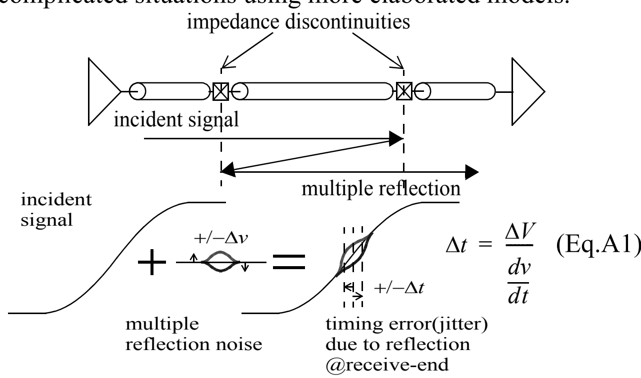
# 4 Conclusion

Having reviewed our traditional timing calibration methods in detail, we have recognized the essential limitations in the traditional calibration methods and the necessity of investigating alternatives for the ever-increasing higher timing accuracy requirement. In order to address such need, we have developed a new calibration scheme which adds data dependent timing error/jitter calibration and utilization of signal path modeling and circuit simulation. As a roadmap for this new calibration scheme, we also discussed what we need to work on next as the extension of the current implementation.

# 5 Appendix: How Much Impedance Discontinuity Can We Tolerate in terms of Return Loss?

When there are more than two impedance discontinuity points between a signal source and a receiver, there exist multiple reflections in the signal path, which can cause timing error depending on the impedance discontinuity locations and the data rate. As illustrated in Fig.A1, the maximum timing error occurs when the incident signal is reflected at one point, then reflected again at another point, and the two-time reflected signal is superimposed on the data edge. The amount of the timing error is determined by the data edge's slew rate and the

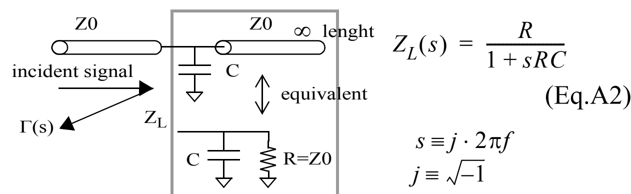
voltage noise generated by the multiple reflection as expressed by (Eq.A1). The noise voltage due to reflection depends on the signal frequency bandwidth (i.e. edge rate[10]) and the impedance discontinuity amount which is a function of frequency. In order to specify the impedance discontinuity of a physically small component such as a connector, "return loss" or its equivalent "VSWR:voltage standing wave ratio"[15] is usually used, and our challenge here is how much return loss at what frequency we can tolerate for a given edge rate and a tolerable timing error amount. As the first step to address this challenge, we discuss below the basic idea of our attempt to relate all the parameters mentioned above using a simple example with the Transient and AC simulation that any SPICE supports. Based on it, one can study much more complicated situations using more elaborated models.




$$\Delta t = \frac{\Delta V}{\frac{dv}{dt}} \quad \text{(Eq.A1)}$$

Fig.A1 Timing Error due to Multiple Reflection

Since reflected signal changes its direction, applying AC simulation is difficult and not intuitive. To overcome this issue, we have to recognize that the reflected signal can be modeled by high-pass filtered signal as explained below. Let's study a simple impedance discontinuity in a 50 ohm transmission line as shown in Fig.A2 using Laplace Transform[16]. The load impedance at the discontinuity point is expressed by (Eq.A2), and the reflection and forward transmission characteristics are expressed (Eq.A3) through (Eq.A5) using S-parameters where $S_{11}$ for reflection and $S_{21}$ for forward transmission. On the other hand, a simple RC High Pass Filter is shown in Fig.A3, and its transfer function is expressed by (Eq.A6). Comparing (Eq.A4) and (Eq.A6), when the condition (Eq.A7) therefore (Eq.A8) too are satisfied, one can recognize that the reflected signal in Fig.A2 can be modeled by the high-pass filtered signal in Fig.A3 apart from the polarity.




$$Z_L(s) = \frac{R}{1 + sRC} \quad \text{(Eq.A2)}$$

$$s \equiv j \cdot 2\pi f \qquad j \equiv \sqrt{-1}$$

Fig.A2 Reflection from Capacitive Impedance Discontinuity in 50 ohm Transmission Line

$$S_{11}(s) = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Z_L - Z_0}{1 + s(R \parallel Z_0)C} - \frac{s(R \parallel Z_0)C}{1 + s(R \parallel Z_0)C} \quad \text{(Eq.A3)}$$

$$\text{if} \quad R = Z_0 \quad \text{then} \quad S_{11}(s) = -\frac{s\frac{Z_0}{2}C}{1 + s\frac{Z_0}{2}C} \quad \text{(Eq.A4)}$$

$$S_{21}(s) = \frac{2 \times \left(\frac{1}{sC} \parallel Z_0\right)}{Z_0 + \left(\frac{1}{sC} \parallel Z_0\right)} = \frac{2}{2 + sZ_0C} \quad \text{(Eq.A5)}$$

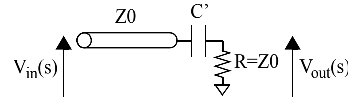



Fig.A3 RC High Pass Filter

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{s \cdot 2Z_0 \cdot C'}{1 + s \cdot 2Z_0 \cdot C'} \quad \text{(Eq.A6)}$$

$$2Z_0 \cdot C' = \frac{Z_0}{2}C \quad \text{(Eq.A7)}$$

$$\therefore C = 4 \times C' \quad \text{(Eq.A8)}$$

Applying the knowledge obtained above, let's go through the procedure to come up with the return loss requirement specification for a given edge speed and tolerable timing error with the assumption that the two impedance discontinuities have the same characteristic to simplify the discussion.

Scenario: The 1V swing signal's rise/fall time is 114ps (20-80%), and the timing error due to reflection must be less than 3ps (one tenth of the EPA budge of a futuristic multi-Gbps ATE). Refer to Fig.A4 for the following procedure.

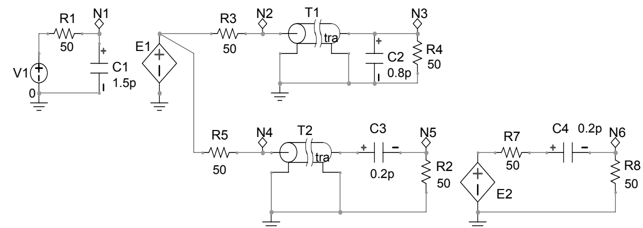



Fig.A4 Simulation Circuit for Single Reflection and for Emulating Two-time Reflection

(1) Adjust C1 to obtain the target signal edge speed at N1. C1=1.5pF resulted in 114ps rise/fall time(20-80%). Applying a rule-of-thumb[3], its -3dB cutoff frequency $fc_{sig}$ is calculated as 1.93GHz (=0.22/114ps) and $2 \times fc_{sig}$ is 3.86GHz.

(2) Adjust C3 and C4 (C3=C4) to obtain the target noise voltage $\Delta V$ at N6, which emulates the noise voltage due to two-time reflection. The signal slew rate is estimated by (Eq.A9). From (Eq.A1), (Eq.A9), and the maximum tolerable timing error requirement of 3ps, the maximum noise voltage requirement is obtained as expressed by (Eq.A11). C3=C4=0.2pF resulted in $\Delta V$= 14.5mV.

$$\frac{dv}{dt} \cong \frac{600mV}{114ps} = \frac{1mV}{0.2ps} \quad \text{(Eq.A9)}$$

$$\Delta t = \frac{\Delta V}{\frac{dv}{dt}} = \frac{\Delta V}{1mV} \times 0.2ps < 3ps \quad \text{(Eq.A10)}$$

$$\therefore \Delta V < \frac{3}{0.2} mV = 15 mV \quad \text{(Eq.A11)}$$

(3) Adjust C2 as expressed by (Eq.A8). C2 must be four times C3(=C4), that is, C2=0.8pF. The simulated time domain waveforms at N2, N5 and N6 are shown in Fig.A5. Note that the amount of the one-time reflected signal observed at N2 is the same as the amount of one-time high-pass filtered signal observed at N5 and that the two-time high-pass filtered signal observed at N6 estimates the two-time reflected signal.

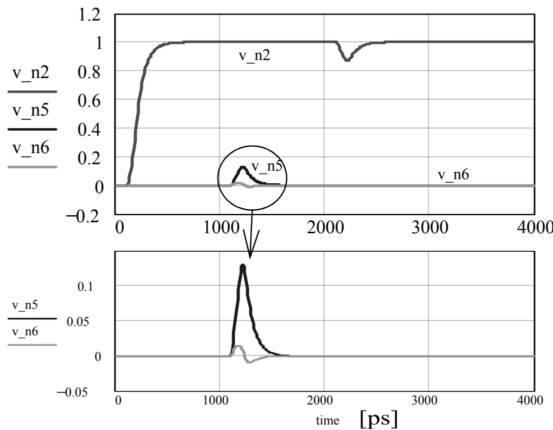



Fig.A5 Simulated Waveforms of Single Reflection, and Emulated Single and Two-time Reflection

(4) Now that all the circuit parameters are set properly, use an AC source for V1 in Fig.A4, and run AC simulation. The results are shown in Fig.A6 along with the $S_{11}$ and $S_{22}$ calculated by (Eq.A4) and (Eq.A5). One can notice the following. At frequencies lower than the -3dB cutoff frequency $fc_{sig}$ (1.93GHz) of the incident signal, the one-time reflected signal's frequency component observed at N5, is about the same as $S_{11}$. At frequencies higher than $fc_{sig}$, the one-time reflected signal's frequency component is approximated by the product of the incident signal's frequency component and $S_{11}$. Thus we have confirmed and/or understood the physical meaning of signal reflection in frequency domain.

(5) Specify the return loss requirement using $S_{11}$.

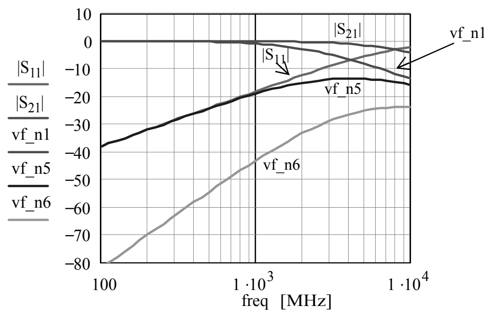



Fig.A6 Frequency Bandwidths of Incident Signal, Single and Two-time Reflection with Signal Path's S11 and S21

The $S_{11}$ in Fig.A6 is the result of adjusting the reflection amount so that the reflection-induced timing error for the given edge speed is contained within the specified maximum timing error. The resulting S11 is -12.6dB at the cutoff frequency (1.93GHz) and -7.2dB at two times the cutoff frequency (3.86GHz). In practice, depending on the other impedance discontinuities, the final requirement specification would be tightened. Note that return loss is usually defined as RL= $-20\log_{10}|S_{11}|$, and so its polarity is positive.

## 6 Acknowledgements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