Feed Forward Test Methodology Utilizing Device Identification

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Abstract

In this paper, we present applications and results for adapted testing at package test utilizing part specific data collected at wafer test. Using unique die level identification we are able to define part specific binning, and parametric limits based on analysis of prior test results and feed this forward to package test.

1. Introduction

Electronic die level trace ability has been readily available in the semiconductor industry for a number of years [1,2]. This random and unique die level ID has historically been created using intrinsic process variations converted into a digital fingerprint or randomly generated bit string stored into non-volatile memory. The purpose of this paper is not to discuss the creation of a unique ID. Rather this paper will focus on a novel test application using the unique ID as an advantage.

In the semiconductor industry unique identification has historically been used in evaluating reliability data in relation to yield and low yield events [3,4]. The purpose here is to evaluate existing defect screens and develop possible new screens.

This paper will present a technique using unique die identification in a different mode. Instead of using the unique ID to evaluate screens, the ID itself will be actively used to bin die, set parametric limits, or modify testing of a given part. The advantage to this feed forward approach for binning and setting of parametric test limits at package test is that you have already tested this die at wafer sort. If the wafer sort data is stored in a database, this data can be used as a seed for evaluating this same part in future tests prior to customer shipment.

In production the first use of the feed forward technique was for binning at-risk material from a low yield wafer at final test. Once this application was proven out in production, limit setting for final test based on wafer sort results was discussed as a second application. Currently we have some experimental data for IDD screening at final test using this technique. In each case utilizing either look-up tables loaded onto the tester or accessed by the tester from a separate database.

The following work documents the use of die ID for screening rogue wafer events at final test. It also documents the use of die ID for setting final test limits for IDD on an experiment lot. Feed forward limits will be compared to final test limits set using standard historical techniques and advanced techniques such as delta IDDQ. Further applications and uses of the technique will be presented, along with any possible drawbacks associated with using die ID in a feed forward manner.

2.1 Final Test Yield Analysis and Disposition

The capability of tracing individual parts from package test to wafer-location allows variations in package test yield to be analyzed as possible wafer-level events. Data collected, including yield, parametric values, and x-y locations of parts at final test can be correlated to information from wafer sort and scribe line test data. Relatively minor package test yield events are possibly related to significantly depressed yield on a single wafer. However these events can fly under the radar since their high loss is typically averaged in with the remaining 24 wafers in the lot. This type issue is more likely to occur if wafer sort coverage does not include analog performance testing. Analog testing is often not included at wafer sort due to test time or tester resource limitations.

Wafer-level analysis becomes possible with die ID. The capability of tracking specific die from wafer sort through final test allows the unique characteristics of each die to be compared at various stages in the manufacturing process. Additionally, disposition of material, after a wafer-level event has been identified, can involve selection of specific die or wafer from an assembly lot of material.

In a recent low yield final test event at LSI, die ID data was collected from a sample of Universal Serial Bus (USB) failures. Die ID was collected on 30 random parts out of a sample of 360 fails. In analysis of these random sample of failures it was determined that all fails originated from the same wafer. What was initially thought to be a 2% lot issue was in actuality a 50% wafer issue. Figure 1. (below) shows 30 USB fails all located on the right hand side of representative wafer map.

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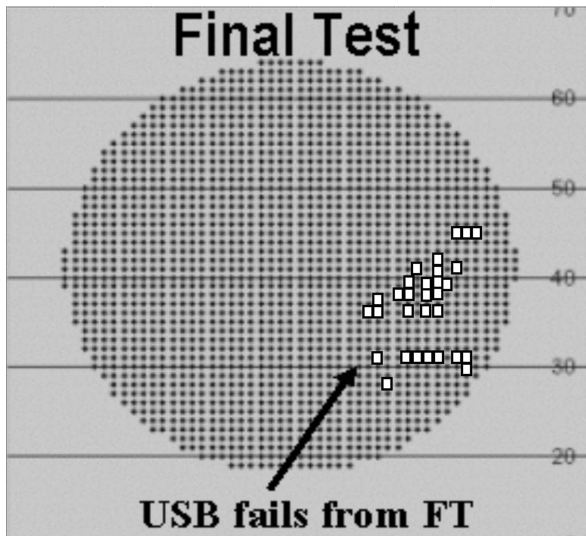


Figure 1. FINAL TEST Failures mapped to Wafer and x-y coordinate

2.2 Disposition of at risk material post assembly

Process monitors in the fabrication process are used to gain insight into the possibility that the end device will be functional. Similarly, wafer test provides a flag to engineering of possible future problems. Unfortunately, not all tests can be performed at the wafer level. Wafer testing is typically done with guard-banded limits and limited to basic functional and structural tests. Even still, there are events at wafer test that will cause the material to be scrapped or held for further analysis. The flow for these events once they have been triggered can lead to scrapping the questionable wafer(s) or holding the entire lot for investigation.

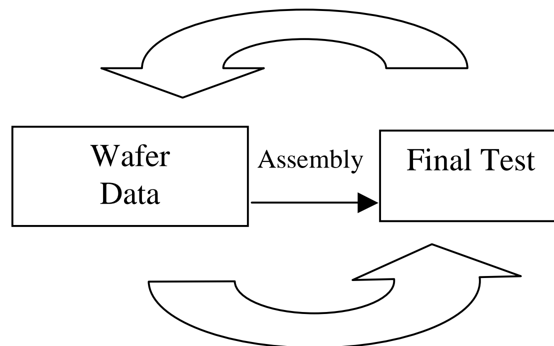
Many times the entire lot is held in order to determine which wafers to remove prior to assembly. This method is recognized as removing questionably reliable material from the general population. Historically once the devices were packaged, all trace ability to direct wafer level information was lost. This is no longer the case with die ID. Mapping die ID back to known wafer sort results such as wafer number and x,y location enables the capability to detect rogue wafer events and clustered defective die at final test.

Now that there is at risk material detected at final test due to rogue wafer or clustered defect events, how is it screened from the remaining good die in the lot? At LSI we have embedded code in our test programs just for this purpose. The technique we developed and used for this purpose is called feed forward binning.

In this, the most basic feed forward application, we have utilized unique die identification to alter binning at final test. The example given is for a test failure at package test that impacted the overall lot yield by ~2%. Using the die identification, the wafer specific information for these devices was fed forward in the yield analysis. This led to the determination that this 2% package fallout was specific to one wafer and represented what would have been a 50% yield loss on that specific wafer. Such a loss at wafer level is usually grounds for scrapping that wafer when detected at wafer sort.

With feed forward binning enabled, this entire wafer was scrapped from the package test lot. This was accomplished by utilizing a 128-bit device identification algorithm within the test program. The DUT ID was compared against a database of target ID's. These "target" ID's were extracted from the yield system database collected from wafer sort results on the at risk parts. See Figure 2 representing the data flow needed to highlight and screen wafer of wafer region level events at final test.

Package Wafer map generated from Low-Yield Final Test event



Yield analysis identifies die that are selected for removal from Lot

Figure 2. Iterative Data Flow

Using this combination — device identification, binning and matching algorithm — further reduces the possibility of future problems from devices that share a possible rogue wafer. The added cost of ensuring a higher level of quality to our customers was the time to re-test these parts. This test cost is approx. 5% adder to standard final test time. The test to evaluate the part ID against the wafer table and bin was done real time on the tester and not offline.

Historical techniques for screening similar events at final test include additional guard banding of low yield

tests or scrapping of full final test lots. Guard banding requires substantial engineering time for additional characterization of tests, limit setting, and program revision. Scrapping of the full lot for a several percent issue is also very costly. Both of these techniques are a round about way of getting to the desired end of scrapping the known rogue wafer. By using die ID we can cut to the chase and with little additional cost and engineering time scrap the known rogue wafer in its entirety using the advantage of known die ID on at-risk parts.

3.0 Feed Forward Limits

3.1 Introduction to Feed Forward Limits

With the use of feed forward binning at LSI we now had the seed infra structure to build some more interesting capabilities utilizing die ID. One other capability developed was feed forward limits.

Current industry standard limit setting for final test is distribution based limits (mean + x sigma) from a statistical representative population of parts at wafer sort plus some tester to tester guard band. To further tighten limit tolerances for screening parametric fails two parameter relationships are sometimes used [5]. An example of this could be setting IDD limit values based on intrinsic speed of a given die.

Using a feed forward limit methodology takes advantage of the fact that this identical part was already tested at wafer sort. Instead of having to set limits based on a group of representative die with varying parametric results, limits can now be set based on this specific die's parametric results collected at wafer sort. This allows for much tighter screening at final test. This method has application not only for standard final test but would also be very interesting for post stress and post burn in testing.

3.2 Setting of Feed Forward Limits

Part specific parametric limits are calculated using standard statistical methods on a significant sample of good parts run through both wafer and package test. Die identification can be used to match die for analysis of wafer test to package test baseline parametric shifts. The intrinsic shift calculated accounts for variation due to processing effects post wafer test and wafer tester to package tester differences. This characterized variation is used to calculate a package test adder or guard band.

An example of this limit setting has been completed on a group of parts for IDD testing. Figure 3. (next column) shows a group of 200 parts with IDD collected at both wafer sort and final test matched by sample number. The parts were selected randomly from a poly split lot run on a new design at LSI Logic. The samples are plotted in increasing IDD order from wafer sort.

In this plot there is a systematic negative offset between wafer sort and final test. This offset averages 12.5% across the entire distribution with a standard deviation is just over 3.3%. Based on this data a final test adder could be calculated. The final limit used for evaluating a certain parameter on a specific part will be that individual parts wafer test parametric result plus the characterized adder.

In the case of IDD there is an apparent decreased in variation as IDD increases as shown in Figure 3. . A possible explanation for this decrease is that the tester to tester variation becomes a smaller percentage contributor as IDD increases or tester resolution changes with scale of IDD. To eliminate this affect the use of more advanced screening algorithms can be used in place of hard percentage limits across the entire IDD range.

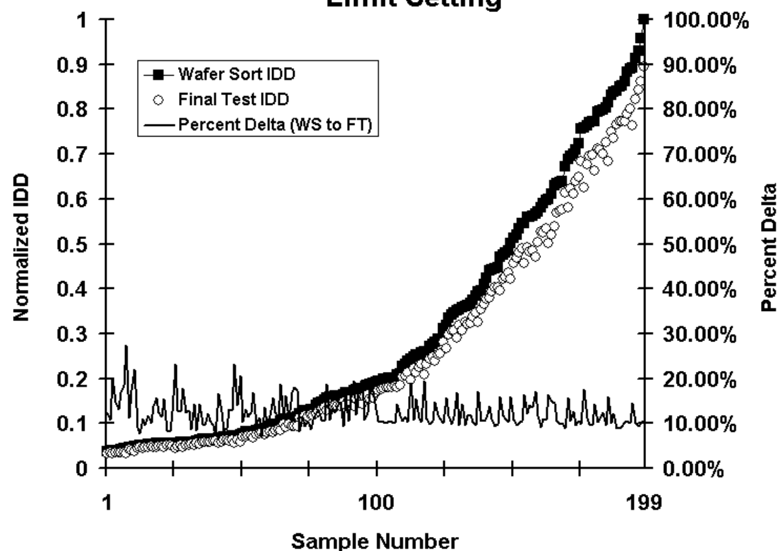


Figure 3: Comparison of IDD values on 200 samples between wafer sort and final test

3.3 Advantages over historical methods

Utilizing the feed forward screening methodology presented above provides advantages over historical methods for calculating package test limits. The advantages stem from the fact that the wafer test measurement result on a specific die is now available for setting the package test limit. The feed forward limit is set

at the wafer sort result plus some final test adder as presented in section 3.2.

Historical methods are without this advantage and are relegated to setting the final test limit at the wafer test limit plus some guard band for post wafer test variation. The main difference here stemming from the difference between known wafer sort results in the feed forward case versus the wafer sort limit in the historical case. Since wafer test limits must account for all fabrication and test related variation they are fairly relaxed to start out. In the historical model this relaxed limit is passed onto package test. In the feed forward case they are not.

Another historical screening method that has allowed for more stringent IDD limit setting on a given die is Delta IDDQ [6-10]. Delta IDDQ uses multiple stop locations and multiple reads of IDD to evaluate parts. Delta IDDQ has two historical advantages over straight IDD testing. The first is toggle coverage, which is made possible by collecting data at multiple vector stop locations. Another advantage is that with taking multiple measurements better statistics can be used for IDD limit setting. One disadvantage to IDDQ testing is time required for multi IDD measurements. On a typical code this time can be as large as 800mS for 20 IDDQ vectors. Due to the time impact and related cost of IDDQ testing it is often run at either wafer sort or final test but not at both.

A comparison of the feed forward approach to limit setting versus both historical methods is displayed in Figure 4. The plot shows current measurements from IDD testing on 175 packaged parts and associated limits using historical stepped limits, feed forward method, and Delta IDDQ at wafer sort. The samples are plotted in increasing IDD order. The Historical speed based limit shows a step as IDD increases.

As evidenced in this production example, feed forward limits are on average as tight as Delta IDDQ and 400% tighter than the historical limits. Some die show limits as much as 3200% tighter than the historical method. Since the intrinsic shift between wafer and package test has been fully characterized there is little concern of over screening with the feed forward limits.

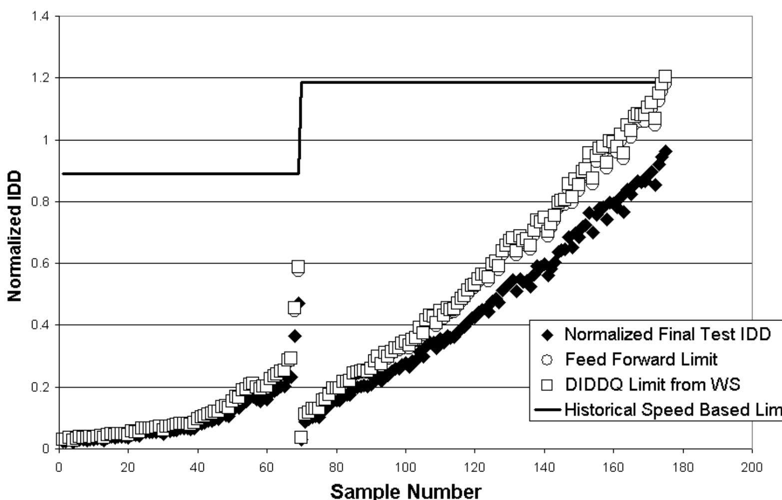


Figure 4: Comparison of Historical IDD limits vs. Part Specific Feed Forward IDD Limits

3.4 Drawbacks to Feed Forward Limit Setting

There are two main drawbacks to using feed forward method for limit setting at final test. The first is building of the infra structure necessary. There is a large amount of engineering overhead to develop the database and tools necessary to feed parametric results from wafer sort forward to final test. Luckily in our case at LSI logic a lot of this infrastructure already existed. The second and largest drawback is the additional test time. As highlighted earlier Delta IDDQ testing can take 800mS for 20 vectors therefore it is typically not run at final test. On the other hand historical IDD limits at final test have almost no time associated with them other than the time required to measure IDD.

In the case of feed forward limits there is overhead associated with the time required to look-up the necessary limit on a given die. This time scales with the size of the database. The database size scales to the number of die within the assembly lot at final test. See Figure 5. (below) which shows a plot of additional test time for feed forward testing as a function of assembly lot size. For a typical lot size of 10,000 units the added test time is 365 mS.

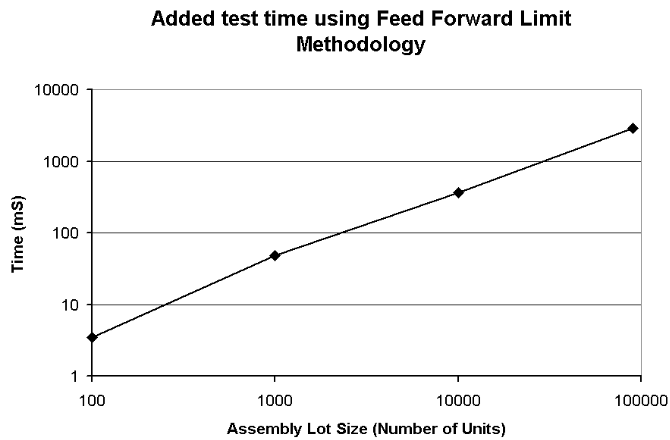


Figure 5: Plot of added test time for feed forward limit methodology vs. assembly lot size

4.0 Conclusions

Two methodologies have been discussed which can improve outgoing quality through the use of unique die identification in a feed forward approach. Using this feed forward approach to binning an example was presented where at risk wafer was effectively scrapped post packaging.

The use of a feed forward methodology was also presented for parametric limit setting. An example of how limits could be set for IDD was presented. With this type of approach it was proven that package test limits for IDD could be tightened 400% on average and up to 3200% tighter without risk of significant over screening.

This paper presents a new methodology and uses IDD as a key example. This technique however can be applied to any parametric tests where data is collected at both wafer sort and final test or during reliability testing at multiple read points. This method improves our resolution to detect shifts. It eliminates the additional noise associated with comparing a die to a historical distribution instead the die is compared directly to itself at some previous read point using a unique die ID.

Disadvantages to the technique were highlighted. The top disadvantage is additional test time required for the real time limit look-up at final test.

5.0 Future Work

Currently we have implemented feed forward limit methodology on volume production at final test on a pilot code. This additional data will hopefully be available for presentation later this year. Our feeling is that this is an untapped data source and could show interesting results across multiple parameters. Other parameters of interest are input leakage and min VDD.

In addition to the topics presented we are working on using the die identification and feed forward methodology for reliability screening. This methodology can be used effectively to look for shifts between pre and post test on multiple reliability screens including burn-in. This unique die ID and wafer sort results can be used for adaptive test applications. One example would be increasing test vectors (coverage) on a die that showed low surrounding yield at wafer sort.

Using package test map generation we will enable post package wafer level yield analysis. This capability when available will allow multiple options for low cost wafer test without sacrificing wafer level data critical for effective yield learning.

6.0 References

[1] M. Alavi, M. Bohr, J. Hicks, M. Denham, A. Cassens, D. Douglas, M. Tsai, “A PROM element based on salicide agglomeration of poly fuses in a CMOS logic process”, IEDM, 1997.

[2] K. Lofstrom, W. Daasch, D. Taylor, “IC identification circuit using device mismatch”, Solid-State Circuits Conference, 2000.

[3] W. Riordan, R. Miller, J. Sherman, J. Hicks, “Microprocessor Reliability Performance as a Function of Die Location for a 0.25u, Five Layer Metal CMOS Logic Process”, Proceedings of the International Reliability Physics Symposium, 1999, pp. 1-11.

[4] R. Miller, W. Riordan, “Unit Level Predicted Yield: a Method of Identifying High Defect Density Die at Wafer Sort” ITC International Test Conference, 2001.

[5] A. Keshavarzi, et al., “Multiple-Parameter CMOS IC Testing with Increased Sensitivity for IDDQ,” Int. Test Conf., pp. 1051-1059, 2000.

[6] A. Gattiker et al., “Current Signatures for Production Testing,” IEEE International Workshop on IDDQ Testing, pp. 25-28, 1996.

[7] W.R. Daasch, J. McNames, D. Bockelman, K. Cota, R. Madge, “Variance Reduction using Wafer patterns in IDDQ Data,” ITC International Test Conference, 2000.

[8] C. Thibeault, “Improving Delta-IDDQ-based Test Methods,” ITC International Test Conference, 2000.

[9] D. Bergman and H. Engler, "Improved IDDQ Testing with Empirical Linear Prediction," Int. Test Conf., pp. 964-963, 2002.

[10] R. Daasch, et al., "Neighbor Selection for Variance Reduction in IDDQ and Other Parametric Data," Int. Test Conf., pp. 1240-1248, 2002.