Future Trends in Test: The Adoption and Use of Low Cost Structural Testers

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Abstract
Recently, low cost and desktop structural testers have become popular for various reasons. Although originally aimed at reducing production test costs, they have quickly migrated to other niches and have proven useful in reducing not only cost, but time-to-market. Tracking the "use" spaces has resulted in identifying three clearly different areas of application: design-desktop, correlation-lab, and the production-test floor. These spaces have defined tasks such as characterization, first silicon bring-up, test program development, yield-learning diagnosis, and production probe, some of which will be described as case studies.

1. INTRODUCTION

One of the drivers that brought a handful of manufacturers to the "low-cost structural tester" market was the very public statement of the ITRS (International Technology Roadmap for Semiconductors) that test cost was beginning to dominate the overall silicon cost and that a $200 per pin tester would alleviate this problem [1]. One of the other drivers of the market was the thought that design-for-test (DFT), specifically scan, had reached a level of maturity that would enable wide adoption of DFT or structural testers. Both of these assumptions would come under fire in the early days of establishing the DFT tester business.

Just a few years ago several manufacturers began making optimized structural testers that were more geared to processing Scan and BIST data and operations, as opposed to complex functional sequences. By doing this, the requirements on the ATE were significantly reduced and this in turn reduced the cost associated with the creation of the tester. The lesser requirements allowed the tester to be created with "off the shelf" electronic components which made it possible to achieve a very low cost-point, but this did result in an ATE that was deemed to have reduced capability as compared to traditional "big iron" semiconductor testers (which was the measuring stick of the day). In reality, the point of view of a lesser-capability is cultural artifact of comparing "the way things have always been done" to new ways of doing things [2]. The structural tester represents "a different way of doing things."

The method used to reduce the cost of a tester is to remove the precision, accuracy, and flexibility involved with clock timing, signal timing, and voltage adjustment (power delivery) – which is exactly what Scan, logic BIST and memory BIST test techniques require [3]. For example, Scan can be shifted at a fairly slow rate such as 50MHz and with loose timing such as 2ns and at fairly fixed voltage levels. Since delivering scan data to scan input pins is not an exercise in testing pin timing with hundreds of picoseconds of edge placement and tens of picoseconds of resolution; and since providing scan data into a scan chain at data rates greater than 100 MHz can be a toggling power problem; then optimizing only for scan operation enables a lesser constrained set of specifications to be supported by the tester. In addition, with many portions of the semiconductor industry now claiming that DFT and scan were mature technologies – as evidenced by the adoption (sales figures) of scan insertion and automatic test pattern generation (ATPG) tools – the thought process was that there would be a plausible market for scan-only lower cost testers.

So, the initial target market of the structural tester was to reduce the cost involved in providing structural or DFT-based digital test for production test. The incentive to market that drove the early-adoption manufacturers was that there really would be a market for a reduced functionality tester optimized and aimed at structural test techniques such as scan, logic BIST, and memory BIST – and this type of tester would reduce the cost of asset acquisition, operation, and ongoing maintenance costs.

However, history and hindsight has shown that the production test market on low cost commodity parts – the market that would benefit the most from the tester – at that point in time, did not rely on scan and BIST techniques, but on legacy and reuse functional vectors that are applied on fully amortized functional testers. Attempts to get this market to adopt scan and BIST to enable a

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migration to the low cost structural testers turned out to be an exercise in "the cost of change" dynamics – in most cases, the parts cannot afford the area overhead of scan; do meet their coverage, quality, and time-to-vector needs with legacy functional vectors; and have reasonable test times. So, for the low cost structural testers, there was a mismatch between the initial goals of "introduction to the market" and the reality of "use."

As a response to this obvious mismatch, the structural tester manufacturers tried to find a better technological fit and discovered that the structural tester could be used in other markets (SoCs, ASICs, and Microprocessors) and in other "use spaces" than just "cost reduction of production test" – and in a broad enough sense so that they weren't considered niche solutions.

This paper will describe the "use spaces" and the tasks and drivers involved in each space, and will then describe some of these tasks in the context of a compact customer case study. Section 2 will introduce the change from traditional thinking on the use of structural testers, and section 3 will introduce and define the "use" spaces of structural testers. Section 4 will discuss some of the actual applications of structural testers in the use spaces by citing customer case studies. Section 5 will conclude the paper.

2. THE NEW APPLICATION MODEL

Having discovered that the target market for low cost structural testers was not a match for the assumptions behind the tester, the low cost structural tester manufacturers assessed the market and found that they were a fit in other places. What was discovered was that the market that supported scan and BIST techniques, was actually the larger ASIC and the SoC markets, and in and extreme sense, the high-performance microprocessor market – the markets that use automatic test pattern generation (ATPG) and design-for-test (DFT) techniques to increase the quality metric and to reduce the time-to-vectors. The goal here is more about "time-to-market" rather than "test cost." In addition, it was discovered that calling a "structural tester" a "tester" was actually politically and culturally a hindrance in most companies (if it is called a tester, then the asset acquisition group must get involved – no matter what the size, cost, or application of the tester).

Today, however, after some reassessment and a shift in goals and some features and capabilities, there has been an active adoption of low cost structural testers and the applications have been in some varied and surprising venues. There has been, though an active movement to remove the "low cost" moniker and to revitalize the market as the "structural" or "DFT" analysis engine/tester.

There are at least three major application spaces that have been defined that have completely different goals and technology drivers; and that have significantly different user communities: the Design-Desktop; the Correlation-Lab; and the Production-Testfloor.

3. THE USE SPACES

Almost all of the structural testers that are being used today can be described as being in the three defined "use spaces." There are a few notable exceptions such as using the structural tester in the burn-in or life-test environments – but the large majority of the structural testers fit within the following descriptions of the Design-Desktop Space; the Correlation-Lab Space, and the Production-Testfloor Space.

Table 1 DFT-Structural Tester Use Spaces

Use Space	**Principle User**	**Driver**
Design-Desktop	DFT Engineer	Capability
Correlation-Lab	Test Engineer	TTY, TTV
Production-Test	Test Floor Manager	Throughput, Cost

3.1. The Design-Desktop Space

The Design-Desktop Space is defined as the use of the structural tester by the Design, DFT, or Validation engineer – and that use is predominantly on the desktop which may be in a cubicle or office, or possibly in a lab environment. The purpose is using the instrument, which is not viewed as a tester, in the design environment – and is commonly for test chip and final device characterization, first silicon bring-up, and experiments. All of these tasks are to understand the device with respect to the design goals, not as a precursor to going into production.

The key driver is "capabilities." From the designer's point of view, the question asked is, "do I have the capabilities and resources necessary to conduct the measurements required for characterization, bring-up, and experiments; or to assess my silicon against my specifications, goals, and the design library?"

The design-side focus in this space is to link the desktop structural "instrument" to design-side tools – simulators, ATPG engines, waveform viewers, and even tools such as static timing analysis and layout viewers. The designer is more comfortable with using familiar design tools than in learning a tester interface. In addition, the design-side is much more comfortable using scripts to drive their processes rather than bringing up GUIs to accomplish tasks. This has driven several efforts at operating the “structural assessment instrument” more like a simulator than a tester.

Some new directions for use in this space are investigations of using the tester to drive emulation configurations, or on conducting simulation acceleration using large FPGAs. The structural tester can be viewed as a reusable and configurable testbench or testbench driver.

Another new focus in the first silicon and characterization space is the use of EDA tools and voltage manipulation techniques to auto-debug scan chains [5]. The growth in this area is in the capabilities of the EDA tools which feed the structural testers and receive feedback data from them.

3.2. Correlation-Lab Space

The Correlation-Lab Space is defined as the use of the structural tester by the traditional test aligned organizations – the test, product, and failure analysis engineer. However, the form-factor of the structural tester (desktop) allows the tester to be comfortably located in a cubicle, office, or (kiosk) engineering laboratory. The key purpose in this environment is to use the tester in a lower cost environment that is linked to a production tester. The structural tester provides a less-expensive and more convenient way to conduct test pattern validation, test program development, and debug-diagnosis or failure analysis that is related to fails on a production tester – commonly called yield-learning during ramp-to-volume.

Even though the structural tester offers a less-costly alternative to using a production tester on a test floor or to using a traditional big-iron tester in the engineering lab, the key driver is for "time-to-" optimizations such as reduction of time-to-market, time-to-yield, and time-to-volume. The test engineer’s goal is to validate vectors and develop the test program more rapidly; or to trace the root causes of systemic failures more quickly.

The main optimization originally aimed at only this space (but now found useful in the design space as well) is the direct link or connection to EDA vector generation (ATPG) software. The EDA-Link, as it is called, is the ability to create and directly use tool-created vectors without complex and error-prone translations; and for returning fail data directly from the tester’s fail log to the diagnostic tools associated with the ATPG tools to rapidly find the gate level element responsible for the fails.

The most common design vector formats are VCD (see IEEE Standard 1364) and WGL, but STIL is slowly gaining ground since all of the ATPG tools now support this format. The extra information that STIL (see IEEE Standard 1450) carries makes the fail log more useful and helps reduce the time to diagnosis. There have been several tester-related tools that have sprung up to make use of the extra information carried in STIL to produce failure displays that can immediately show clusters of failures in the scan chain format, the hierarchical register format, or even the physical layout format. It is then also fairly easy to relate the failing scan bit to a schematic viewer to conduct logic tracing. All of these views are possible because of the Scan Structures portion of a STIL vector file that carries design information related to the scan chain trace file (the chain name, the bit order, netlist names of the scan cells, the associated clocks, etc.).

The power of scan versus functional pattern application, in this case, is that each scan test is an independent test – and so reams of fail data may be collected. Whereas functional tests are corrupted after the first fail and so only the first fail is valuable – then a complex and convoluted process of masking and repairing the pattern must be done to collect useful data. One of the original advantages of the structural tester in this case is that they support much more capture memory (a shortcoming now noted by big iron ATE providers).

All of the ATPG tools support the diagnosis of fail data by making use of scan test independence and the capture of multiple fails – these fails, when fault-simulated without fault dropping, can implicate faults common to groups of fails. The implicated fault is generally a gate input or output – to explore beyond the gate, a layout tools is required for further investigation into the routing (interconnecting wires).

Some new directions for use in this space are the direct import and export of patterns and vector sets between a desktop or laboratory machine and a production tester. This enables development of vectors in the “easy-access” test environment to be directly applied to the other “difficult production” environment – and for tests associated with failing behavior to easily be transferred from the production machine to the debug machine. Another area of activity is to directly connect and synchronize the desktop-sized structural test machines to e-beam probers and other diagnostic equipments.

3.3. Production-Testfloor Space

The Production-Testfloor Space is defined as the traditional use of a tester on a production test floor (or as part of the traditional production test flow). The user in this space is largely the test floor manager who is responsible for keeping the test floor fully engaged (no idle capacity) and for keeping operating costs low. The purpose is the same as the original traditional purpose of using the tester as a wafer probe tester, final package tester, or multi-site tester (and related processes such as 24 hour burn-in). And along with this purpose, comes all of the standard production concerns about uptime-downtime, throughput, capacity, cost and hardware equipment interfaces (such as handlers and probers).

The key drivers in this space are for sustained throughput and for managed cost. The difference in application, however, is because very few parts are tested solely and completely with structural test – functional tests are still applied. Therefore, "insertion management" has been the main traction in this area. For example, the restrictions placed on inexpensive wafer probe, due to the probe needles, probe head cost, and power problems, line up remarkably with the abilities of structural test. For example, DC, AC and compressed scan vectors, and memory BIST, can be applied through a smaller interface, no high speed signals are required, and the AC testing can be done with a slower data rate applied at the pins, but using the internal embedded chip's PLL to generate the internal at-speed conditions. If a DFT technique such as wrap-IO has been applied (to allow input pins to be ignored), then a high quality probe insertion can be accomplished by having probe needles touch only a few pins – and with signal requirements well within the electrical capabilities of those needles. This opens the technological door for conducting wider multi-site testing of logic.

The new directions in the production space concern actual "insertion management" on die that contain analog/mixed-signal, high-speed IO, embedded flash memory, and other non-digital functions – the old thinking was to have one fully capable machine to do all testing in as few insertions as possible. However, many of the new SoC devices have very low ASPs and conducting multiple insertions on lower cost equipment is proving to be a viable solution.

Another new direction in the production space is the use of loadboard solutions for high-speed IO and separate instrumentation for RF testing. Both of these steps enable low cost structural testers to be used in conjunction with these tasks.

4. CUSTOMER CASE STUDIES

As can be seen, there are many applications for which the structural tester is ideal, and many for which it is useful, cost-effective, or time-effective. The development of the "use spaces" model is not a theoretical development that came from a marketing group somewhere, but instead comes from the observation of real structural testers being used in various and different customer organizations.

However, not all customers are willing to discuss their research or specific uses. Fortunately, there are a few that are willing to provide information that can be used to show the tradeoffs and, hopefully, the advantages of the structural tester over competing traditional methods. Below are some compact customer case studies with commentary to show some of the real uses, and their advantages and concerns.

4.1. Customer #1, Teresa McLaurin, ARM: AC Characterization [4]

- Customer: IP Core provider that must evaluate test chips for hard core certification.
- Main use: Characterization of first silicon test chips.
- Goals: Understanding timing and performance.
- Technique: AC Scan using Path Delay and launch-to-capture VCO-driven on-chip clocking.
- Alternative method: Functional vectors applied at-speed.
- Advantage: Deterministic targeted evaluation of AC coverage in a desktop environment.
- Comment: Still not enough support from or linkage to EDA tools for this particular application.

4.1.1. Added Commentary

The desktop or lab-bench environment is ideal compared to physically taking parts over to a rent-a-tester test floor. The unit is easy to learn, and once the scripts and methods are in place, a whole tray of parts can be tested in about a half-hour.

4.2. Customer #2, Luis Basto, Analog Devices: Functional vs Structural

- Customer: Chip provider that must evaluate test chips and first silicon.
- Main use: Comparison of functional methodology versus structural methodology.
- Goals: Understanding coverage, tradeoffs, techniques and schedules.
- Technique: Application of both functional and structural vectors on identical parts and on both structural and functional testers.
- Alternative method: Application of scan on traditional functional testers on a test floor.
- Advantage: Experiments conducted in desktop environment to compare and contrast both functional vectors applied on functional testers and structural vectors on structural testers.

- Comment: There is still a requirement to translate vectors from design formats VCD and WGL to both the structural and the functional tester.

4.2.1. Added Commentary

While the desktop structural tester is designed primarily for structural testing, it is also a very capable machine for initial silicon validation using functional test patterns as long as those patterns meet the reduced edge-set handling requirement. This technique provides a cost effective method for silicon bring-up, working in conjunction and in parallel with silicon debug on big iron ATE.

One of the major issues in running functional vectors on equipment such as the desktop structural tester involves vector translation. Many of the low cost testers typically operate only in the STIL language so the user needs to do a VCD-to-STIL or WGL-to-STIL translation from the design formats; or must convert from other tester formats to STIL to do direct comparisons to other testers. There are at least two techniques to convert these functional test vectors. The first method is to do a direct translation by cycle-izing the functional vectors into STIL test patterns with exact and correct timing information. A second method is to take an existing pattern that has already been cycle-ized and to convert it.

The advantage of the direct translation method is its standalone nature, but it is equivalent to test pattern development for the device or test chip. The disadvantage is that it has all the pitfalls of new pattern development. Additionally, a pattern translated independently to run on two different testers may exhibit different behavior that unnecessarily complicates debugging and correlation. Translating a pattern that has already been cycle-ized on the big iron ATE provides the opportunity to directly correlate with the ATE.

Our method to convert from existing ATE vectors, was to take the test vectors, the pin and waveform information for the functional patterns, and to use scripts to process these to generate an equivalent STIL pattern file with the appropriate timing, pin groups, and vector data. This test pattern is now easily compile-able and run-able on the desktop structural tester.

Initial tests exhibit high correlation with results from their big iron brethren. That is, tests that give a passing indication on high-end ATE are passing on the Ocelot. Tests that fail also fail similarly. After this initial correlation, we are much more confident in converting and running other test patterns.

We also ran a test on a device with scan chains. This really highlights the capability of the structural testers. Since the test vectors are a scan pattern, ATPG tools directly output the scan vectors in STIL format. These vectors are then compiled on the desktop structural tester and a test program quickly develops. No translation is needed. Schedule wise, from generation of the scan vectors to running the vectors on the device took less than a day – or in other words, we got the scan test program working in less than one day. This same development took at least two weeks on the big iron tester.

4.3. Customer #3, Jay Bedsole, Freescale Semiconductor: Production Probe

- Customer: Chip (IDM) provider that must sustain full production probe.
- Main use: Production wafer probe for devices with strong DFT.
- Goals: Sustained throughput at the lowest cost.
- Technique: Using a low-cost, DFT tester.
- Alternative method: A functional big-iron tester.
- Advantage: Lower asset cost of equipment, lower operational cost, small footprint, and meets or exceeds all requirements for the probe insertion. Also, it fits within the capabilities and limitations of testing through probe needles.
- Comment: As an added benefit, the chosen platform accelerated test development and deployment.

4.4. Customer #4, Composite Customer: Test Program Development

The original customer that was to represent this case study pulled out of the final paper, so the originators of case study #2 and #3 have graciously volunteered to address this case study since they both have experiences in this area.

- Chip (IDM) providers that must develop the test program for production test.
- Main use: Rapid development and validation of production test program.
- Goals: Reduced time-to-test program.
- Technique: Using the desktop and production-sized tester as a vector development vehicle in conjunction with EDA tool links to prove out ATPG vectors; restricted functional vectors (meeting edge set restrictions); and to provide fail information that allows diagnosis to be conducted (to fix vectors).
- Alternative method: Test program development on a big-iron functional tester.
- Advantage: Reducing the time to validate vectors and turn them into test program components.

- Comment: One customer makes the comment that "this is great for stuck-at scan vectors, but functional vectors must still be used and they do not flow through the easy ATPG-flow". The other customer comments that "the flow for AC scan vectors has been made much easier".

5. CONCLUSIONS

The evidence points to the fact that there is such a volume of silicon to be evaluated, and that the new defect models are making the diagnosis process so daunting, that adoption of structural techniques is the only way (currently known) to make the process more efficient. Functional vectors are costly and time-consuming to develop; require many steps that can lead to errors during the translation steps required to get them to the tester; and require a high level of expertise when using them to conduct debug and diagnosis. Structural test and structural testers have made the tasks of characterization, first silicon bring up, and yield-learning much more efficient.

Currently, a back of the envelope tally by the providers of low cost structural testers indicates that there are have been more than 50 evaluations, somewhere near 40 current customers, and around 15 traction buys (organizations coming back for more). These numbers have been filtered through several layers of proprietary interest and are suspect, but they give a good indication that the market is growing, rather than being stagnant or having an initial heyday and then dropping off. It is known, although maybe not publicly, that many of the companies listed in the top 30 semiconductor listing have evaluated and adopted a structural tester for one or more of these "use" spaces.

In addition, the big iron ATE providers have recently tried to emulate many of the advantages of the low cost structural testers – attempting to smooth out the direct reading of ATPG vectors or STIL; adding more capture memory; and post processing the failure logs to provide the pattern/chain/bit format. And largely, all of them are becoming friends with the EDA ATPG providers.

Clearly, the number of customers, the growth curve for sales, and the expansion of the structural testers into the various use spaces, and the change in functionality of the big iron ATE providers, show that adoption is a necessary trend – not just a fad.

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