

Testing and Remote Field Update of Distributed Base Stations in a Wireless Network

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Abstract

A novel distributed test architecture of transmitting IEEE 1149.1 Boundary Scan (a.k.a JTAG) Test Access Port (TAP) signals over a serial channel is presented in this paper. It is developed to facilitate the system testing and remote field update of distributed base stations (DBS) in a wireless network. The state-of-the-art DBS does not only improve the overall quality of wireless network services via its ability and ease to provide wider coverage in various environments, but also lowers the installation and operation costs as well as reduces the space requirements. However, the DBS poses great challenges for system testing and field update operation due to its distributed architecture. The proposed distributed test architecture enables the system testing as if the distributed units are on a backplane within the same chassis. In addition, the embedded boundary scan test software, that is running on the microprocessor of the controller board, takes advantage of the proposed distributed test architecture to update the configuration Programmable ROMs (PROMs) of the distributed units remotely without on-site visits. A novel slow-fast programming algorithm is also proposed for efficient remote field update in DBS to overcome significant fiber propagation delay. It reduces the time for PROM update from over an hour to less than 19 minutes over a 12km fiber.

1 Introduction

Bell Labs of Lucent Technologies introduced a third-generation (3G) CDMA2000 base station that, because of its compact design and distributed architecture, offers the

flexibility needed to meet a variety of deployment needs and coverage challenges for mobile operators.

This platform can be used to simplify deployment in areas difficult to cover with traditional products, fill in coverage gaps, or provide additional capacity in high-traffic areas such as highways, major cities or in buildings. Because it has a small footprint, and can be mounted on telephone poles, walls and roofs of buildings, the base station can substantially reduce cell site acquisition costs.

This state-of-the-art distributed base station (DBS) does not only improve the overall quality of wireless network services via its ability and ease to provide wider coverage in various environments, but also lowers the installation and operation costs as well as reduces the space requirements. However, *the DBS poses great challenges for system testing and field update operation due to its distributed architecture.*

A novel distributed boundary scan (BS) test bus architecture of transmitting IEEE 1149.1 Boundary Scan (a.k.a JTAG) [5] Test Access Port (TAP) signals over a serial channel is presented in this paper. It is designed to facilitate distributed system testing and remote field update of DBS. The proposed BS test bus architecture enables the system testing as if the distributed units are on a backplane within the same chassis.

In addition, the embedded BS test software, that is running on the microprocessor of the controller board, takes advantage of the proposed test architecture to update the configuration Programmable ROMs (PROMs) of the distributed units remotely without on-site visits. A new programming algorithm is also proposed for remote field update to efficiently program the PROMs in DBS to overcome the significant fiber propagation delay.

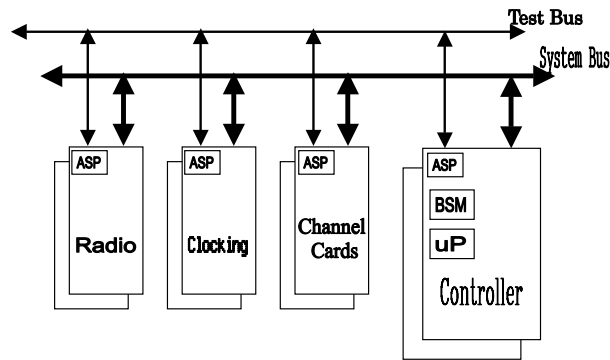


Figure 1: Traditional base station test bus architecture.

In the following of this paper, we will first briefly introduce the DBS architecture for the readers to not only understand the advantages of DBS but also realize the test challenges associated with it. We will then describe the proposed BS test bus architecture for distributed system testing and the proposed embedded BS software algorithm for remote field update.

2 Advances in 3G Distributed Base Station Architecture

This section is only intended to describe the advantages of DBS and introduce the features of DBS architecture that make it unique and difficult for testing.

In DBS architecture, the radio frequency units (RFUs) refer to the components that send and receive radio signals; the base band units (BBUs) refer to the components that process and send the radio signals to and from the mobile switching center. The DBS's unique distributed design enables mobile operators to deploy RFUs and power system separately from BBUs. The RFUs and BBUs can be connected by a customer-provided single-mode fiber cable at distances of 10km or even farther.

For example, in an urban environment, multiple BBUs can be deployed at a company maintenance facility and connected to a mobile switching center via a T1 line, while the RFUs are deployed miles away near major highways, train and bus stations and hospitals and connected to the BBUs via a single-mode fiber cable.

The DBS provides a compact, low cost unit for small or entry-level networks. It is designed for suburban build-out, hole filling, hot spots, in-building or any

broad coverage, medium capacity network need. Flexible mounting options include poles, walls, roofs and in buildings.

DBS is designed for increased capacity and coverage in the smallest footprint. Its compact construction reduces space requirements and real estate costs, which may significantly shorten the time to market through rapid site selection and zoning. In addition, the overall quality of network service improves via the ability of DBS to provide coverage for a variety of environments. Furthermore, DBS provides remote software control by remote maintenance tool (RMT), which results in fewer on-site visits, trimming travel and labor costs.

3 Test Challenges Posed by Distributed Base Stations

As shown in Figure 1, a traditional base station usually consists of controller boards, channel cards, clocking units and radio cards, which all reside on a system backplane in the same chassis. The system level test bus architecture is an extended BS multi-drop bus architecture [9, 1]. It is made of the five BS TAP signals and contains a boundary scan master (BSM) [4, 3] as a test bus master in the controller board. Each of the other boards contains an addressable scan port (ASP) [9, 7] device as a test bus slave. This multi-drop test architecture supports *embedded boundary scan* [8], where the BS tests are embedded on the controller board and executed by the on-board microprocessor as a part of system functions during field operation.

However, in DBS as shown in Figure 2, the BBU

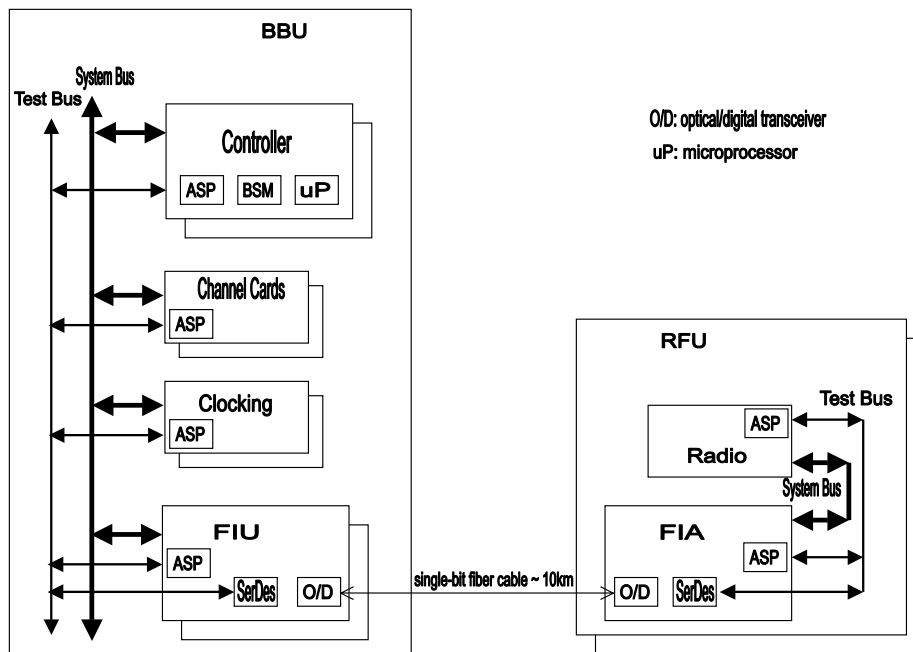


Figure 2: Distributed base station test bus architecture.

consists of controller boards, channel cards, clocking units and fiber interface units (FIU) on one local backplane. Over a single-bit fiber, on the other side of each FIU, there is a RFU which consists of one or more radio cards and a fiber interface adapter (FIA). The FIA acts as a remote and distributed backplane for the radio cards in RFU. Furthermore, communication between BBU and RFU is accomplished by the communication of FIU and FIA via a long single-bit fiber cable.

Due to the distributed architecture, the following is a list of test challenges posed by DBS.

- Only a serial fiber channel between the local and remote backplanes is available. Oversampling [2] and multiplexing compression techniques must be implemented due to the limited bandwidth between the pair of serializer and de-serializer (SerDes).
- The serial fiber channel is a functional channel, not a dedicated test channel such as the five BS TAP signals. How to test the distributed units as well as the integrity of the serial fiber channel during system integration test and field operation are the most difficult test problems of DBS.

- FIA of DBS is not only a distributed backplane for a radio card but also is a board itself in the distributed system. How to effectively test FIA during system integration test and field operation must be addressed.
- How to perform field update to eliminate on-site visits for the distributed RFUs is a key issue of DBS.
- We propose to transmit the five BS TAP signals over the serial fiber channel to address the above test challenges. The proposed architecture will be described in detail later in Section 4. However, *a long fiber causes significant propagation delay*, which limits BS test clock (TCK) frequency. Usually a single-mode fiber incurs 5 μ s propagation delay per kilometer. For example, a 10km long fiber (i.e., 20km roundtrip) incurs 100 μ s roundtrip delay. Since BS test data output (TDO) changes only on the falling edge of TCK and BS test data input (TDI) is clocked on the rising edge of TCK, for a 50% duty cycle TCK, there is only 0.5 cycle for falling edge to travel to FIA and data coming back down to FIU (i.e., 0.5 cycle = 100 μ s). Hence, TCK must be slower than 5kHz for correct operations. Therefore, it is very

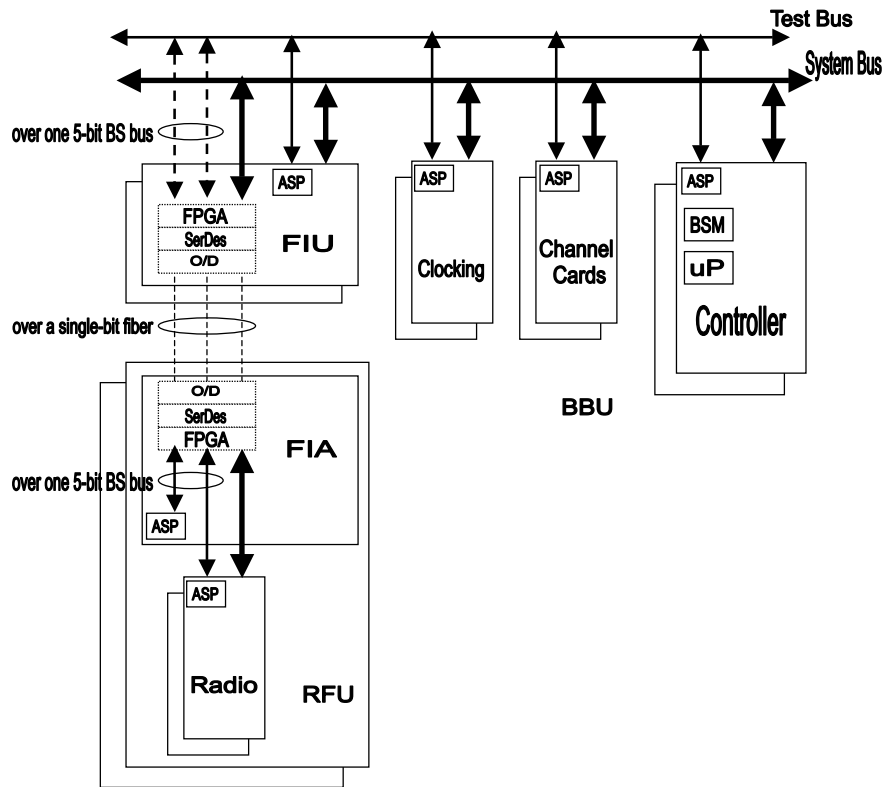


Figure 3: Conceptual/logical view of the distributed test bus architecture.

essential to slow down TCK for distributed system testing.

- Due to the slow TCK frequency to accommodate long fiber delay, how to efficiently update the configuration PROMs of distributed units need to be addressed.
- How to design the remote units robust enough so that a failure during remote field update does not cause the breakdown of the remote units is a key design-for-reliability issue.

4 Proposed Distributed Boundary Scan Test Bus Architecture

To address the distributed characteristics of DBS and the test challenges described above, we propose to transmit the five BS TAP signals over the serial fiber channel to

implement a *distributed BS test bus architecture*. The proposed distributed test architecture enables the distributed system testing as if the distributed FIAs and radio cards are on a backplane within the same chassis. The conceptual view of the resulting test architecture is shown in Figure 3.

In the proposed test architecture, ASP is equipped on each board, including FIU and FIA. While the ASPs of FIU and other boards in BBU connect directly to the system BS multi-drop test bus, ASPs of FIA and remote radio cards communicate to the system BS multi-drop test bus via a virtual connection. The main components consisting of the virtual connection on each side of the serial fiber cable are an FPGA, a SerDes, and an optical/digital transceiver. Both the oversampling and multiplexing compression techniques, implemented in the FPGA, are applied to the five TAP signals as well as the data on the system bus to be transmitted between the pair of SerDes via the single-bit fiber channel.

Note that we equip the FIA with an ASP device

to ease the test and field update, although FIA itself is a distributed backplane for radio card. FIA is treated as a board in the distributed test bus architecture as shown in Figure 3.

The followings are the four other important DFT issues of the proposed test architecture.

1. According to the ASP protocols, each board in the system must be assigned to a unique 10-bit address. In our traditional system test bus architecture [1], we always assign the 10-bit ASP address as a combination of a board ID and a slot ID, where the board ID is unique for each type of the boards and the slot ID is unique for a slot in the system backplane. In the proposed distributed test bus architecture, we still assign the ASP address as the combination of board and slot IDs. However, the slot ID of FIA and the radio card in any of the RFUs is identical to that of the corresponding FIU. That is, we treat the FIA and radio card as if they are plugged into the same slot of corresponding FIU. This slot ID is embedded in the data that is transmitted over the fiber from FIU to FIA.
2. In the multi-drop test bus architecture, only the primary TDO (PTDO) of the ASP, that has a matched 10-bit address of the ASP protocol, is enabled to drive the test bus. The PTDOs of other ASPs are in high impedance. In our proposed architecture, since there are two logical links over one 5-bit BS bus to the multi-drop test bus without the administration of an ASP device as shown in Figure 3, an *ASP protocol watcher* must be implemented to guarantee the proper TDO enabling in a multi-drop bus.

The ASP protocol watcher can be implemented in the fiber interface FPGA of either the FIU or FIA to monitor the ASP protocol sent from BSM to all ASPs. We decide to implement it in the fiber interface FPGA of the FIU.

Theoretically, the ASP protocol watcher should at least consist of a TAP controller and a simplified ASP protocol decoder for the multi-drop test bus arbitration. PTDO will be enabled when the ASP address matches either FIA or the radio card (only need to check the board ID since the slot ID for the corresponding FIU, FIA and radio cards are identical) on the same slot. Otherwise, PTDO remain(or change to) disabled when address is not matched.

However, since the TDO is pulled-up to a logic-1 at the system backplane in this particular DBS under development. Hence, PTDO of the fiber interface FPGA on FIU (that connects to the multi-drop test bus) only needs to drive logic-0 when the ASP acknowledgement protocol is being sent back, i.e., when ASP address is matched with FIA or radio cards on RFU. Therefore, the ASP protocol watcher can be significantly simplified by the use of a tri-state buffer on PTDO signal, where both the negative-enable and input are PTDO itself.

3. The integrity of the fiber cable becomes a part of BS chain integrity test in the proposed distributed test bus architecture. Currently, other than the BS chain structure integrity test problems, we do not have serious performance test issues yet. However, we are researching in two directions for performance testing on the long fiber cable: (i) using BIST circuitries at both sides of the SerDes to test the fiber interconnect at-speed for performance testing; (ii) investigating the availability of the SerDes devices that supports IEEE 1149.6 Boundary Scan Testing for Advanced Digital Networks [6].
4. It is a fact that the proposed test bus to connect the local system backplane with the distributed backplanes is built over a functional channel! We discover this problem as a critical DFT issue late in the development of the proposed test architecture. For example, without the existence of a working clocking unit in BBU, the DBS is designed to shut off the serial fiber channel as a fail-safe mechanism. Hence, if without a working clocking unit, we can not perform system test and field maintenance using the proposed test bus as well. This defeats the purpose of having a test bus. Hence, we minimize the dependency between the proposed distributed test bus and the serial functional fiber channel by generating clocks for fiber channel at the fiber interface FPGA in the absence of a working clocking unit in DBS.

5 Proposed Remote Field Update via Embedded Boundary Scan Architecture

Standards in wireless networking are advanced faster than the designs can ever catch up. Hence, the system designs

utilize a lot of programmable devices such as FPGAs, whose program contents are usually stored in configuration PROMs. Because of the standard advance and design upgrade, in-system field update for configuration PROMs of communication systems becomes an important issue. It is especially essential and costly for DBS since there are a lot of distributed RFUs that needs updating and each of them are separated in long distances.

To minimize the cost and ease the field update for DBS, we decided to take advantage of both the proposed distributed test bus and embedded BS architectures to perform remote in-system field update. That is, via the embedded software running on the microprocessor of the controller card and the distributed test bus architecture, configuration PROMs in each of the RFUs can be accessed and updated remotely from a computer that is connected to a network (such as internet) where the BBU is connected.

The proposed embedded BS-based in-system field update approach requires the least amount of system software support since it does require the control of on-board microprocessors (except for the microprocessor of the controller card). The proposed distributed BS test bus architecture provides the access to the desired BS device for update without affecting the system function of the other boards in the system.

However, to prevent the accidental breakdown of the DBS due to a failure during in-system remote update, it is advised to have at least a secondary configuration PROM for an FPGA as backup. It is absolutely essential for FIA since once the fiber channel breaks down, DBS systems break down and there is no way of remote accessing distributed RFUs except for on-site repair.

5.1 Slow-Fast Programming Algorithm for DBS Remote Update

As described earlier in Section 3, due to the long fiber propagation delay, TCK must be slow down significantly. Typically in BSM (where the TCK is generated for embedded BS), TCK can only be 1/128 speed of a reference input clock signal. However, once BSM is set to be in the TAP manual mode, TCK is automatically generated as the frequency of the microprocessor accessing one of the BSM internal control register — the CUTO register. Using this software technique, we can generate TCK as

slow as 1hz to meet the requirement of slow TCK on a long fiber.

Due to the slow TCK requirement and the huge volume of PROM update data, it is expected to have a rather long programming time. However, device updates need to be carried out in the shortest possible time in order to minimize system down time.

Since not all the data for device update require remote response, the requirement of slow TCK frequency to accommodate the significant fiber propagation delay does not apply to those data that do not require remote response. Based on this key observation, a novel programming algorithm is proposed for field update in DBS to provide efficient PROM programming. It is called *slow-fast programming algorithm*. A slow TCK is applied whenever remote response is needed (since the roundtrip propagation delay must be considered), such as device ID test for BS integrity in the beginning of PROM programming. Whenever the remote response is ignored during PROM programming, a fast TCK is applied, such as during the PROM memory programming phase. Note that due to the fiber interface design as well as the oversampling frequency, the fast TCK frequency also has an upper bound.

Since the majority of the data for device update are in the memory programming phase, where a fast TCK is applied, time for field update is reduced significantly from over an hour to less than 19 minutes on a 12km fiber as the experimental results shown in Section 6. However, it is still too long for system down time. If we update the PROM without readback, i.e. without reading back PROM content bit-by-bit for verification right after the completion of memory programming phase, the time for update further reduces to 50 seconds. Although it is very efficient, we do not verify the newly updated programming data in the PROM. Besides bit-by-bit readback verification, PROM currently does not have any other options for program verification, such as cyclic redundancy code (CRC) or checksum signature. We are researching how to provide a CRC signature for fast and correct remote PROM update.

For the ease of remote field update operation for DBS, the algorithm automatically determines what the slow TCK frequency is and when it should be applied. Before any programming data is applied to the target device, the algorithm performs a *ping test* to determine if the circuit board containing the target device is present

Table 1: Slow-fast programming for PROM update over 12km fiber in a DBS.

<i>Slow TCK</i>	<i>Fast TCK</i>	<i>With Readback</i>	<i>Without Readback</i>
		658746 bytes	310682 bytes
4khz	4khz	> 1 hour	≈ 50 min
4khz	500khz	18 min 35 sec	50 sec

in the system. It is during this test the algorithm determines what the slow TCK frequency should be. This is done by pinging the target board and waiting for acknowledgement. This is initially done at the highest possible frequency and the frequency is incrementally reduced until remote acknowledgement is properly received. Based on the programming data that are in Serial Vector Format (SVF), the algorithm also determines automatically when remote response is needed and adjusts TCK frequency accordingly.

All the embedded BS software features, such as BS integrity test, system test and remote field update, are offered as a part of system software functions and included in our RMT for remote software control of DBS. They are used for system integration test and for system maintenance during field operation.

6 Experimental Results

We have successfully developed the proposed distributed test bus architecture and remote field update embedded software with the proposed slow-fast programming algorithm in a real DBS with a fiber up to 12km between FIU and FIA. The experimental results are shown in Table 1. Programming time for PROM remote field update is reduced significantly from over an hour to less than 19 minutes over a 12km fiber when the slow-fast programming algorithm is applied. It takes about 15 seconds for the field update programming data downloaded from a PC hard disk drive to the flash memory on the controller card via Ethernet connection for embedded BS application. We also verify that the theoretical 4khz slow TCK for 12km fiber is indeed the TCK frequency to guarantee correct remote response. The fast TCK frequency is determined by the fiber interface design and the oversampling frequency.

There are the four major phases in PROM programming data: erase, BS chain integrity check, memory

programming and bit-by-bit readback verification. Remote response are required for integrity check and readback verification since the device ID codes and PROM program content must be read back from RFU over the long fiber cable. Hence, slow TCK must be applied during these two phases.

Huge volume of data are involved in memory programming and readback verification. For example, as shown in Table 1, field update data size for program with readback is 658746 bytes and that for program without readback is 310682 bytes. As discussed earlier, since the about half of the data for device update are in the memory programming phase, where a fast TCK is applied, time for field update can be reduced significantly.

However, the other half of the data require remote response during bit-by-bit readback verification. If we update the PROM without readback and reply on the fiber interface to report errors during programming data transmission, the time for update further reduces to 50 seconds. Although it is very efficient, we still can not guarantee if the data are correctly programmed into the PROM. In addition, we need to update system software to report fiber transmission error and, if needed, request embedded BS software to re-program PROM. On the other hand, we can provide CRC signature for readback verification instead of bit-by-bit of the PROM content. We are researching the above two options to not only further reduce time for remote field update, i.e. system down time, but also maintain high reliability for PROM update.

During the experiments, we appreciate about the BS TCK clocking scheme. Since TDO changes only on the falling edge of TCK and TDI is sampled on the rising edge of TCK, test data is always available 1/2 TCK cycle ahead of the rising edge of TCK. Such a clocking scheme makes the ordering of multiplexing technique, which was a major problem for some other functional channels, become irrelevant. Otherwise, due to the jitter of the clock signal over the fiber, it is always advised to multiplex data before the clock to avoid errors.

7 Conclusion

A novel distributed BS test bus architecture of transmitting the five BS TAP signals over a serial channel to facilitate distributed system testing and remote field update of DBS is presented in this paper. The proposed BS test bus architecture enables the system testing as if the distributed units are on a backplane within the same chassis.

Test challenges posed by DBS are described and addressed in the proposed distributed test architecture. The significant propagation delay over a long fiber cable creates an interesting DFT issue which desires to have a slow TCK. Hence, we propose a novel slow-fast programming algorithm to accommodate the requirement of slow TCK while reducing time for remote field update.

In the proposed test architecture, a special ASP address assignment not only guarantee the uniqueness of the resulting ASP address, but also provide a consistent logical view of related FIUs, FIAs and radio cards. An ASP protocol watcher is also implemented in the fiber interface FPGA of FIU to ensure the integrity of multi-drop test bus.

In addition, the embedded BS test software takes advantage of the distributed test architecture to update the configuration PROMs of the distributed units remotely without on-site visits. It also applies the newly proposed slow-fast programming algorithm for very efficient remote field update of PROMs in the DBS.

We are currently researching for alternatives on the fiber channel integrity and performance testing using BIST or IEEE 1149.6. We are also in the process of developing CRC signature for readback verification to replace bit-by-bit PROM verification for fast and reliable remote field update in the DBS for 3G wireless networks.

8 Acknowledgment

The authors would like to acknowledge Robert W. Barr who made the test architecture of DBS possible. We thank John A. Andersen and Dante G. De Rogatis, who support the DFT designs and feedback us valuable ideas with their design expertise. We appreciate Bradford G. Van Treuren and Jose M. Miranda for their valuable discussions and expertise in boundary scan test issues.

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