Tester Architecture For The Source Synchronous Bus

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Abstract

A majority of digital logic devices receives stimulus from an external system clock and sends information out on bus pins which are synchronized to the system clock. During functional testing of such devices, ATE architectures supply the clock and input data signals. The output signals generated by these devices are synchronous to the tester and are sampled accurately by the test equipment's strobe circuits. With the emergence of wide data busses in memories and high speed communication protocols implemented to transfer data between the CPU and peripherals, it has become necessary to forward a clock along with a group of bus pins to maintain skew across the high speed bus pins to an acceptable value for system design. This has resulted in a class of devices which have source synchronous busses where output signals are sent out relative to their strobe (output clock) signals. This paper describes the challenges associated with testing this class of devices with the classical automatic test equipment (ATE) architecture and presents a unique hardware solution implemented on a contemporary tester architecture to meet the test challenge. This paper also compares this implementation with other solutions available in the ATE domain.

1 Introduction

As data busses approach gigabit speeds, chip designers have a challenge trying to keep the skew among the bus pins at an acceptable value. Board designers are similarly faced with the difficult task of matching trace lengths for these high speed busses. To overcome high speed data transfer problems, two types of data transmission methods have been gaining more and more acceptance in computers and communications devices. The first method uses a clock signal for small numbers of bus pins such that the data is timed by the clock. The number of data bits transmitted in a clock cycle can be 1,2 or even 4 giving rise to the term "quad pumped data bus." It is common for the clock signal to be delayed at the originating device such that the clock occurs at the center of the data. This ensures that there is enough setup and hold time at the receiving device's input register. This is shown in Figure 1 where the double pumped data has a timing specification with respect to the output clock signal. A 64-bit data bus is thus broken into eight groups of eight pins; associated with each group is a clock, also known as strobe. Such busses are known as source synchronous busses. Examples of such busses are the Intel P4 bus, the HyperTransport™ bus from the HyperTransport Technology Consortium and the parallel RapidIO bus from the RapidIO Trade Association.

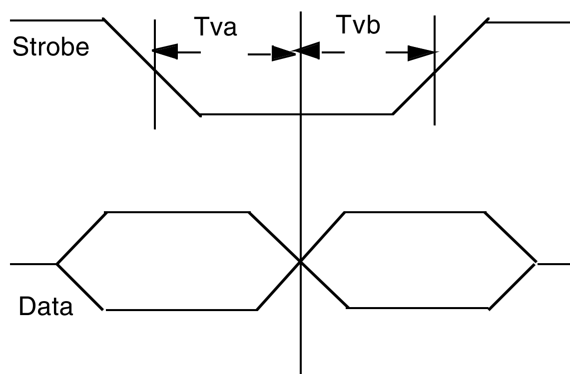

Figure 1. Source Synchronous Transfer

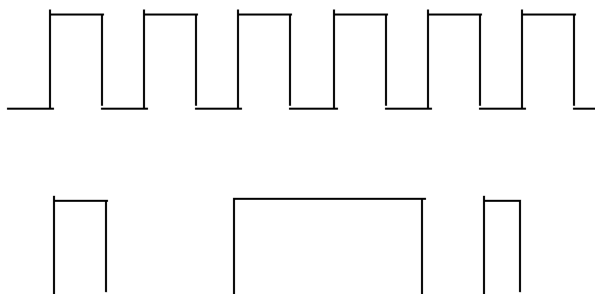

Figure 2 Serial Data Transmission

The second method, originally adopted in the communication field, uses an embedded clock technique where data is sent serially as bit streams of 1's and 0's. This is shown in figure 2. In this serial transmission technique the receiver recovers the clock using a clock data recovery circuit, CDR, and

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then uses it to decode the data from the bit stream. Examples of serial links are serial ATA, XAUI and PCI-Express. Each of the two methods has advantages and disadvantages which are well covered in the literature. At speeds beyond 2.5Gbps, serial data transmission is gaining total acceptance due to very tight skew tolerances required of the source synchronous bus.

The conventional ATE architecture has been designed to test parallel IO and data busses by providing accurate drivers and comparators. The emergence of high speed source synchronous buses and serial links on devices introduces new test challenges for the test engineers and the test equipment. Serial link test solutions have been around in the communication industry for quite some time and are provided in the reference [1]. This paper focuses on the source synchronous testing challenge and shows a hardware solution for testing source synchronous busses, designed and implemented on the EXA3000 family of testers from Credence. Section 2 presents the source synchronous test challenge and the test methods used in conventional ATE to implement it. This leads into section 3 which describes the design of a hardware called the data strobe receiver (DSR) for converting an output clock from a device under test (DUT) to a tester strobe and uses it to test other device outputs. The description goes into the details of the software designed and implemented to seamlessly integrate the source synchronous test method with the existing GUI tools. Section 4 enumerates the advantages of the source synchronous test over conventional methods and comparable architectures. The paper concludes with the details of implementations of source synchronous test capability in next generation testers .

2 Background

In source synchronous operation the device produces its own clock which travels in parallel with the data. In this way, the clock suffers the same delay and drift as the data, enabling the data to be reliably clocked into the receiving device.

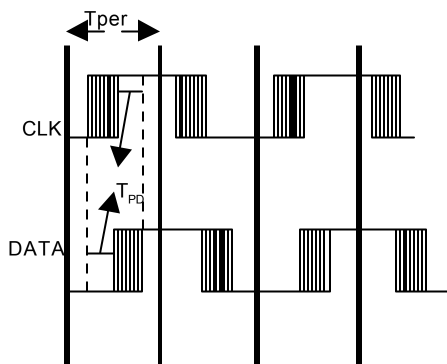


Figure 3. Clock, Data, Period relationship

A wide range of devices including graphics chips, chip sets, hard-disk-drive controllers, and DSPs is now starting to use data ports that involve source synchronous clocks. The widespread use of these techniques has profound test implications for SoC devices. In a test environment the tester is usually the master, with its period generator that determines the timing of all other signals to and from the DUT. The waveform diagram in Figure 3 shows the relationship between the source synchronous clock and data with respect to the ATE tester period. The DUT clock and data have a specified relationship usually termed as time valid before/after (Tvb/Tva) or simply Tpd. But neither one of these signals has any fixed time specification to the beginning of the tester period. These signals can occur anywhere in the tester period for each DUT due to process, voltage and temperature (PVT) variations. Furthermore, as clock forwarding, another name for source synchronous operation, technique is adopted by higher speed devices jitter causes clock and data signals to move with respect to the tester clock from one test to another test of the same device and also within a functional test of a single DUT. Therefore, the traditional ATE has the following test challenges in testing a source synchronous bus:

- Validating the delay between the clock and the data signals in a functional test.
- Measuring the delay between the clock and data for device characterization.
- Being able to perform the above at the high operating frequencies of the bus in the presence of high amounts of jitter.

Devices have been designed in the past with timing specifications defined with respect to one of their output signals instead of the input clock. Test methods do exist for such devices in production and validation. These methods are described in the next section. The source synchronous (SS) bus architecture is another example of this class of devices with the main difference being that its test requirement can exceed 1Gbps.

2.1 Conventional ATE SS test using search

In order to validate the delay between the DUT clock and data, a search is performed to first locate the clock within the tester period using a short functional test pattern. The tester strobe for the clock signal is modified using Tclk, the result of the search. Knowing the DUT clock position relative to the tester period, tester strobes for the data signals are positioned Tpd+Tck (maximum spec value for Tpd is used) seconds away from the beginning of the tester period. The main functional pattern is then run on the DUT with the new adjusted timing. This pattern serves to verify the clock to data delay specification. In order to determine the clock to data delay, a series of strobe searches is done, one per data signal, to determine the earliest time from the tester period that the data signal could be strobed and still get the main functional pattern to pass. The search results yield the position from the beginning of the tester period of each data signal. The clock signal position from the tester period, determined by the first search, is then subtracted from the data signal search result to get the actual clock-to-data delay. In order to compensate for PVT variations,

the search to locate the clock and the subsequent tester timing adjustments are done in the test program for each device and are repeated within the test program each time a level or frequency is changed prior to a test.

2.2 SS test using capture methods

Many ATE architectures use capture memory for storing functional test failures. With enough capture memory behind individual tester channels, it is possible to undersample the outputs of the SS DUT over a reasonable range of input stimulus patterns and display the acquired data in a scope-like graphical form for timing and voltage relationships [3]. The acquired data can also be processed online to calculate the delay between the strobe and data signals of the DUT to enable pass fail decisions for the test program. The analysis can produce SS delay data on a per data bit basis. Figure 4 shows an acquired signal from the test system using the capture method.

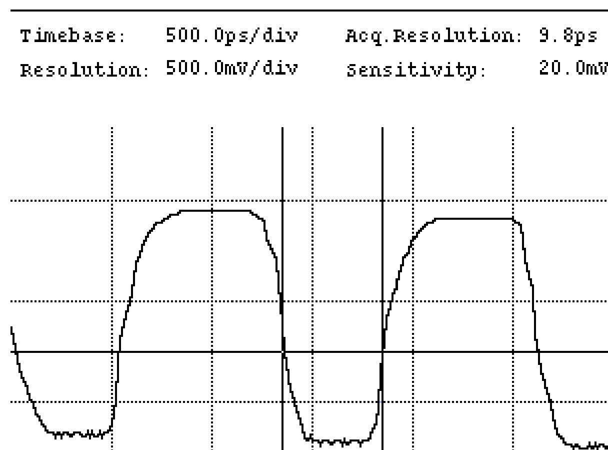


Figure 4. Acquired Signal from DUT

2.3 Need for dedicated hardware for SS test

The above two methods for SS testing work satisfactorily at low data rates of less than 400Mbps where the amount of jitter in the signals is low and is a small fraction of the data bit width. At higher data rates approaching 1Gbps, the amount of jitter is a large percentage of the data bit width. The clock/strobe signal from the DUT at high frequencies can move in time from cycle to cycle and can wander over a long functional pattern burst. Because of this jitter/wander effect, the search for the SS clock yields a worst case result. When the search result is used to position the tester timing for the data signals, functional failures can occur on devices that could potentially have a lot of jitter but are not necessarily bad. The reason for this is that the search method does not allow for the jitter inherent in the data and clock signals. Typically the data and clock signals jitter in the same direction and by roughly the same magnitude for short term conditions. This is shown clearly in Figure 5. The capture method, described in the last section, which uses undersampling to acquire signals from the DUT will be able to deal with the jitter on the SS signals and can compute the delay between clock and data on a cycle to cycle basis. A large number of samples is normally required for signal acquisition, directly impacting SS test time. Therefore, there is a strong case for developing a dedicated hardware for the SS test implementation. The next section describes a new pin electronics card (PEC) design for the purpose of SS testing.

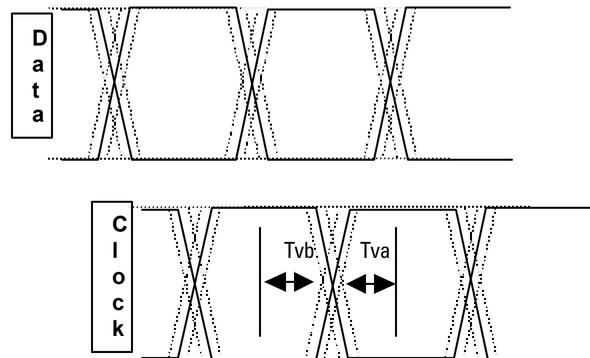


Figure 5. Clock and Data Jitter

3 Source Synchronous Test Option

Conceptually, the implementation for realizing a source synchronous test uses the DUT generated clock as a tester strobe for the corresponding data signals. To support the general source synchronous test requirement, the following capabilities need to exist in the hardware implementation of the SS test option:

- Operate at 1.6Gbps or better
- Accommodate up to 32 SS DUT differential clocks
- Accommodate a minimum of 32 data bus pins per SS clock. The data pins could be differential or single ended.
- Comprehend rising edge, falling edge and dual edge generated data bus.
- Be able to position the data strobes derived from the DUT clock anywhere in the data eye of the data signals.
- Support the flexibility of two different clocks generating the SS data.
- Enable multi pass testing for increasing maximum SS test rate by providing a divider for the SS DUT clock. The multi pass test will also be useful in devices with high amount of clock jitter exceeding 1 unit interval (UI).
- Allow SS testing to be turned off and on easily.
- Provide for per pin search capability of the SS delay between clock and data.

The SS test option is designed for the EXA3000

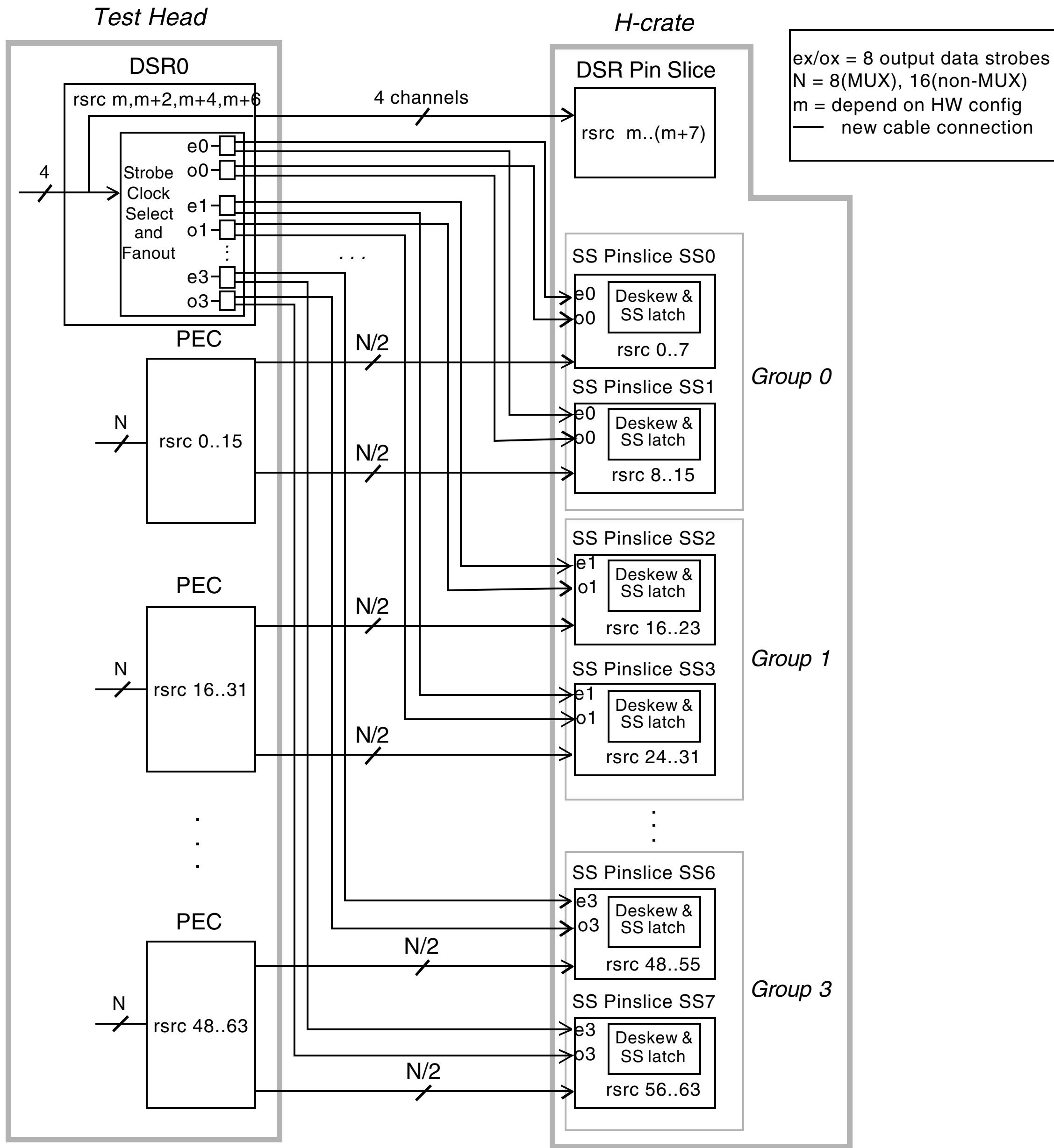


Figure 6. Source Synchronous Option Hardware Block Diagram

tester, the latest member of the Credence ITS9000 family of testers, employing the Sequencer Per Pin (SPP™) timing architecture [2].The option consists of both hardware and software with the main areas of hardware development being the creation of Data Strobe Receiver PEC and the SS pin slice. The software supports the new hardware functionality by enhancing the various tools with SS test functionality. It also includes runtime and cal / diags enhancements to support the new hardware features. The hardware and software changes are detailed in this section. At a high level, the EXA3000 tester hardware architecture consists of a test head housing PECs which provide stimulus to and digitize the response from the DUT. The stimulus signals come from mainframe pin slice cards to the PECs in the test head. The digitized response signals are sent from the PECs back to the pin slices in the main frame for pass/fail evaluation. More details of the tester architecture can be found in the references [2],[3]. The EXA3000 tester can be configured with a large (1024 channels) or a small (512 channels) test head. The SS hardware and software description in the next sections reference the large test head, which supports 16 single ended (PEC516 card) or 8 true differential (PEC7 card) channels in each of the 64 test head slots. Figure 6 shows the hardware block diagram depicting the connectivity and the relationships at the system level for the source synchronous test option. There are

two main hardware blocks which deal with the SS

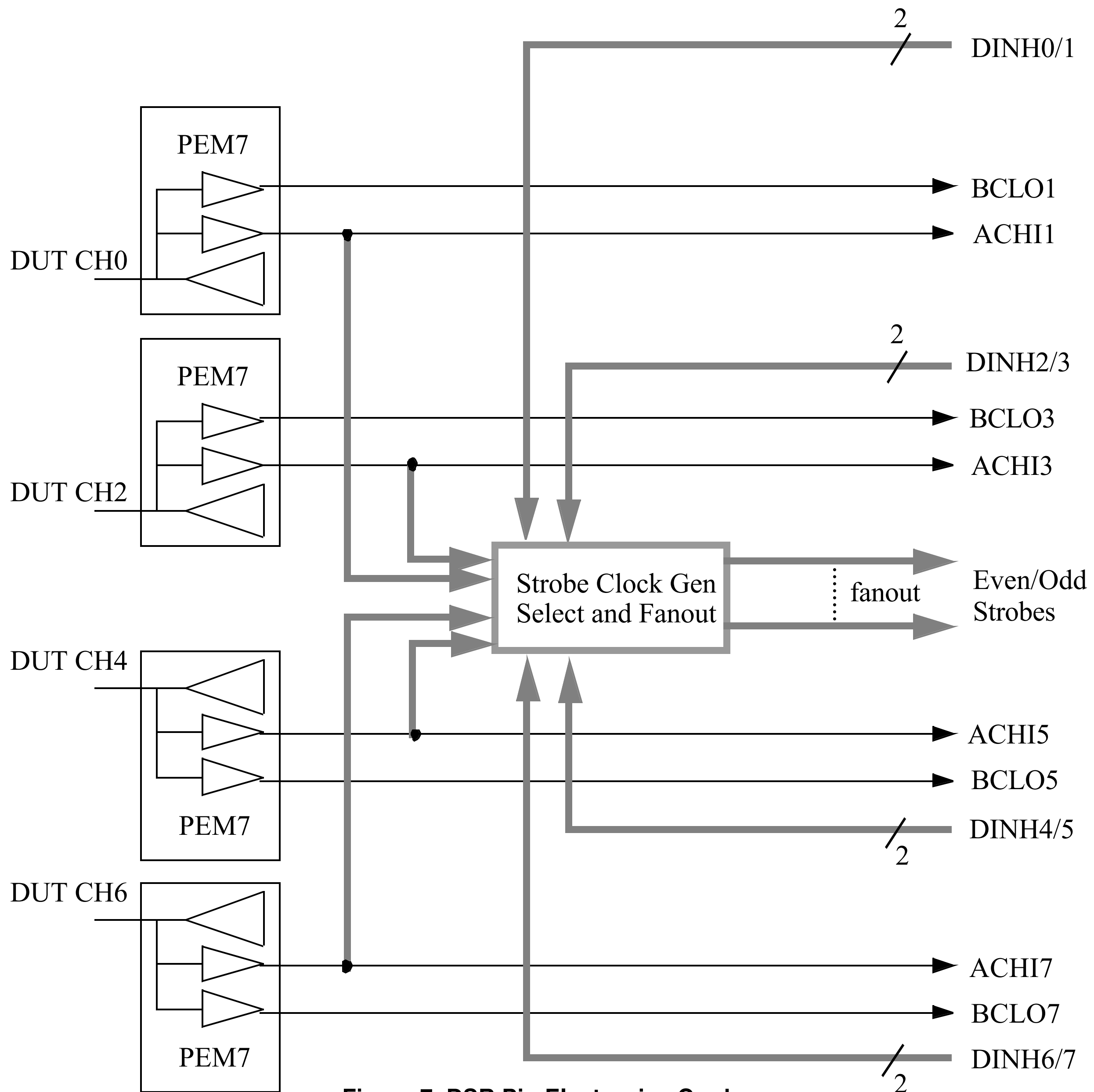


Figure 7. DSR Pin Electronics Card

implementation, the data strobe receiver in the test head and the SS pin slice in the main frame. There can be a maximum of eight DSR cards in the test head. As shown in Figure 6 the output strobes from a single DSR can be wired to a maximum of eight pin slices in the main frame. Each pin slice in the main frame supports eight tester channels. The length of the cables from the DSR cards to the main frame SS pinslices are made shorter than those from the PECs to the SS pinslices. This is done in order to make the data strobes from the DUT arrive at the main frame SS pin slice earlier than the digitized data bus signals from the PECs to the same SS pinslice. By using programmable delay lines, the data strobes may be located anywhere in the eye of the data bus signals, limited only by the range of the delay line avaialble.The SS pinslice contains the delay line for each pin and a latch which is clocked by the data strobe. The DSR and the SS pinslice are described in the following subsections.

3.1 Data Strobe Receiver (DSR)

The DSR PEC located in the test head receives the DUT clocks (also called data strobes) and implements the following major functions:

- Provides true differential AC and DC parametric capability for four DUT clocks.
- Generates new strobe signals from four DUT

clocks and fans them out to eight pin slices in the main frame. Strobe generation is selectable on rising, falling and both edges of the input clock with capability to divide the input clock by two.

The DSR block shown in Figure 7 is based on a differential pin electronics card, PEC7. The PEC7 card supports 8 differential channels using a custom differential pin electronics integrated circuit PEM7 [4]. The upper four differential pin-pairs of PEC7 are removed in order to implement the DSR specific functionalities. The lower four differential pin-pairs are preserved including all the DC and AC test capabilities.

Source synchronous clocks from DUT can be received single-ended or differentially with a 50 ohm termination to a user programmed V_T level. The above comparator high (ACHI) output of each PEM fans out to normal ACHI which is sent to its DSR pin slice in the main frame as in a normal PEC7, and to the Source Synchronous Strobe Generation block where new data strobes are generated and distributed to SS pin slices in the main frame. From each ACHI the following data strobes can be generated under software control:

- Rising edge Strobe
- Falling edge Strobe
- Both edges Strobe (Double Strobe)

Furthermore, the strobes can be divided by 2, again under software control. When the by-2 divider is used, the drive inhibit event signal, DINH, from the DSR pin slice is used to control the start timing of the division. Calibration ensures that the DINH event occurs at the correct time at the by-2 divider input. New strobes generated from any ACHI (one of the four) can be distributed to any of the eight SS Pin Slices in the main frame connected to this DSR. The strobe block generates even and odd data strobes for the SS Pin Slice from ACHI1 (ACHI3, ACHI5 and ACHI7). The reason for even and odd strobe generation is that each pin on the pinslice has a maximum test data rate of 800Mbps. The pinslice allows multiplexing of the odd and even channels to achieve 1600Mbps test data rate.The even strobe is used for even pins in the pinslice, and the odd strobe is used for odd pins in the pin slice. The fan out of the even (odd) data strobe is achieved by using eight identical 4:1 muxes, which select one of the four strobe inputs and drive the TH-cable to the main frame with a cable compensator. The strobe generation from ACHI can be disabled by software, which may be used to prevent unnecessary signals

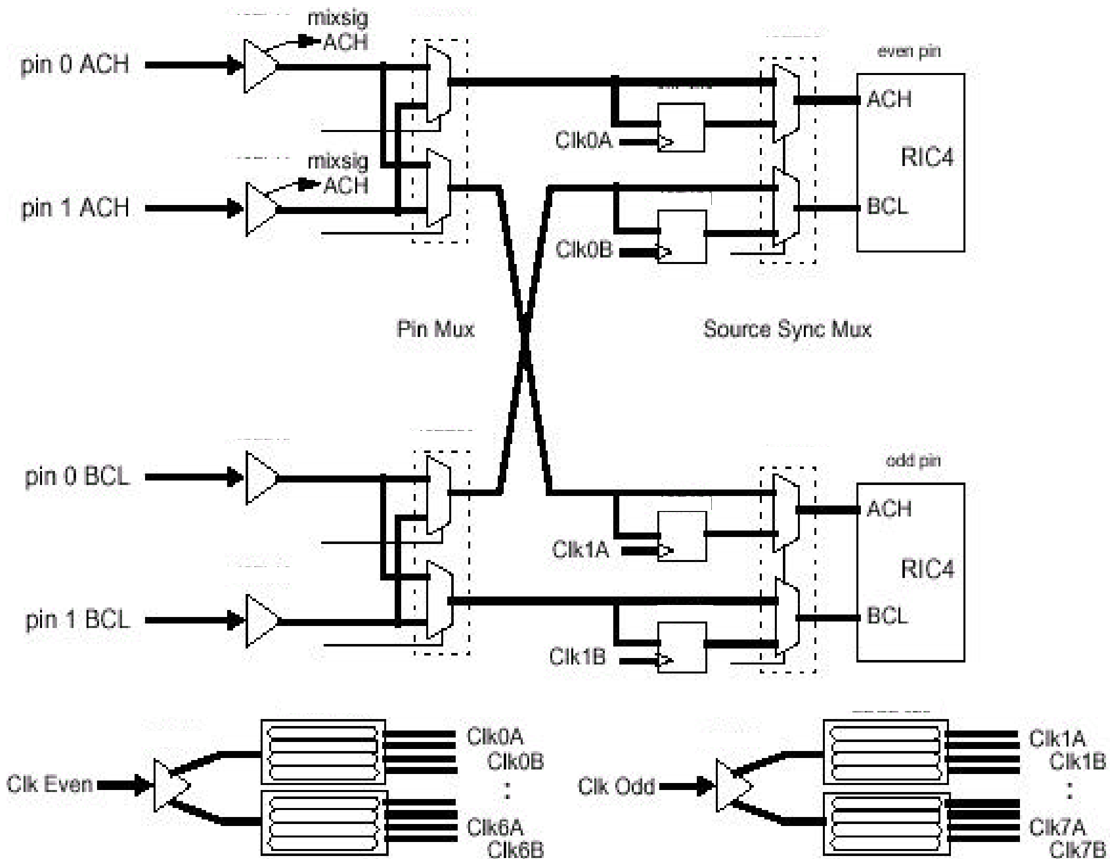


Figure 8. SS Pinslice Strobe Side Block

from being sent to SS Pin Slice when DSR is used in normal (non Source Synchronous) test mode.

3.2 Source Synchronous Pinslice

The Source Sync pin slice contains the main memory, subroutine memory, capture memory, timing generation and formatting circuits for eight device pins. The SS pin slice provides the same pin count vs. data rate flexibility of its predecessor, the Flex Mux pin slice, with the additional ability to test source synchronous devices. To reduce cost a SS pin slice can also become a dedicated Flex Mux Pin Slice by removing about 10 ICs. The SS pin slice is able to provide clock and data rates up to 1600 Mbps. Two tester channels are combined for clock or data rates greater than 800 Mbps. Figure 8 shows the compare side block of the pin slice, where the source synchronous test function is implemented.

The response IC RIC4 makes the pass fail decision based on the ACH and BCL inputs [5]. ACH and BCL signals are the digitized DUT outputs from the test head PEC hardware. In normal mode of operation, each RIC4 of each pin receives its own ACH and BCL data from the test head. In mux mode ACH/BCL data from an even or odd pin is copied to both the RIC4s. This allows the pin slice to strobe effectively at 1600Mbps data rate on either the even or odd pin. Source Sync function added to the pin slice consists of a source sync latch and 2:1 mux prior to each RIC4 and the addition of a delay line used to deskew the source synchronous channels and provide the user with source synchronous delay control. The even and odd clock paths to the Source Sync Pin Slice require deskewing. In addition, the deskew elements are used to shmoo and search the SS delay between the clock and data signals. Since the deskew elements are not linear, a look up table is used in order for the deskews to be programmed to the desired time.The resolution of the table is 2.5ps in order to meet the user requirement of 10ps.

3.3 Source Synchronous Operation

The simplified block diagram in Figure 9 shows the system described thus far. During SS operation, the SS pin slice receives the odd and even data strobes from its corresponding DSR card on the test head. The data strobe is used to latch the ACH and BCL data from the DUT's data bus pins into the SS latch.

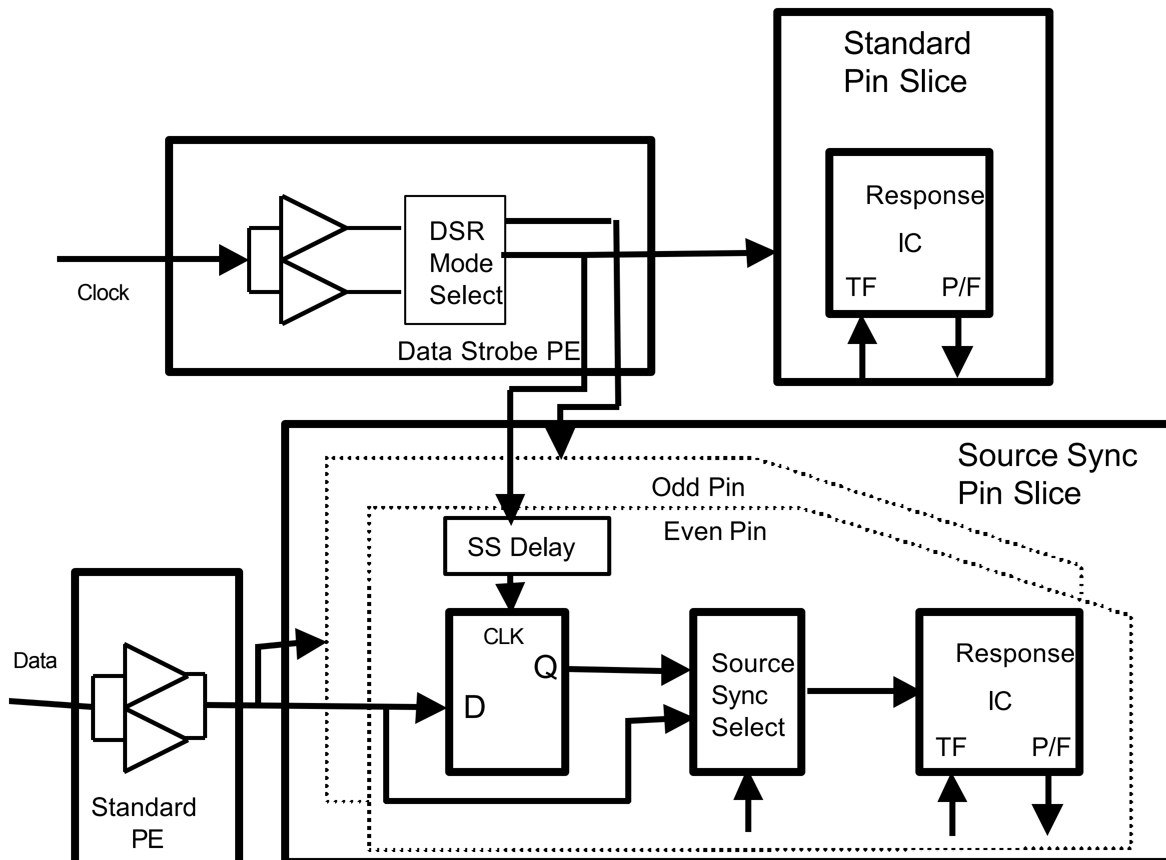


Figure 9. SS Option Simplified Block Diagram

The latch output is selected by the mux and sent to

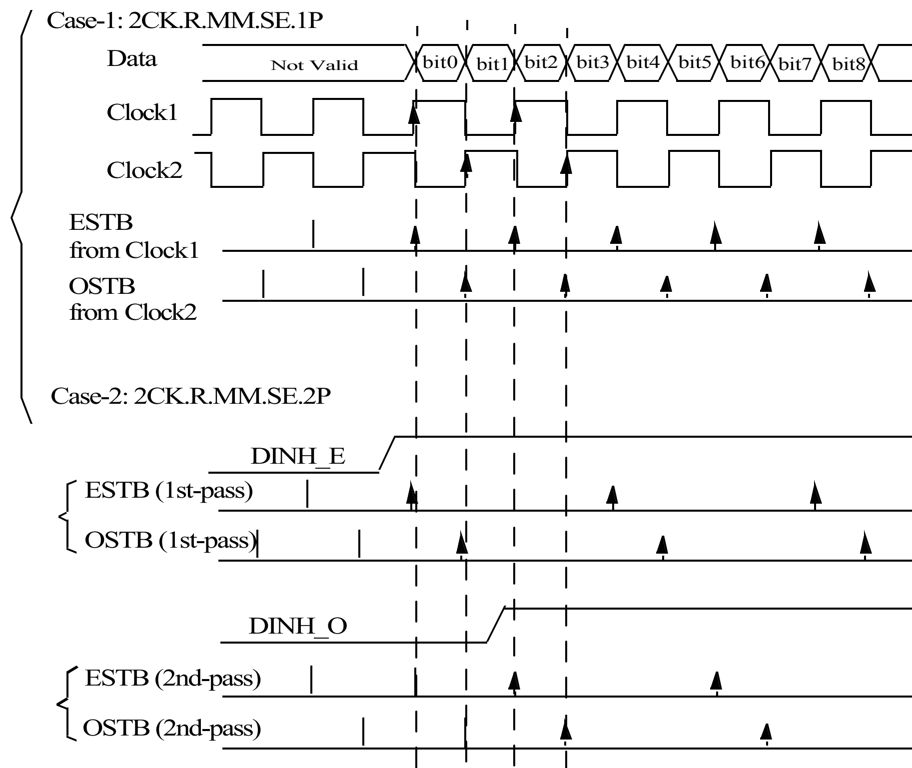


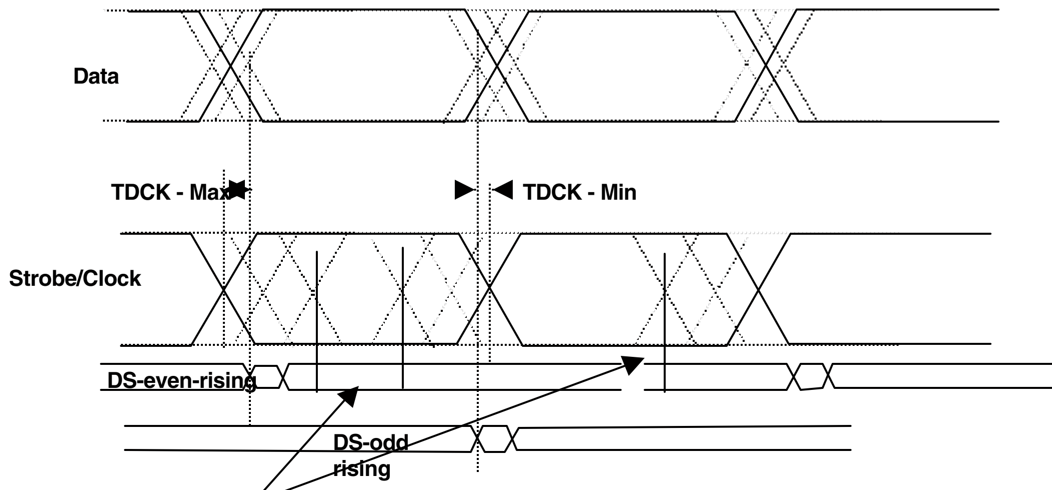
Figure 10. SS Operation 1600Gbps example

the RIC4 instead of the ACH/BCL output. The RIC4 tests the latched data for pass/fail decision. Depending on the mode of the DSR strobe generation, different types of source synchronous tests can be made possible.The simplest case is where a data transition accompanies every rising edge of two DUT clocks, clock1 and clock2. In this mode the SS test can run 1600Mbps data rate and the clock rate into the DSR is 800Mhz for each clock. The SS pin slice itself is set to mux mode, and the ACH/BCL from the data pin is sent to the even and odd channel RIC4. The even data strobe generated from the rising edge of clock1 will load even bits of data (bit 0, bit2 ...) in the even SS latch. The odd data strobe generated from the rising edge of clock2 will load odd data bits (bit 1, bit 3, ...) in the odd SS latch. The even and odd channel RIC4s will unload the latch every unit interval. This is shown in the Figure 10 case 1 (Two Clock, Rising Edge, Mux Mode, Single edge, 1 Pass). If the data and clock from the DUT were faster than 1600Mbps and 800Mhz rates, then the two pass strategy described next will enable SS test at higher than 1600Mbps data rates. Here the mode selection of the DSR is shown in case 2 of Figure 10 (Two Clock, Rising Edge, Mux Mode, Single edge, 2 Pass). Here the DINH even signal will reset the by-2 divider in the DSR so as to enable the data strobes to start coincident with bit0 and bit1. Furthermore, since the DUT clocks are divided by 2 the data bits 2 and 3 are skipped in the first pass and the sequence of bits tested is 0,1,4,5,8,9 ...etc.

In the second functional pass the DINH is delayed such that the data bits 2,3,6,7,10,11... are tested. So each SS latch is loaded every 4th UI thereby inreasing the jitter tolearnce of the SS test to high clock jitter.

3.4 Source Synchronous Hardware Calibration

There are three calibration steps which are specific to the SS hardware. They are performed during normal calibration of the tester. The delay line calibration performs calibration of the delay lines in the SS pin slice. These delay lines are used by the deskew calibration program to align the ACH/BCL source sync paths from the DSR cards in the test head. The ACH and BCL have three delays, a common fixed delay and per pin individual coarse and fine delay elements. The coarse and fine delay lines are fitted in series, and the combination provides 2.5ps step cal values. The DINH delay line calibration is performed in order to accurately enable the data strobes. There are eight DINH delay lines, four for the odd strobes and four for the even strobes. The DSR driver/comparator calibration is very similar to the calibration of the PEC7 card. It includes calibration of the differential driver and the calibration of the comparator in the three different modes: window, differential and common. All the calibration routines are run interactively or in batch mode and provide extensive data log information.



Since Data Strobe clock also jitters, Strobe latch can only be observed during “quite time”.

Quite time is data_bit_time - Clk_jitter p-p. 0r (2 * data_bit_time) - Clk_jitter p-p for Mux mode.

Tdck is the skew (delay) between Clock and the Data pins

Figure 11. SS Operation and Clock Jitter (Differential Clock)

3.5 Support Software For SS

The EXA3000 tester platform uses ASAP, a set of software tools for creating test programs and debugging device test issues. Existing ASAP tools and block structure language were enhanced to support development of test programs using the SS test option. Timingtool was modified to provide the main focus for development of tests for devices using source synchronous controlled data bus pins. It allows the user to specify the association between a data strobe pin and its data bus pins. It enables the different modes to be set up for data strobe pins. It also allows a timing parameter to be associated with the source synchronous delay line elements to allow the user to position the data strobe relative to the data eye. Timingtool and Scopetool use the fast acquire technique to display DUT waveforms [3]. They have been enhanced to acquire waveforms with and without source synchronous being enabled. Plottool, and searchtool provide features to aid the debugging of these types of tests. They allow plotting of the source sync delay parameter to measure Tva and Tvb spec values of the DUT. A new block syntax supported in the ASAP software allows the user to setup or change the conditions as well as the input data strobe selection for each output strobes. The selection of MUX pins and non-MUX pins is also supported in the software syntax. The software has programmable source sync latches to allow the user to enable or disable source sync strobe for each pin. If the source sync is enabled, the selected output data strobe compensated with the programmed delay value will be chosen for strobing. The normal strobe will be done if the source sync is disabled.

4 SS Architecture Comparison

The SS architecture presented is clearly the right test solution for source synchronous devices since device output clock triggers data strobes (DS) for the tester effectively strobing its own data outputs. In addition the device data output jitter is eliminated. Figure 11 shows how the tester strobe can be positioned to unload the SS latch during the quiet time. The clock and data jitter in a typical SS device environment. The device clock is converted to a data strobe and carries with it the jitter of the clock. The strobe latches the data into the SS latch in the SS pin slice. The amount of jitter in the clock will determine the "quiet time" when the tester can unload the latch. In a typical SS test, the tester strobe is placed in the middle of the "quite time." When running SS tests at > 800Mbps the mux mode is enabled and the DS even and DS odd steer the incoming data to the odd and even SS latch, doubling the amount of time available to place the tester strobe. In addition to this, two pass testing covered earlier essentially doubles the amount of jitter tolerance from +-1UI to +-2 UI. Consequently, no search is needed to locate the DUT output clock for every SS test. As compared to the capture method where pass/fail decision is made at the end of the pattern burst, in the SS option the pass/fail decision is on a per cycle basis and does not have the overhead of the capture. Clearly the SS architecture is better than the test methods used in the traditional ATE. There are other similar SS architectures, which use device gen-

erated strobes but are heavily pipelined which causes the data strobe generated in one cycle to test the data occurring several cycles later. This causes the DUT output data to be ignored in the very first few cycles of the SS test. It also mandates that the SS test needs to have the DUT provide output clocks at all test cycles so as not to mask additional DUT output data. If the DUT switches from input to output (transmit and receive data and clocks on the same lines) in SS operation, it will clearly be a test challenge.

5 Conclusion

In this paper we described the hardware implementation of the SS tester architecture and how it allows easy switching from SS test to conventional non SS tests. Prior to the new SS architecture, conventional

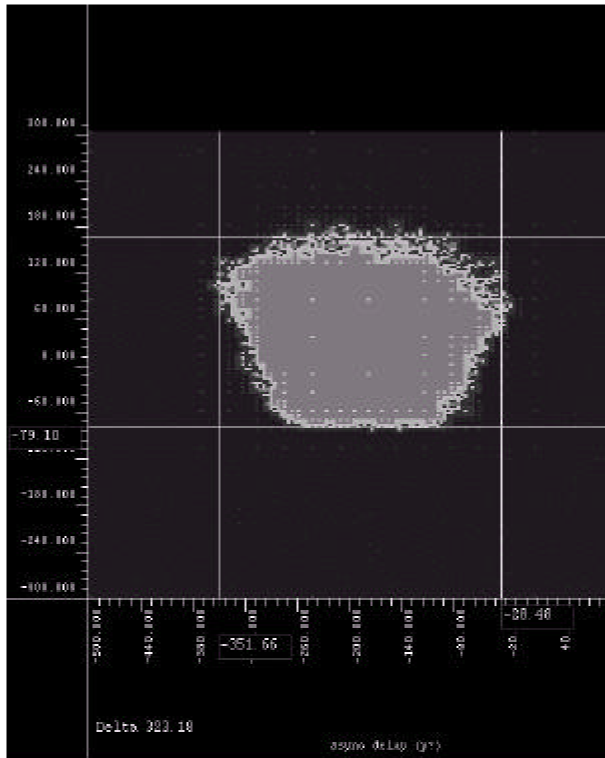


Figure 12 SS Strobing Enabled

ATE used search and capture methods to accomplish source synchronous device testing. These methods served well at low frequencies since the jitter of clock and data was a small fraction of the data bit width. As frequencies of SS busses increased, jitter of the signals made the validation of the devices more challenging until the arrival of the new SS tester architecture. The effect of this on device testing can be seen from improvement in the eye diagram shmoo plots from SS tests and the ability to characterize the source sync delay between clock and data. Figure 12 shows the improved eye diagram when source synchronous strobing is turned on. Figure 13 shows the same shmoo plot with source synchronous strobing turned off. This source synchronous tester architecture is being carried over to the next generation Sapphire architecture with increased performance capability to test 3.2Gbps SS devices.

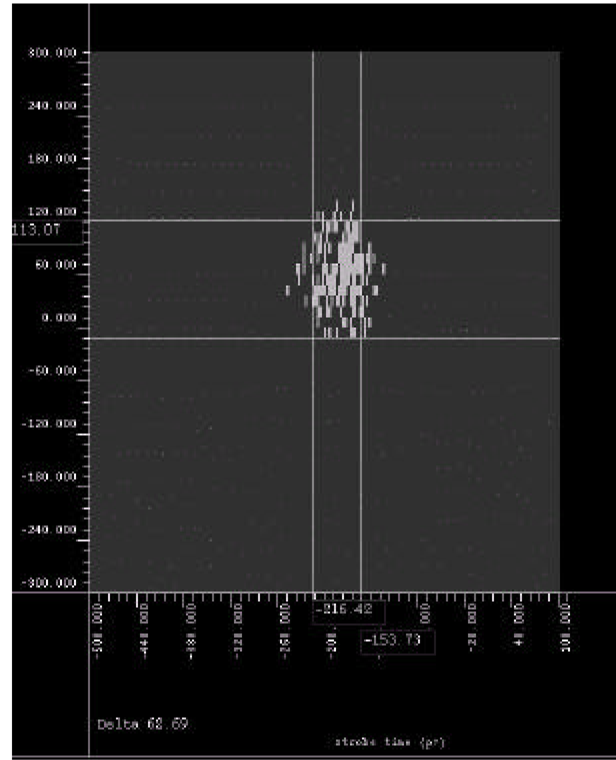


Figure 13 SS Strobing Disabled

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