# A Model-Based Test Approach for Testing High Speed PLLs and Phase Regulation Circuitry in SOC Devices

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***Abstract* – Future SOC devices will make extensive use of phase locked loops to either generate Gigahertz clocks on-chip or to adjust the phase of data signals in high speed IO links running at multiple Gigabits per second. The high speed analog nature of the circuitry requires a dedicated test strategy to obtain fault coverage particularly for parametric defects affecting jitter performance. While traditional specification oriented test methods require a complex setup of additional instrumentation, this paper describes a completely new model based approach using existing capture and compare equipment available with ATE. The methodology proposed in this paper performs a test by verifying the frequency domain model of the phase regulation characteristic developed during the design phase of the circuit. The method scales in performance and accuracy with leading edge measurement equipment such as ATE and BERT.**

### *Introduction*

With the introduction of sub-micrometer technologies, the rapidly increasing complexity of digital devices enforced a change in test strategy from a functional to a structural approach. Meanwhile, scan based testing is the dominant structural test that is also fully supported by EDA tools. Many applications leave the test floor without being functionally exercised at all. The manufacturing yield of those devices is assumed to be mainly determined by random defects that are detected from scan tests based on logical fault models.

SOC integration that started with the deep submicron technologies a few years ago, allowed the embedding of significant amounts of analog and RF circuitry into complex digital host designs. In contrast to the digital portions, the analog circuitry can rarely be reconfigured to test correct manufacturing of the analog circuit elements in a structural way as with digital logic. This means that correct manufacturing is still validated by measuring parametric performance of the whole functional block, followed by a comparison to specifications.

Therefore, the manufacturing yield of SOC devices containing analog and RF circuitry is not determined only by pure random defects that cause hard failures. It is also significantly affected by parametric failures that manifest themselves with functionality outside of specifications. Furthermore, the parametric failures in analog circuitry are much more dependent on process variations with respect to the targeted analog functionality, in contrast to logical failures in digital circuitry. Thus, the testing of analog and RF performance parameters requires expensive equipment which is tailored to the specific functionality and consumes a lot of test time.

The phase locked loop had been among the first analog circuits that got embedded into upcoming SOC applications. Initially, a PLL was used to provide a high speed on-chip clock for the digital units that was difficult to be supplied from externally. In the meantime, the number of independent clock domains for purely digital SOC devices grew rapidly. In the advent of core based SOC designs, it was simply impossible to clock the whole device from a single clock with minimum clock skew. Therefore, multiple clock domains became very common introducing completely new test challenges.

Recently, with the disruptive introduction of high speed IO interfaces based on asynchronous serial communication, the need for additional clock domains and local clock generation sky-rocketed. Even though an IO interface shares a PLL among a couple of IO macrocells for outbound data transmission, inbound data transmission requires either a PLL or DLL based clock recovery, in case of clock-less transmission, or a DLL based skew adjustment for buses that use source synchronous clock forwarding. Both imply the use of the phase regulation circuitry on a per bit line basis and therefore form a clock domain for each data line. The consequence of this change in IO technology is a significant increase of the analog circuit content, even in pure digital designs. The complexity of the high speed phase regulation circuitry is even more aggravated by requirements for meeting FCC regulations for unintentional radiation. This leads to the new concept of spread spectrum clocking where the clocks for transmission of data across an IO interface are modulated at low frequencies to avoid spectral concentration of energy in the emitted radiation.

The massive use of PLLs also changed the device specification strategy and thus the test approach, particularly for high speed IO interfaces. Whereas pure PLL parameters such as loop bandwidth rarely appear in data sheets, parametric performance in terms of eye opening and jitter are getting more and more ubiquitous. Again, these parameters are extremely sensitive to process variation and the overall device yield is significantly determined by parametric failures. The prevalent test strategy in turn is based on validation of specifications and thus tremendously increases the cost of test.

***The model based test approach***

The cost pressure on low cost SOC applications caused the industry to spend a high effort on finding alternatives for cost efficient testing of analog and RF circuitry. Whereas efforts for structural test approaches didn't make significant progress, a new methodology called model based test grows in importance, because it seems to be a promising candidate to provide a more cost-efficient alternative compared to the verification of analog device specifications.

The model based approach tries to make use of the a-priori knowledge that exists from the design phase. Conventional testing that is aimed at verifying specifications rarely exploits the design knowledge of internal analog blocks. In case of high speed IO interfaces, parametric performance like eye opening is verified without taking into account the behavioral design data of the phase regulation circuitry that may cause a transmit data eye to close or a receive clock recovery being unable to tolerate incoming data jitter.

With the model based test strategy the measurement goal is to validate a behavioral model of the given analog circuitry during test as simulated during the design phase. As soon as the model behavior is validated in reality, specifications can simply be computed from the valid model and compared to the specs. This avoids the direct measurement of the specs that may contain a lot of redundancy and thus might be more time consuming and costly.

However, a key requirement to be successful with the model based test approach is that a measurement method can be found, able to validate a given behavioral model with existing equipment. Furthermore, it should be possible to implement the method in a way that is compliant with today's manufacturing test requirements in a cost efficient way.

***The model based test approach for PLLs***

PLLs typically use the advantages of leading edge technologies to generate highest frequency clocks locally on-chip from relatively low frequency reference clocks supplied externally. A phase locked loop (PLL) is constructed around a voltage controlled oscillator (VCO) covering a certain frequency range around the target frequency and a phase/frequency detector followed by a loop filter that shapes the frequency response to achieve a fast but stable regulation [1], [2]. In cases where the high speed clock is already supplied externally and the regulation is restricted to adjust the phase only, a delay locked loop (DLL) concept is used for alignment between clock and data. The DLL is designed around a voltage controlled delay line instead of the VCO and uses only a phase detector followed by a loop filter to form the phase regulation loop [3].

Both, the PLL and the DLL, are typically designed based on models for the phase regulation characteristic in the frequency domain. The most simple and therefore most commonly used model is the linear model that allows a relatively simple description of the phase transfer function in the frequency domain, following the rules of linear time invariant systems. Using the Laplace transform the phase/frequency responses are calculated for various excitations such as step, ramp or sinusoidal stimulus [1], [2].

Since high speed phase and frequency regulation circuitry has to operate at the limits of the given technology, the complexity of the VCO or delay line, the phase detector with its charge pump and the loop filter are kept relatively simple. For example, a high speed PLL typically uses a simple lag-lead loop filter of first order, constructed from passive elements (figure 1).

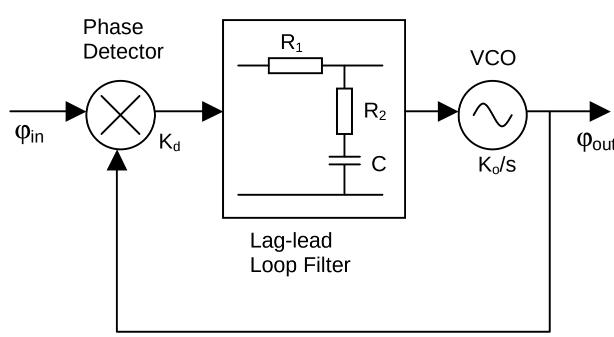


Fig 1.: PLL with second order lag-lead loop filter

The above example of a second order PLL can be described by the following linear model [1]:

$$H(s)=\frac{s\left(2\zeta\omega_n-\omega_n^{\ 2}/K_0K_d\right)+\omega_n^{\ 2}}{s^2+2\zeta\omega_n s+\omega_n^{\ 2}}$$

with the following model parameters:

$$\omega_n=\left(\frac{K_0K_d}{\tau_1}\right)^{1/2}$$
$$\zeta=\frac{1}{2}\left(\frac{K_0K_d}{\tau_1}\right)^{1/2}\left(\tau_2+\frac{1}{K_0K_d}\right)$$
$$\tau_1=(R_1+R_2)\cdot C$$
$$\tau_2=R_2C$$

$\omega_n$ is called the natural frequency of the PLL and $\zeta$ is the damping factor.

In case of a high gain loop ($K_0K_d >> \omega_n$) the phase transfer characteristic simplifies to:

$$H(s)\approx\frac{2\zeta\omega_n s+\omega_n^{\ 2}}{s^2+2s\zeta\omega_n+\omega_n^{\ 2}}$$

Figure 2 shows the resulting phase transfer characteristic according to the above model.

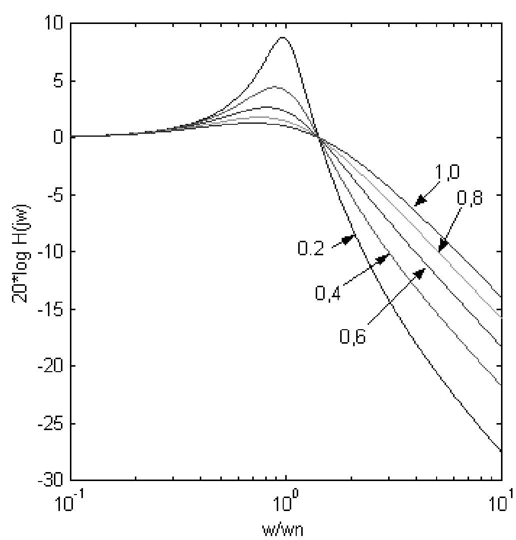


Fig. 2: Linear model based transfer characteristic for a second order PLL with high loop gain for different damping factors $\zeta$.

With the above or a similar model describing the phase transfer characteristic of a PLL or any other phase regulation circuitry, the fundamental behavior can be described qualitatively as follows:

1. For low frequencies the circuitry will pass phase variations with minimal attenuation (pass-band or in-band region)
2. Close to the bandwidth corner it may slightly amplify the phase variations (peaking region)
3. Beyond the corner frequency high frequency variations will be attenuated with a certain roll-off (out-of-band region)

Given this fundamental behavior, a test strategy that checks this behavior based on the mathematical model can be defined. The test strategy aims at verifying that these 3 regions exist and a representative value for the phase transfer function can be measured. In case the peaking is not relevant, the peaking region can be omitted reducing the test goal to verify only the in-band and out-of-band region.

This leads to the test requirement of measuring the phase variations at the output of the circuit while a certain amount of phase variation is injected as stimulus with a subsequent comparison against the model based data at given frequency points in the respective regions. It would be advantageous with respect to test time, if the response could be measured and compared simultaneously for several frequencies using a multi-tone stimulus.

Assuming that PLLs and/or DLLs are embedded in a SOC circuit massively in parallel, it is rarely the case that the high speed clocks are directly available for test purposes externally. Furthermore, a direct measurement of the phase transfer characteristic is not applicable for volume testing because of the complexity of the required setup and the long test time. Therefore, a test method must be found that allows the use of equipment existing in the manufacturing test environment and simultaneously achieves pass/fail decisions in test times acceptable for manufacturing test.

A test method that fulfills these criteria is the spectral analysis of the error density using capture and compare equipment like a BERT or ATE [4], [5]. When a sinusoidal phase variation of a certain amplitude and frequency is injected into the reference clock, it will be transferred according to the phase transfer characteristic into the output clock. When the output clock is used to either serialize or de-serialize data, the phase variation is also present in the data and therefore visible at the IO interface (figure 3).

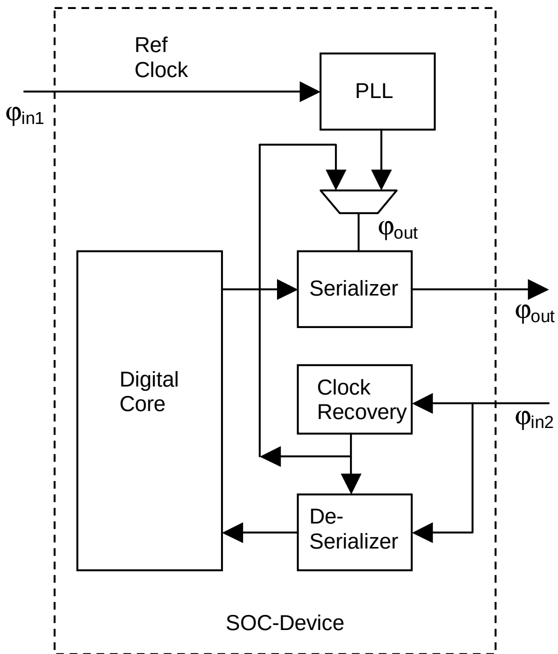


Fig. 3: Input and output of phase variations accessible at the IO interface.

Transferring random data across the IO interface causes the data eye to close according to the amplitude of the injected phase variations. When the data or clock signals are compared to expected data and the strobe point is moved to the crossover of the edge transitions, errors appear with a density that depends on the amplitude of the transferred phase variations. Furthermore, it is essential for the method that the density of the errors is linked to the periodicity of the phase variations. This is illustrated in figure 4 on the following page.

The proposed method requires a wideband random phase variation to be present in the clock or data signal to ensure linear mapping of the spectral energy of the injected sinusoidal phase variation. Capturing and comparing data in the crossover of the edge transitions generates a random binary error signal with a constant error density. In case a sinusoidal phase variation is superimposed on the random portion, it will modulate the error density proportionally. Thus, the spectral components of the sinusoidal portion will be linearly transferred into the error density signal. Then, the energy of the sinusoidal component can be extracted easily from the spectral power density calculated from the error signal.

Using the error density method, both parameters contained in the model for the phase transfer characteristic (phase variation amplitude and frequency) can be determined. Therefore, when a multi-tone signal covering at least the 3 essential behavioral regions is combined with broadband noise as a stimulus signal, the spectral content of the error density captured at the output will reflect the frequency dependent attenuation in the respective frequency bin according to the modeled behavior in the in-band-, peaking- and out-of-band region of the PLL. Using a single shot capture and compare at the output allows to efficiently generate the error density signal that is then transformed into the frequency domain using a discrete Fourier transform. Comparing the spectral energy for the respective frequency bins with the model behavior finally leads to pass-fail results that can be used to prove the validity of the model.

In a very simple case, a multi-tone stimulus is setup such that the stimulus signal consists of a mixture of 3 frequencies plus a broadband noise signal: a very low frequency component in the in-band region, a component at the corner frequency and a component at very high frequency in the out-of-band region. The amplitudes are chosen such that they reflect the inverse of the respective phase transfer characteristic as given by the phase regulation model. This compensates the different attenuation and eases the processing for pass-fail decisions. The phase variation signal is generated from an arbitrary waveform generator (AWG) and is used to modulate the reference clock when passing through a delay line (figure 5).

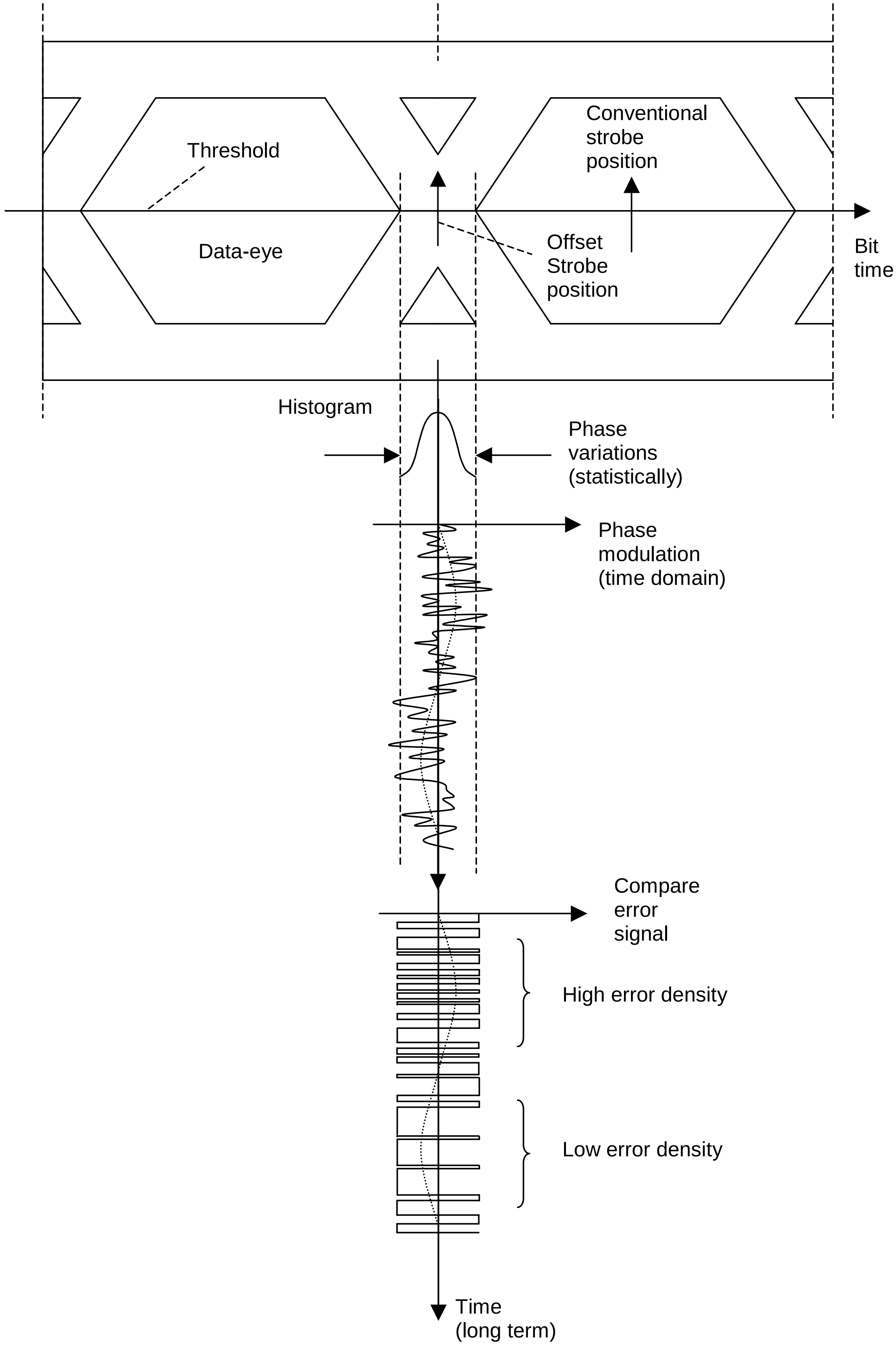


Fig. 4: Mapping of amplitude and frequency of phase variations into an error density signal

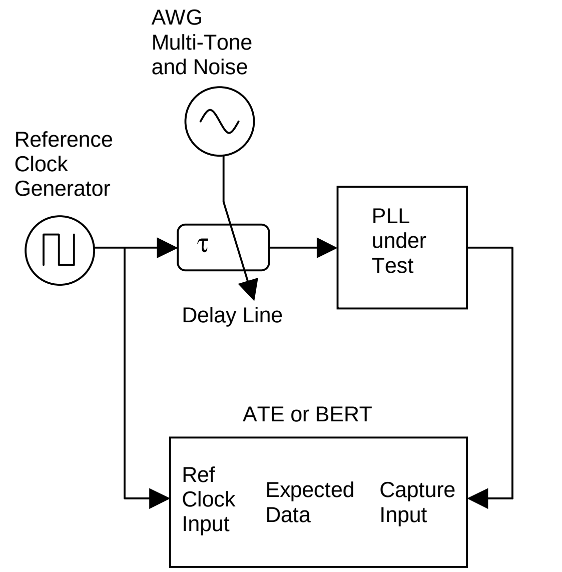


Fig. 5: Stimulus generation and error analysis

Using the composite stimulus, we expect that the output phase variations appear with equal amplitude for each multi-tone frequency according to the model and thus are visible in terms of a respective spectral content in the error density. The test finally verifies that the spectral multi-tone energy components appear in the respective frequency bins within a certain tolerance band (figure 6).

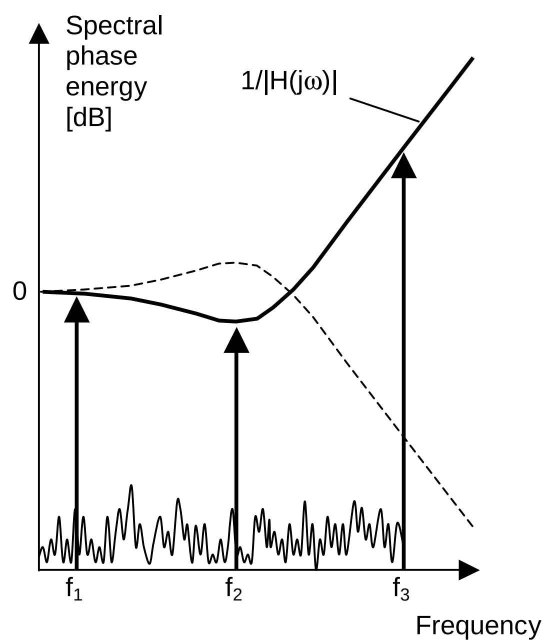


Fig. 6: Model based multi-tone stimulus combined with noise.

### *Measurement results*

For verification of the method, the PLL of a 3.125Gbps IO interface was analyzed. As stimulus source and measurement equipment an ATE (Agilent 93000 XP including the 81250 ParBERT) with phase modulation capability (modulated delay line) and capture and compare capability of up to 13Gbps was used. The phase modulation signal was generated from an AWG with 80MHz bandwidth (Agilent 33250A). A 156.25MHz clock signal from a low phase noise clock generator (Agilent E4422) was modulated with the AWG signal and used as reference clock to the IO interface of the device. The phase output was observed at the transmit output of one of the 3.125Gbps IO channels of the device.

As a model for the PLL behavior we assumed a 2nd order linear model as described above. Even in a case where no or only vague parameters for the model equation exist, the spectral error density method can be used for extraction of the parameters $\omega_n$ (natural frequency or bandwidth) and $\zeta$ (damping). For this purpose, we injected a white noise jitter with the AWG into the reference clock. The white noise jitter is shaped by the PLL and therefore the jitter spectrum measured with the spectral error density method at the device output conveys the complete PLL transfer characteristic (fig. 7). Subsequently we deployed a non-linear LMS-fit algorithm to vary $\omega_n$ and $\zeta$ until the model equation fits to the measured data in the least mean square (LMS) sense. We analyzed 3 different commercially available fitting algorithms (Trust-Region, Levenberg-Marquardt and Gauss-Newton) and for all 3 we found good convergence and robustness with different sets of measurement data and starting conditions.

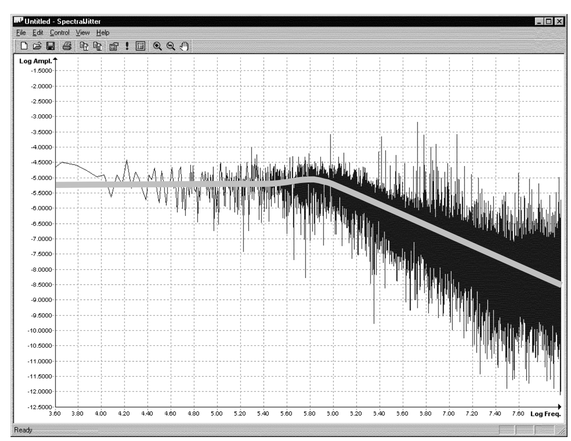

Fig. 7 Measured phase response of the device to a pure 80MHz white noise jitter and the respective LMS-fit of the model equation

With the knowledge of the model parameters, 3 additional multi-tone components were defined to compose the final phase stimulus signal. In the given case ($\omega_n$≈1MHz), the multi-tone input was chosen to be at $\omega/\omega_n$ = 0.2, 1 and 5 and the amplitudes were chosen to follow the inverse characteristic of the model ($V/V_0$=1, 0.7, 4). Since additional white random phase noise with the same overall energy is required, white noise with an rms amplitude of $4*V_0$ rms was superimposed to the multi-tone signal.

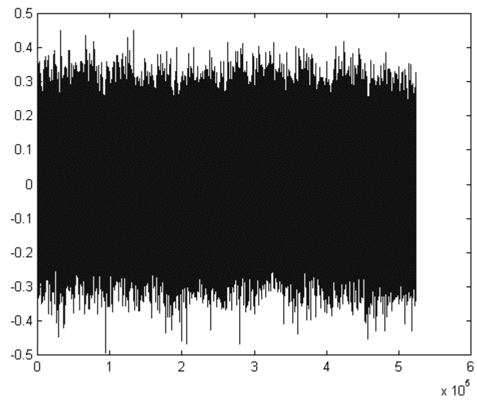

Fig. 8: Multi-tone phase stimulus with superimposed white noise

The time domain representation of the resulting phase stimulus is show in figure 8. The respective histogram is shown in figure 9. From both graphs it becomes evident that the sinusoidal multi-tone components are completely buried in the noise when displayed in the time domain. In the spectral domain, the noise energy spreads over the whole spectrum, significantly reducing the spectral energy per Hertz, whereas for the multi-tone spectral components the energy remains concentrated in single bins according to figure 6. As a consequence, the signal-to-noise ratio is significantly improved in the frequency domain and the evaluation and comparison of the multi-tone spectral components to pass/fail limits can be done in a much more reliable way.

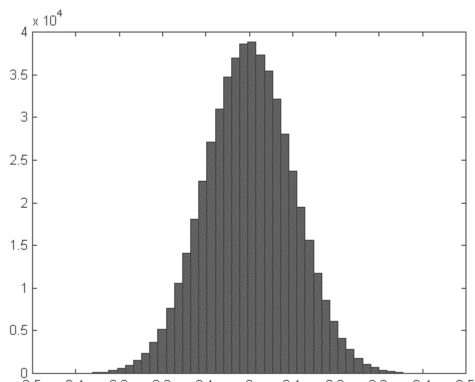

Fig. 9: The statistical representation of the injected phase stimulus is dominated by the superimposed noise component and therefore only shows a Gaussian profile

Since the method is based on the analysis of the error density, the next step is to capture the output data in the cross over of the edge transitions. This is equivalent to a strobe offset of 0.5 UI (unit intervals) to the center of the data eye. In our setup 512kbit were captured and compared at-speed in one shot to expected data stored in the tester. A large sample set is required to also include the very low frequencies. Fig. 10 shows an excerpt of the compare error signal uploaded from the instrument for further post processing. Since the random phase noise dominates the overall phase variations, the error signal does not differ significantly from a random binary signal in the time domain.

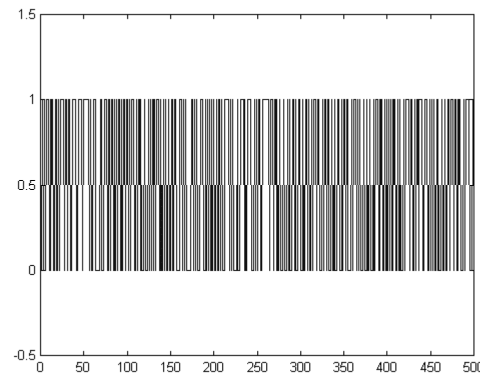

Fig. 10: A subsection of the compare error signal as a result of the composite multi-tone/noise phase stimulus

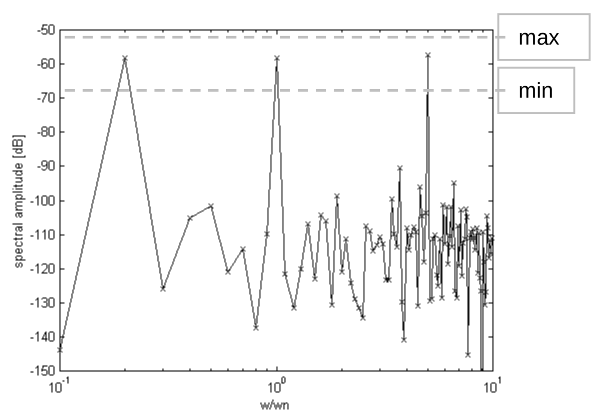


Fig. 11 The spectral analysis of the error signal clearly shows the 3 multi-tone peaks with equal height

However, as soon as the spectral power density is calculated from the error signal, the multi-tone spectral components clearly re-appear out of the noise. The injected multi-tone components are attenuated according to the PLL phase transfer characteristic. Since the attenuation is compensated by the intentional model based shaping of the multi-tone amplitudes, the resulting peaks in the spectrum appear with equal height and therefore can easily be compared to pass fail limits provided in terms of min./max. thresholds (figure 11). For production testing, the evaluation of the spectrum can therefore be restricted to just 3 frequencies.

The signal-to-noise ratio required to precisely identify the multi-tone signal in the noise strongly depends on the number of bits captured. The above data result from a sample set of 512kbit of captured data. Increasing the number of captured bits as well as performing spectral averaging further improves the signal-to-noise ratio but also increases the test time. Both parameters therefore need to be carefully balanced depending on the required accuracy and repeatability requirements.

Even though the described experiment used a multi-tone phase stimulus signal composed of 3 spectral components, the method is not restricted in terms of number of spectral components or shape of the deterministic input to validate the model of the phase transfer characteristic. Since post-processing is done after the upload of the compare error data on the tester's controller, a high degree of flexibility exists for using different post-processing algorithms without significantly increasing the test time. However, care must be taken to keep the balance of the energy in the random noise component and the deterministic signal to always ensure that the noise distribution covers the range of the deterministic signal amplitudes allowing the use of a single threshold compare for linear mapping into a respective error density. If this criteria is not met, harmonic distortion may occur. This becomes easily visible when just one sinusoidal frequency is used and no noise is added. In such a case the error density will vary according to a square wave resulting in harmonic components in the power density spectrum of the error signal.

***Comparison to other measurement methods***

Other traditional methods, commonly known for verification of phase regulation characteristics of PLLs and DLLs, are the use of network analyzers, time interval analyzers (TIAs) and high bandwidth oscilloscopes. With respect to the use of instrumentation for automated test, a key aspect is parallelism and throughput. High speed IO interfaces are embedded into SOC massively in parallel and require the validation of up to hundreds of IOs in parallel to ensure full fault coverage. The use of instruments with only one or few measurement channels may be a help for generic characterization of macrocells but can't be used for automated tests with the goal to achieve high fault coverage. The use of switch matrices to connect multiple device pins to much fewer instrument channels is not a viable option, since it is limited by the additional signal degradation, the switching time and the maximum number of switch cycles until preventive maintenance. The proposed method however, when implemented with regular ATE high speed pin electronic or a highly parallel BERT, satisfies the need for high parallelism and throughput.

Another limiting aspect for other methods is the fact, that typically the high speed bit clocks used for clocking out or sampling the data are not accessible through the device pins. Since the high speed NRZ data signals show a broadband spectrum the direct use of frequency domain measurements on data signals does not reveal any jitter or phase noise information. Using clock like data may help to identify spectral components of jitter and phase variations in terms of discrete side-lobes to a carrier signal but excludes the pattern dependency of the regulation characteristic. This aspect often prevents the use of networking analyzers for the test of PLLs and DLLs.

Software algorithms in modern high bandwidth real-time oscilloscopes also offer spectral jitter analysis. Data transitions extracted from the sampled signal waveform segment are compared to a reference clock and the time interval error is Fourier-transformed to obtain a jitter spectrum. The measurement of a high speed PLL characteristic starting at a frequency of about 1% of the PLL bandwidth requires the analysis of more than 100k transitions. Since oscilloscopes can record only a certain number of samples per waveform, the number of transitions that can be extracted is in turn limited to a fraction of the recorded sample size. Aside of the missing parallelism and throughput, real-time scopes therefore are additionally limited for the lower frequencies in the spectrum.

Modern versions of TIA also offer algorithms for analyzing the frequency characteristic of jitter. Typically, the time interval between a reference transition in a data pattern and the transition after skipping N-1 subsequent transitions is measured. A statistically representative number of M measurements of this type is performed for each N, resulting in jitter values versus the N-th transition. Performing a Fourier transform on this function also yields spectral information on the jitter and may give insight into the frequency characteristic of the phase regulation circuit. However, in order to obtain a complete spectrum from N transitions, MxN measurements have to be performed including a hold time of typically more than 1us between each measurement. The proposed method however, captures and compares all transitions in a single shot, at-speed. This throughput advantage, again combined with the much higher parallelism compared to a TIA instrument and the advantage of re-using existing instrumentation in ATE offers the higher value.

Furthermore, the maximum data-rates for both, real-time oscilloscope as well as for TIA typically lags the development of simple capture and compare equipment such as BERT and ATE. With PLLs and DLLs used in leading edge data communication devices operating at speeds beyond 10Gbps, capture and compare is the only available solution. Since the proposed method is based on this instrumentation, it simply scales with its maximum data rate and performance.

As the proposed method is based on capture and compare operation, its accuracy is mainly linked to the performance of the instrument's sampling accuracy. In case the sampling process includes internal jitter, it will limit the measurement accuracy, particularly when it is broadband random jitter. In case the internal sampling jitter is strictly periodic, it will become visible in the same way as the external periodic jitter in a true measurement signal. When the spectral component of interest does not coincidence with the frequency of the internal jitter, it will not affect the measurement accuracy. Therefore, the total measurement accuracy is given by the internal random jitter performance of the used equipment. For a high end 13Gbps parallel BERT the jitter accuracy ranges down to 1ps rms. The capture memory allows to capture up to 64Mbit of data at speed, corresponding to a minimum jitter frequency of 150Hz. The data upload and processing time strongly depends on the minimum frequency to be processed (the number of bits to be captured) and ranges from a few msec (kHz range) up to several seconds (hundreds of Hz) per channel.

***Summary***

We have successfully demonstrated the employment of a new model based approach for testing phase regulation circuitry such as PLLs and DLLs using existing capture and compare equipment. The presented work shows that it is possible to extract model parameters from an analytical description of the phase regulation characteristic as used during design. For parameter extraction a fitting algorithm was used in conjunction with frequency domain data obtained from a modified BER measurement using existing capture and compare equipment. The parameters were subsequently used to define a model based multi-tone pass/fail test with focus to higher throughput. This strategy reduces the test goal to the pure validation of the phase regulation model for each device under test and therefore has the potential to obtain a high fault coverage in less test time compared to measuring direct specification parameters such as a complete jitter transfer characteristic.

Since PLLs and DLLs will be used in rapidly growing quantities in SOC designs, the new method helps to reduce test cost and the complexity of the required test equipment. It allows a more flexible use of already existing equipment and helps to simplify the test setup and tester configuration.

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