Delayed-RF Based Test Development for FM Transceivers Using Signature Analysis

Erkan Acar and Sule Ozev
Duke University
Durham, NC 27708
{ea5, sule}@ee.duke.edu

Abstract

We present an automatic test development methodology for FM transceivers based on frequency-domain signature analysis and delayed-RF set up. We develop two distinct pass/fail criteria based on eigensignatures and envelope signatures and a test generation algorithm that aims at minimizing the required delay while attaining full coverage of target faults. We develop a fault injection and simulation platform for a VCO-modulation, low-IF transceiver architecture using MATLAB and behavioral models including non-ideal response. The proposed methodology enables the automation of the test generation process, thus reduces the test development time. Experimental results have shown a 90% reduction in the required delay thereby reducing the cost of this test hardware item.

1. Introduction

Increased proliferation of radiofrequency (RF) systems into the electronics market drives the semiconductor industry to search for cost-effective solutions for RF manufacturing. While RF design techniques and process technology have improved considerably, increasing cost-efficiency, the so-called *back-end* issues of testing and packaging have become an increasing percentage of the overall cost. High steady costs of test equipment [16, 17, 4], long test development and application times [5], and the increasing cost of RF packages [15, 20] compared to the decreasing cost of silicon all contribute to this trend. As an example, even with outsourcing production testing to distant locations where tester operation is more cost-efficient, the cost of a single second on a $3 million RF tester still comes to around a dime [16, 4]. As such trend is economically unsustainable, radically new approaches are needed for the testing of RF systems, both after packaging and at the wafer level.

Traditionally, RF systems have been tested through measurement of their performance parameters, such as path gain, noise figure, and third order input intercept, which are specified under certain environmental conditions. Such testing requires not only specific, high calibre test equipment, but also unacceptably long test times. In most cases, generation of modulated signals to duplicate the operation environment creates a need for application-specific pieces of test equipment, exacerbating cost [7, 8].

To attack the problem of ever increasing RF testing and packaging costs, several research venues, such as development of lower cost RF test equipment [21], development of test methods that lower reliance on high-cost and specialized test equipment [4, 3], development of design-for-testability methods and incorporating RF testing at the wafer level [15], and automatic test development [5], have been investigated.

In order to reduce the test development time for RF receivers, the authors propose an automated scheme in [5]. The test signal is specified as a multi-tone sinewave. The test attributes in terms of the frequency and the power of the tones are determined through a search-based algorithm so as to compute the gain and the third order intercept with minimum error. In [21], an RF signal source based on an all-digital PLL bank is presented. The source is capable of generating single-tone, multi-tone, and modulated RF waveforms making it useful for reducing the cost of RF receiver testing where the test input is at the high frequency domain and the output response is in the low frequency domain.

In [4, 3], the authors propose to push most of RF tester functionality onto the tester boards, thereby generating a specialized RF test equipment out of an ordinary mixed-signal tester. As it is much easier to re-design the test board as opposed to buying a new generation RF tester with each product cycle, this approach is promising in reducing the reliance on high-calibre test equipment.

Development of design-for-testability (DFT) approaches has not been attracted much attention for RF circuits due to concerns about the silicon estate, additional pin requirements, and most importantly, performance degradation [4]. RF paths are extremely sensitive to loading and noise injec-

0-7803-8580-2/04 $20.00 Copyright 2004 IEEE

tion thereby making any modifications to the RF path utterly undesirable. However, most transceivers today include a vast amount of digital control to enable channel searching, frequency hopping, and gain control, creating an excellent opportunity for improving testability without modifying the RF path. In [15], an RF test platform based on injection of a delay into the loop-back connection with an associated all-digital DFT approach has been introduced to enable low-cost wafer level testing for frequency modulation (FM) transceivers. The amount of the required delay to enable the measurement of several performance parameters is computed and this method has been shown to detect catastrophic faults in the RF path.

In [15], the optimum delay is determined to enable a set of performance measurements. In a production test environment however it is essential to decide on the acceptability of the die in the shortest period of time using the least costly test hardware. In this regard, direct measurement of the performance parameters may not be necessary as long as the testing scheme ensures identification of dies that do not satisfy performance requirements.

In this paper, we present an automated test development methodology based on frequency domain signature analysis and the delayed-RF set-up [15] to enable cost-efficient go/no-go production testing of FM RF transceivers. Instead of directly measuring the performance parameters, we use signature-based pass/fail criteria to achieve efficiency both in terms of test resources and test development time. The parameters of the test set-up, the injected delay, the offset between the transmit-0 and transmit-1 frequencies, and the bit pattern are determined so as to detect both hard and soft faults in the RF path. Nonidealities, such as nonlinearity, noise, and parametric variations are incorporated through injection of gausian noise sources, high-level behavioral modeling, and Monte-Carlo analysis.

2. Background: Delayed-RF set-up and the associated DfT architecture

Loop-back configurations have been used extensively in mixed-signal circuits which contain signal paths that perform complementary operations. In theory, the upconversion and the downconversion pair in transceivers serves as a good candidate for a loop-back connection. However, in practice, the time domain duplexing nature of the receive (RX) and the transmit (TX) operations enables many design optimizations, which in turn make the TX-RX loop-back connection infeasible [17]. Typically, the frequency synthesizer is shared between the receiver and the transmitter resulting in a frequency incompatibility when intermediate frequencies (IF) are used [19]. As a further optimization in FM transceivers, the transmit signal is directly imposed on the VCO output, distorting the LO port of the receive mixer [22, 6]. In order to overcome these problems while preserving the advantages of the loop-back configuration, a test set-up based on delay injection into the TX-RX connection and an associated DFT method have been presented in [15]. In this section, we provide an overview of this set-up.

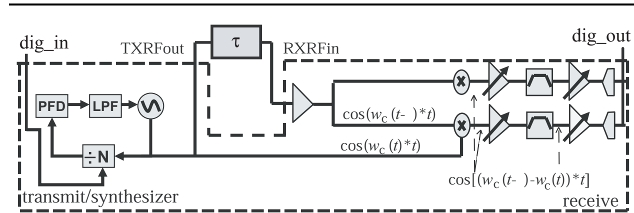

Figure 1. Delayed-RF Set-up

In a frequency shift keying architecture, the frequency of the transmitted signal is varied with respect to the input data. The FSK signal at the transmitter output is given by [19]:

$$x_{FSK}(t) = Acos[w_c t + K \int b(t) * h(t)]$$

where $b(t)$ is the digital base-band signal, w_c is the transmitter VCO frequency, $h(t)$ is the transfer function of the transmit filter, and K is the voltage to frequency conversion gain.

For VCO modulating architectures, connecting the transmitter directly to the receiver results in self-mixing of the signal, thus a pure DC output. One can argue that even this combination may provide a valid path-checking mechanism by measuring the output DC signal. However, DC offsets generated in the path, or any DC coupling after the receive mixer make the application of such testing impossible. While direct loop-back bears little hope for these frequently used transceiver architectures, introducing a delay into the loop-back path together with a simple change to the all-digital control circuit of the synthesizer provide a mechanism to control the frequency of the output signal, thus making measurements feasible, as shown in Figure 1. We call this test set-up the *delayed-RF* set-up. The output signal of a delayed RF path, shown in Figure 1, is given by:

$$x_R(t) = X_{DC} + Acos\{K[h(t) * b(t - \tau) - h(t) * b(t)]t\}$$

For the period of time when $b(t - \tau) \neq b(t)$, the output is sinusoidal with the frequency $K/2\pi$. Similarly for the period of time when $b(t - \tau) = b(t)$, the output is a DC signal. Thus, application of an alternating bit pattern results in a time-varying signal which can be differentiated from DC offsets in the path.

The DFT method proposed in [15] also enables controlling of the transmit-1 to transmit-0 frequency offset by controlling the fractional component of the fractional-N divider

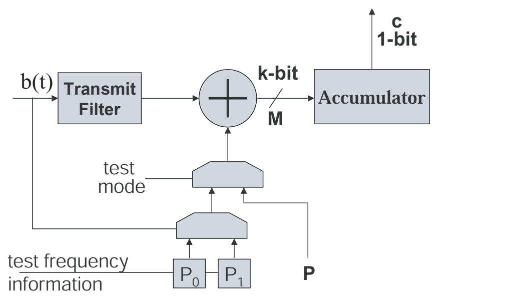

Figure 2. All-digital DFT architecture to control the output signal frequency

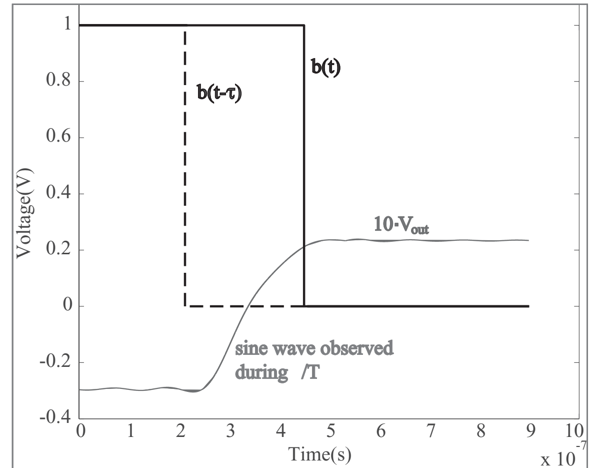

Figure 3. Output waveform with τ delay compared to T signal period

in the test mode. The divide ratio in the PLL path is either N or $N + 1$ depending on the carry that is generated by the overflow of an accumulator. At each cycle, the accumulator adds a number M to the value stored at the previous cycle. The average divide ratio depends on how large M is compared to the accumulator's maximum, 2^k. During one transmit period, the number M is composed of a constant, P, and the digital input data, $b(t)$, resulting in an average PLL divide ratio of $N + (P + b(t))/2^k$. The constant P is used to set the carrier frequency and can be changed only from one transmit period to another in the normal operation mode. Therefore, in the delayed-RF mode, the frequency of the VCO and receive output are:

$$f_o = f_{ref} \cdot (\frac{P + b(t)}{2^k}) \quad \text{and}$$

$$f_R = f_{ref} \cdot (\frac{b(t) - b(t-\tau)}{2^k}) = f_{ref} \cdot (\frac{1}{2^k})$$

As a DFT modification, the number P is changed during the transmit period along with the bit pattern in order to provide a mechanism to control the output frequency. Implementing this capability requires two multiplexers at the input of carrier frequency and two registers to hold the desired values, as shown in Figure 2. As a result, the receive output frequency, f_R, can be controlled by setting P_1 and P_2:

$$f_o = f_{ref} \cdot (\frac{P(t) + b(t)}{2^k}) \quad \text{and} \quad f_R = f_{ref} \cdot (\frac{P_1 - P_0 + 1}{2^k})$$

3. Signature Analysis

In [15], the minimum required delay to enable direct measurement of performance parameters is determined. The minimum delay is the period of the output sine wave or the input bit pattern, whichever is larger. We call this delay *the full swing delay*. In some cases, the full swing delay may be too large, making the hardware implementation of the delay component nontrivial or costly. In order to obviate this burden, shorter delays can be used with the help of signature analysis.

When the injected time delay is less than the full swing delay, the output signal is not a pure sinusoidal. Instead, a time-duplexed combination of a sinusoidal and a DC waveform can be observed at the output, as shown in Figure 3. While this output signal does not enable direct measurement of performance parameters, it can be used to deduce the operational health of the device by comparing it to an expected signature.

The signature that is extracted from the good circuit should not only depict the ideal behavior, but also must incorporate all non-ideal effects expected in an RF circuit, such as noise, non-linearity, offsets, and parametric variations. As a result, the fault-free circuit yields multiple look-alike signatures. The pass/fail criteria based on these multiple acceptable signatures must ensure minimal rate of false alarms while the test development method must ensure detection of target all faults.

Both time domain and frequency domain representations of the output signal can serve as a valid signature for testing. However, the compactness of frequency domain signatures and their robustness to infrequent data failures such as an isolated measurement error at a particular time point, make them a better candidate to obtain low false alarm rates and a high fault coverage.

Using the frequency domain representation, the information about multiple acceptable signatures can be merged in two ways. As all the acceptable signatures have similar shapes (i.e., basic signal components in the frequency spectrum), they can be combined into an *eigensignature*, which can be viewed as a collective average. Eigensignatures have been used extensively in face recognition [9, 23], and in

IDDQ testing [13] where the information content resides in the shape of the signature rather than the absolute values of the datapoints. Using the eigensignature, the pass/fail criterion can be defined based on its correlation with the measured output. As the correlation measure is sensitive to changes in the shape of the signature, it is highly effective for detecting hard faults as well as deviations in noise figure and DC offsets.

Another way of analyzing multiple acceptable signatures is to use an envelope signature, which contains the upper and lower limit of acceptable regions. The pass/fail criterion then is based on the violations of this envelope. This type of signature is highly effective for detecting faults that do not particularly change the overall shape of the frequency domain response, but manifest as strong disturbances at particular frequency locations. For example, the effectiveness of frequency domain envelope signatures in detecting faults that cause harmonic distortion has been demonstrated in [14]. As a result, envelope signatures can be used in detecting parametric faults in gain, offsets, and third order input intercept, all of which cause large single-point deviations in the signature.

In the proposed method, we combine the detection techniques based on both eigensignatures and envelope signatures. Therefore, for a circuit to be classified as *fault-free*, it needs to satisfy both pass criteria based on correlation with the eigensignature and violation of the envelope signature.

3.1. Pass/fail criterion based on eigensignature correlation

Each acceptable signature is highly correlated to the eigensignature as it is derived as a collective average. However, due to random disturbances such as noise, the correlation of each signature displays a certain deviation from the *perfect correlation* value of 1. The correlation between the eigensignature and a particular signature is calculated as follows:

$$\frac{\sum_{i=1}^{N}(S_i-\overline{S})(E_i-\overline{E})}{\sqrt{(\sum_{i=1}^{N}(S_i-\overline{S})^2)\cdot(\sum_{i=1}^{N}(E_i-\overline{E})^2)}}$$

where S is one individual signature of the fault-free or faulty circuit, $\overline{S}$ is its average, E is the eigensignature of the fault-free circuit, $\overline{E}$ is its average, and N is the number of datapoints in the frequency response.

In order to reduce the rate of false alarms, a certain deviation from the ideal correlation value needs to be allowed. Thus, a threshold for alarming a fault based on eigensignature correlation needs to be determined. In statistical analysis, confidence intervals together with a confidence level is used to determine whether a given component is acceptable [2, 11]. In the case of eigensignature correlation, the upperbound of the correlation is 1. The lower bound of the confidence interval can then be determined with respect to the desired confidence level. As an example, a confidence level of 0.99 indicates that 99% of the fault-free chips will be classified as such. Typically in the analog domain, the 3σ cut-off point corresponds to a 0.99 confidence level.

3.2. Pass/fail criterion based on envelope violation

Defining a pass/fail criterion based on envelope violations is trickier due to multiple datapoints and the importance of the amount of violation. Similar to the eigensignature case, we define the envelope signature with respect to a desired confidence level. However, one cannot process each datapoint in the frequency spectrum independently since distinct signatures may violate the envelope at distinct points, resulting in a lower confidence level than targeted. Thus, we determine the envelope in an iterative fashion. We start from the eigensignature and the minimum and maximum bounds as determined by the signature samples. Then, we move the bounds of the envelope signature towards the eigensignature such that the desired confidence level is reached with minimum distance from the eigensignature.

Once the envelope signature is determined, outliers violate this envelope with a certain energy. In order to reduce the false alarm rate, we define a pass/fail criterion based on the overall energy of violation with respect to the fundamental signal energy. The fundamental signal energy is defined as the peak signal energy in the upperbound of the envelope signature at frequencies other than DC. This violation percentage does not directly correspond to the violation energy. However, it takes into account both the number and the strength of the violations. Thus, the violation percentage is calculated as follows:

$$\frac{\sqrt{\sum_{i=1}^{N}[max(S_{f_i}-E_{ub},0)^2+min(S_{f_i}-E_{lb},0)^2]}}{max(E_{ub})}$$

where S_f is the signature of the faulty circuit, E_{ub} is the upperbound of the envelope signature, E_{lb} is the lowerbound of the envelope signature, and N is the number of datapoints in the frequency spectrum.

In this study, we classify a chip as defective if the collective energy of envelope violations exceeds -17dB (2%) with respect to the peak signal energy. This threshold adds an additional margin over the already determined upper and lower bounds of the envelope, thus favoring yield conservatism over detecting soft faults. For tight performance specifications, lower thresholds can be used.

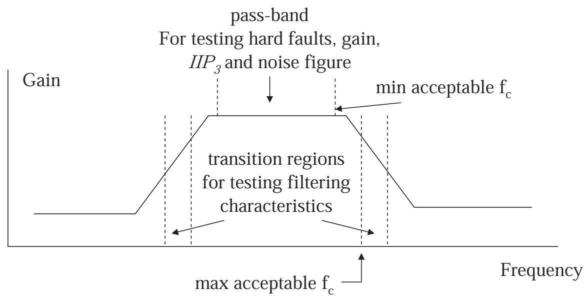

Figure 4. Transfer function of the channel filter and the test regions for hard and soft faults

4. Test development methodology

The goal of the test development methodology is to determine the parameters of the delayed-RF set-up with minimum delay and full coverage of target faults. Three variables define the delayed-RF set-up: the offset between the transmit-0 and transmit-1 frequencies, the injected delay, and the input bit pattern.

The offset between the transmit-0 and transmit-1 frequencies determines the frequency of the sinusoidal waveform at the output of the ADC. The injected delay and the bit pattern determine the time period within which this sinusoidal signal is observed. In the normal mode of operation, the transmit-0 to transmit-1 frequency offset is determined by system specifications. As an example, this offset is 333kHz for the Bluetooth standard [12]. However, the DFT method presented in [15] enables controlling this frequency offset, providing more flexibility in setting the test parameters.

The parameters of the delayed-RF set-up are interrelated; our goal is to determine the set of parameters that enables detection of all target faults with minimum hardware. The cost of the required test hardware, i.e. the delay component, increases linearly with increased delay [10]. Moreover, each distinct delay requires a distinct piece of hardware whereas changing the frequency offset or the bit pattern can be achieved through the digital input. Thus, it is desirable to determine a single delay value for the duration of the test application, while the frequency offset or the bit pattern can be changed during test application.

4.1. Relation among the frequency offset (Δf), the bit pattern ($b(t)$), and the time delay (τ)

As illustrated in Figure 3, the expected signature consists of a DC component and a sinusoidal waveform with frequency Δf. The sinusoidal component is observed during a period when $b(t) \neq b(t-\tau)$. The full swing of this sine wave can be observed uninterruptedly if the bit pattern never overlaps with its delayed version and the time delay can cover at least one full cycle of the sinusoidal waveform. However, as satisfying all of these conditions may result in high required delays, we would like to determine a shorter delay that yields a viable signature.

While there is no tight relation among the test variables, there exist bounds within which the optimal point can be searched. Figure 4 shows the test frequency requirements for various target faults. As the sine wave needs to be observed at the output of the ADC, its frequency needs to be within the pass-band of the channel filter for coverage of performance parameters, such as gain, IIP_3, and noise figure. In order to test the filtering characteristics however, the frequency needs to be set around the dominant poles of the channel filter. Due to these conflicting requirements, there is a need to determine at least three sets of test parameters, one in the pass-band of the channel filter and two in the transitions regions, as shown in Figure 4. These requirements define a certain range to search for the frequency offset (Δf) in each case.

For a given Δf, the full swing delay constitutes an upperbound on the search as there is no incentive to increase the delay beyond this point. As illustrated in Figure 5, smaller delays result in lower peak signal energy. Finally, for very short delays the signature is lost into the noise floor and cannot be distinguished from noise. While some degradation in the SNR can be allowed, the peak signal energy needs to be above the noise level by a certain margin for a viable signature. The degradation in the peak signal energy is mainly due to the inability to observe the waveform continuously. Thus, the minimum time period within which the sine wave needs to be observed can be determined using the desired noise margin:

$$SNR_{full} - SNR_{min} \leq 10 \cdot log(\tau^* \cdot \Delta f)$$

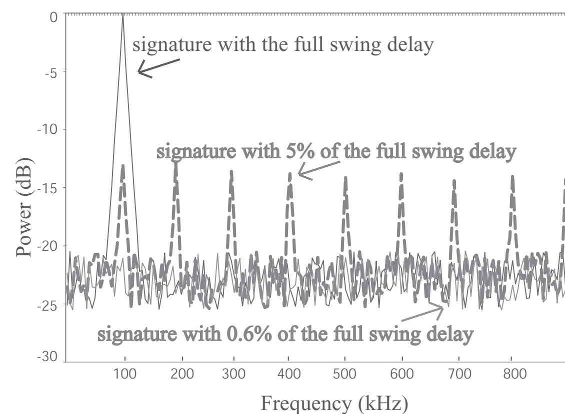

Figure 5. Changes in the peak energy of the signature with respect to the injected delay

where SNR_{full} is the peak signal-to-noise ratio with the full swing delay, SNR_{min} is the minimum required peak signal-to-noise ratio, and τ^* is the time period where the sine wave is observed. Assuming that the bit rate is lower than Δf, τ^* can be replaced with τ in the above inequality and the bit pattern is simply set to (1010...). Figure 5 also shows the signature attained with this minimum delay. In this example, the peak signal-to-noise ratio is 25dB, and a 12dB of minimum SNR is required, resulting in a degradation margin of 13dB. Thus, the minimum delay is 20 times shorter than the full-swing delay. Clearly, this signature represents a highly distorted waveform, which will not be effective in detecting some soft faults, such as errors in IIP_3. As a result, rather than directly resorting to the minimum delay, we use this value as a lowerbound in our search for the optimum test set-up that enables coverage of all target faults.

4.2. Test development algorithm

In the proposed test generation methodology, two variables constitute the search space: the injected delay and the frequency offset. The bit pattern needs to be adjusted such that it never coincides with its delayed version for the duration of the delay.

The boundaries of this two-dimensional search space are determined as explained in Section 4.1. The search variables, Δf and τ, both impact the quality of the signature, thus the detectability of the faults. However, the impact of τ on the peak SNR of the signature is much more dominant than the impact of Δf (A 10% change in τ within the search space changes the peak signal energy roughly 10%, while a similar change in Δf has roughly 1% effect). Moreover since the amount of delay directly impacts the cost of the delay component (coaxial cable or LC tank as used in phase noise measurements [10]), we prioritize reducing the delay over increasing the frequency. We use a nested binary search with the Δf search in the outer loop and the τ search in the inner loop.

Performance parameters that are related to processing of the signal within the pass-band, such as gain, IIP_3, and noise figure, as well as the hard faults need to be tested within the pass-band of the channel filter. Parameters related to the filtering characteristics, such as the cut-off frequency or the attenuation at certain offsets, need to be tested within the transition regions of the filter. Thus, two or three distinct test set-ups are required depending on whether a low-pass or a band-pass filter is used for channel selection. However, since it is desirable to use a single delay component, the searches within the distinct frequency regions are interrelated. In the test development algorithm, we determine a universal delay to be used with all frequency settings through sequential binary searches within the distinct frequency regions. In order to decrease the computation time, the minimum delay determined in one search is used as the lower bound in the next search if it is higher than the calculated lower bound. Moreover, we start the search from the lowest frequency region, where the signal period is higher thus lower bound of the delay search is higher.

List(1) = { $f_{c_{lower}}$ }
List(2) = { G, IIP_3, NF, { Hard Faults} }
List(3) = { $f_{c_{upper}}$ }
$w(1) = \{(1+tol)f_{sb_{lower}}, (1-tol)f_{c_{lower}}\}$
$w(2) = \{(1+tol)f_{c_{lower}}, (1-tol)f_{c_{upper}}\}$
$w(3) = \{(1+tol)f_{c_{upper}}, (1-tol)f_{sp_{upper}}\}$
τ_{min} = calculate $\tau_{lb}((1+tol)f_{sb_{lower}})$
Loop1: For List(1):List(3)
    set(f_{ub}, f_{lb})
    Loop 2: Binary search f
        calculate τ_{ub}
        Loop 3: $\tau_{min_{search}}$ = Binary search τ
    τ_{min} = max(τ_{min}, $\tau_{min_{search}}$)
    $\tau_{lb} = \tau_{min}$

Figure 6. Search algorithm to determine the test parameters

Figure 6 illustrates the test development algorithm. First we determine the upper and lower bounds of the frequency region. The bounds are set from either end of the stop-band region ($f_{sb_{lower}}$, $f_{sb_{upper}}$) and divided into two transition regions and one pass-band region ($[(1+tol)f_{c_{lower}}, (1-tol)f_{c_{upper}}]$). The tolerances on cut-off frequencies and stop-band offset are taken into account and frequency regions with uncertainty are excluded from the search. With a given frequency, the upper and lower bounds on the delay search can be determined as explained in Section 4.1. If the computed lower-bound is lower than the previously determined minimum delay, we take the minimum delay as the lower bound to reduce search time. Target faults are injected into the circuit and fault simulations are conducted taking noise, non-linearity and parametric variations into account. The fault injection and simulation platform is explained in detail in the next section. The complexity of the algorithm depends on the range of the search space and the desired granularity. Assuming that there are N_τ data-points in the delay search space and N_f data points in the frequency search space, the complexity of the algorithm is of $O(log(N_\tau) * log(N_f)) * O(Sim)$ where $O(Sim)$ is the time complexity of fault simulations. With efficient and accurate behavioral simulation methods [18], the time complexity of fault simulations can be reduced considerably.

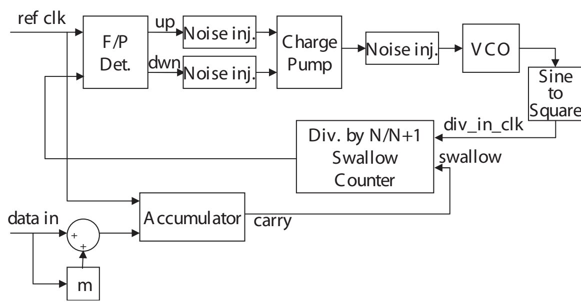

Figure 7. Modified Fractional-N PLL architecture used in the implementation of the transmitter [1]

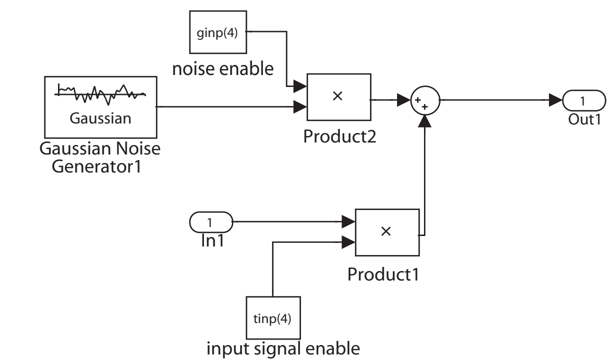

Figure 9. MATLAB noise injection module

5. Experimental results

In this section, we present the test development and fault simulation results on an FM transceiver circuit (Figure 1) and the associated DFT circuit (Figure 2) that are implemented using a MATLAB platform and behavioral models. The system employs a direct conversion transmitter and a low-IF receiver with a band-pass channel filter. The transmit frequency is located around 2.4GHz, and the IF frequency is at 5MHz, with a 2MHz channel bandwidth. The bit rate is at 250kHz. The complete receive path has a minimum sensitivity of -20dBm and a maximum signal input of 20dBm, resulting in a dynamic range of 40dB.

5.1. MATLAB simulation and fault injection platform

The transmitter is implemented based on the fractional-N PLL architecture shown in Figure 7 [1]. The direct upconversion of the input bit pattern is achieved through changing the fractional component of the divide ratio as in the closed-loop VCO modulation architectures [6, 22]. The DFT method [15] is implemented through controlling the base value of the fractional-divide value with respect to the bit pattern.

While this platform enables simulation of the ideal behavior of the transmitter, it does not take non-ideal response into account. Thus, the effects of the non-ideal response need to be injected at the corresponding points of the circuit. Noise injection into each intermediate point of the circuit is achieved through using random signal generators and adders in MATLAB. DC offsets are injected through adding a constant to the signal, while saturation is modeled through adding a simple limiter to each module.

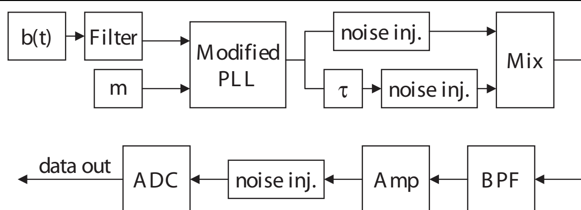

Figure 8. Modified transceiver architecture for fault injection and simulation

Figure 8 shows the complete transceiver architecture including the low-IF receiver. The non-linear behavior of the receive path is modeled at the mixer by adding a third order term such that:

$$V_{out_{mix}} = G_1 \cdot V_{in_{RF}} \cdot V_{in_{RF}} + G_3 \cdot V_{in_{RF}}^3 \cdot V_{in_{RF}}$$

Hard faults in terms of opens are injected by breaking a certain connection and replacing it with a noise source to emulate a real broken wire, as shown in Figure 9. The noise injection module also serves as a noise source while simulating the fault-free behavior. Short circuits are injected by simply connecting two points of the circuit. Soft faults are injected by varying the corresponding parameters of the modules. Each fault injection also requires a new set of Monte-Carlo simulations. In order to reduce the overall computation time, we use a two step approach: We first conduct a coarse Monte-Carlo analysis with limited number of sampling points. If signature of the faulty circuit differs from the signature of the fault-free circuit by a large margin, we declare the fault as detected. However, if the distinction is marginal, we conduct further simulations in order to obtain statistically meaningful data. We declare a fault as *detected* if at least 99% of its signatures fail one of the pass/fail criteria described in Section 3.

5.2. Signature extraction

During the search process, Monte-Carlo simulations are conducted for a given set of τ, Δf, and $b(t)$ to extract the envelope and eigen-signatures. Figure 10 shows the two signatures for the good circuit with $b(t) = (10101...)$, $\Delta f =$

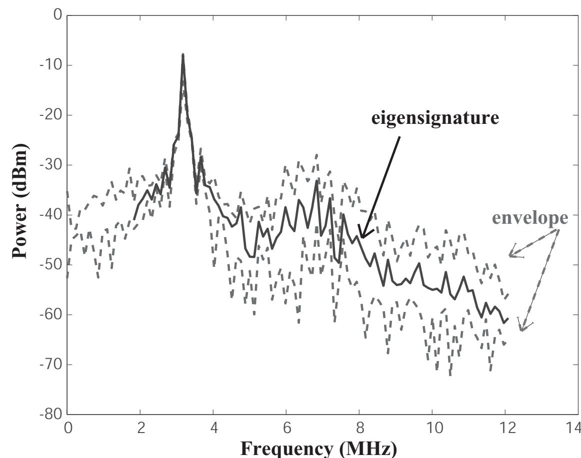

Figure 10. Envelope and eigensignatures extracted from the good circuit with $\tau = 2.5\mu s$ and $\Delta f = 3.2MHz$

$3.2MHz$, and $\tau = 2.5\mu s$, which corresponds to the full-swing delay. The eigensignature is then correlated to each individual fault-free signature to determine the threshold for the pass/fail condition so as to achieve a confidence level of 99% (i.e. 99% of the fault-free eigensignatures are classified as fault-free). The envelope signature is constucted to ensure that at least 99% of fault-free signatures fall within the envelope. The threshold for alarming a fault due to envelope violations is determined with respect to the peak signal energy in the upperbound of the envelope signature. With the above test parameters, the peak signal energy is at 13dBm, thus the threshold for a fault alarm is set to -4dBm, corresponding to 2% of the peak signal energy.

In order to enable an evaluation of the test development algorithm in determining the optimal test parameters, we also define a measure called *fault detectability*. Fault detectability refers to the margin of differentiating the fault response from the good circuit response. In eigensignature analysis, fault detectability is the difference between the determined threshold and the faulty eigensignature correlation. In envelope analysis, the detectability is the difference between the envelope violation energy of the fault response from the set threshold of 2%. In either case, the overall detectability is defied as the minimum of individual fault detectabilities. While we do not use this metric in the test development, we use it to confirm that the variation in fault detectability with respect to the injected delay is monotonic.

5.3. Fault injection and simulations

In order to confirm the detection capability of the delayed-RF set-up and the signature analysis, various hard and soft faults (given in Table 1) are injected into the circuit with the full-swing delay, as it corresponds to the optimal detection point.

Fault	Description
HF1	Up charge pump connection
HF2	Down charge pump connection
HF3	LPF-VCO connection (Synthesizer)
HF4	Receive LO-Mixer connection
HF5	Input Amp-Mixer connection
NF	Noise Figure degraded by 5dB
Offset	50mV DC offset
Gain	3% error
IIP_3	2dB error
fc_{upper}	5% error
fc_{lower}	5% error

Table 1. Definitions of hard and soft faults used in simulations

Table 2 shows the fault simulation results for various target faults to be detected within the pass-band region, with a delay value of $2.5\mu s$ and the frequency offset of $3.2MHz$. The results indicate that using the full delay, all target faults can be detected. Moreover, the detectability of each fault is at least 2%. Our goal is to exploit this margin to reduce the time delay while still attaining full coverage.

5.4. Test generation

It is evident from Figure 10 that the injected delay can be reduced by allowing a degradation in the peak SNR. Requiring a minimum signal observability of 10dB, there is a 15dB margin for SNR degradation. Assuming that all degra-

Circuit	Eigensignature Correlation	Envelope Violation	Thres.	P/F
Good	0.99	0%	> 0.99	P
HF1	-0.04	89%	> 0.99	F
HF2	0.33	89%	> 0.99	F
HF3	-0.04	93%	> 0.99	F
HF4	0.39	89%	> 0.99	F
HF5	-0.07	89%	> 0.99	F
NF	0.97	0.5%	> 0.99	F
Offset	0.99	7%	$< 2\%$	F
Gain	0.99	13%	$< 2\%$	F
IIP_3	0.99	9%	$< 2\%$	F

Table 2. Fault simulation results for target faults to be tested within the pass-band

Parameter	Pass Band	Lower Transition	Upper Transition
τ	$0.26\mu s$		
$b(t)$	101010...		
Δf	3.2MHz	1MHz	11MHz

Table 3. Test parameters determined through the search algorithm

Fault	Criterion	Thresh.	Response	P/F
HF1	Eigensig	> 0.72	0.14	F
HF2	Eigensig	> 0.72	-0.07	F
HF3	Eigensig	> 0.72	0.01	F
HF4	Eigensig	> 0.72	0.01	F
HF5	Eigensig	> 0.72	0.19	F
NF	Eigensig	> 0.72	0.68	F
Offset	Env.	$< 2\%$	23%	F
IIP_3	Env.	$< 2\%$	3%	F
Gain	Env.	$< 2\%$	9%	F
$f_{c_{lower}}$	Env.	$< 2\%$	30%	F
$f_{c_{upper}}$	Env.	$< 2\%$	27%	F

Table 4. Detectability of target faults with the determined test parameters

dation stems from the inability to observe the full sine wave, the delay can be set to $80ns$. However, fault simulations at $\tau = 80ns$ and various values of Δf indicate that particularly soft faults in IIP_3 and gain become undetectable. Thus, there is a need to search for the optimal test parameters.

The search for optimal test parameters within the passband and the two transitions regions is conducted in two ways: First, we determine the minimum time delay, the bit pattern and the transmit-0 to transmit-1 frequency offset through the binary search algorithm described in Section 4.2. In order confirm that we indeed can obtain the optimal test parameters, we divide the search space into 30 identical steps for time delay, and 5 identical steps for the frequency and conduct fault simulations for each combination. Our results indicate that binary search is just as effective in finding the optimal time delay and the frequency offset. The success of the binary search algorithm stems from the fact that the overall fault detectability decreases monotonically with the injected time delay, even though the detectability of individual faults fluctuate by small amounts. The effect of search on frequency has been less clear, as there has been only a small correlation with the exact frequency location and fault detectability as long as the correct frequency region is ensured. Thus, it is beneficial to keep the termination factor for the frequency search much coarser to reduce the overall search time.

Table 3 shows the test parameters that are determined through the proposed test algorithm and confirmed through exhaustive search. Using the proposed method, a tenfold decrease in the required time delay is achieved while conserving full fault coverage. Fault simulation results for all the target faults are given in Table 4. Hard faults have the highest fault detectability margin as most hard faults result in complete malfunction of the device. Of the soft faults, IIP_3 errors have the smallest detectability margin since the third order harmonic has no direct in-band influence for pure sinusoidal waveforms. Despite the inability to directly measure the IIP_3 parameter with this set-up, faults in IIP_3 are still detectable using the proposed methodology. The attained detectability stems from the fact that the output signal has additional components due to either phase reversal or insufficient time delay, effectively generating a multi-tone signal. The low detectability of IIP_3 is mainly due to the small power of the third order response.

The complete test development algorithm including the Monte-Carlo simulations takes roughly 15 hours on a 2.4GHz PC running MATLAB. For coarse Monte-Carlo analysis, we use 50 datapoints whereas for detailed Monte-Carlo analysis, we use 500 datapoints. As the experimental circuit contains the complete transceiver, scalability in terms of the number of modules and single simulation time is not an issue. The algorithm has roughly linear time complexity in the number of faults simulated. Hard fault simulations typically consume less computational time as coarse Monte-Carlo analysis is sufficient to determine their detectability.

6. Conclusion

We have presented a signature-based automatic test development methodology for FM transceivers using the delayed-RF set-up. In order to enable automatic development, we define two kinds of frequency domain signatures and associated pass/fail criteria: eigensignatures and envelope signatures, which are sensitive to various types of hard and soft faults. Based on this signature analysis, we develop a test generation algorithm that aims at reducing the cost of the external test equipment by determining the optimal test parameters that provide full coverage of target faults. Even though the proposoed method does not enable direct measurement of performance parameters, such as gain or third order input intercept, it provides a fast go/no-go decision on the operational health of the transceiver.

In order to demonstrate the proposed methodology, we use a VCO-modulation, low-IF transceiver architecture. We

have developed a fault injection and simulation platform in MATLAB, where non-ideal behavior such as noise, nonlinearity, and parametric variations are incorporated through either dedicated modules, or through modifying the parameters of existing modules. Experimental results show that the proposed methodology not only provides a fast test development venue, but also enables reducing the required time delay by tenfold, thereby reducing the cost of external test equipment.

References

[1] D. Benson. Analog and mixed-signal examples. http://www.mathworks.com/matlabcentral/fileexchange, 2002.

[2] D. Evans. Statistical tolerancing: The state of the art, part II: Methods for estimating moments. *Journal of Quality Technology*, 7(1):1–11, January 1975.

[3] J. Ferrario, R. Wolf, and H. Ding. Moving from mixed-signal to RF test hardware development. In *IEEE International Test Conference*, pages 948–956, Nov 2003.

[4] J. Ferrario, R. Wolf, S. Moss, and M. Slamani. A low-cost test solution for wireless phone RFICs. *IEEE Communications Magazine*, pages 82–88, September 2003.

[5] A. Halder, S. Bhattacharya, and A. Chatterjee. Automatic multitone alternate test generation for RF circuits using behavioral models. In *IEEE International Test Conference*, pages 665–673, Nov 2003.

[6] S. Heinen, S. Beyer, and J. Fenk. A 3.0V 2GHz transmitter IC for digital radio communication with integrated VCOs. In *IEEE International Solid-State Circuits Conference*, pages 146–147, 1995.

[7] M. Heutmaker and D. Le. An architecture for self-test of a wireless communication system using sampled IQ modulation and boundary scan. *IEEE Communications Magazine*, 37(6):98–102, Jun 1999.

[8] M. Jarwala, L. Duy, and M. Heutmaker. End-to-end test strategy for wireless systems. In *IEEE International Test Conference*, pages 940–946, 1995.

[9] J. Ma, N. Ahuja, C. Neti, and A. W. Senior. Recovering frontal-pose image from a single profile image. In *IEEE International Conference on Image Processing*, pages 243–246, September 2000.

[10] H. S. Nam, B. Cuddy, and D. Luecking. A phase noise spectrum test solution for high volume mixed-signal/wireless automatic test equipments. In *IEEE International Test Conference*, pages 957–964, Nov 2001.

[11] S. Nigam and J. Turner. Review of statistical approaches to tolerance analysis. *Computer-Aided Design*, 27(1):6–15, 1995.

[12] L. Nord. Specifications of the Bluetooth system. http://www.bluetooth.org, 2001.

[13] Y. Okuda. Eigen-signatures for regularity-based IDDQ testing. In *IEEE VLSI Test Symposium*, pages 289–294, April 2002.

[14] S. Ozev, I. Bayraktaroglu, and A. Orailoglu. Seamless test of digital components in mixed-signal paths. *IEEE Design & Test of Computers*, 21(1):44–55, January-February 2004.

[15] S. Ozev and C. Olgaard. Wafer-level RF test and DfT for VCO modulating transceiver architecures. In *IEEE VLSI Test Symposium*, April 2004.

[16] S. Ozev, C. Olgaard, and A. Orailoglu. Testability implications in low-cost integrated radio transceivers: a Bluetooth case study. In *IEEE International Test Conference*, pages 965–974, Nov 2001.

[17] S. Ozev, C. Olgaard, and A. Orailoglu. Multi-level testability analysis and solutions for integrated Bluetooth transceivers. *IEEE D&T of Computers*, 19(5):82–91, Sep-Oct 2002.

[18] M. H. Perrott. Fast and accurate behavioral simulation of fractional-N frequency synthesizers and other PLL/DLL circuits. In *ACM Design Automation Conference*, pages 498–503, June 2002.

[19] B. Razavi. *RF Microelectronics*. Prentice-Hall, 1998.

[20] Semiconductor Industry Association. International technology roadmap for semiconductors. http://public.itrs.net/Files/2001ITRS/Test.pdf, 2001.

[21] I. T. Sylla. Building an RF source for low cost testers using an ADPLL coltrolled by Texas Instruments digital signal processor DSP TMS320C5402. In *IEEE International Test Conference*, pages 659–664, Nov 2003.

[22] W. T. Tax and M. A. Copeland. A GMSK modulator using a $\Delta\Sigma$ frequency discriminator-based synthesizer. *IEEE Journal of Solid-State Circuits*, 36(8):1218–1227, Aug 2001.

[23] M. A. Turk and A. Pentland. Face recognition using eigenfaces. In *IEEE Computer Vision and Pattern Recognition*, pages 586–591, June 1991.