RF TESTING ON A MIXED SIGNAL TESTER

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Abstract

In this paper, testing of radio frequency (RF) devices with mixed-signal testers is discussed. General purpose automatic test equipment (ATE) will be used for this. A global positioning system (GPS) device is used as the example to illustrate how to develop the RF test plan with this usage. The test plan developed includes fast, cost-effective and dedicated circuitry.

1. Introduction

2004 continues to be a challenging year for IC testing [1]. As pointed out in ITRS 2003, "Customer requirements for form factor and power consumption are driving a significant increase in design integration levels. Test complexity will increase dramatically with the combination of different classes of circuits on a single die or within a single package. In particular, for SIP (system in package) increased focus on known good die and sub-assembly test will be driven by the cost issue". As for RF chips, the cost of RF testing constitutes a significant portion of the manufacturing cost. It is not surprising since ICs are being designed with faster speed and more complexity, both of which drive the need for more advanced test technology. This tends to drive up the cost of test equipment needed to test these chips and creates a dilemma. On the one hand, there is this increasing need for advanced test technology as test becomes more and more complex and important. On the other hand, there is intense industry pressure to drive down the test cost.

For many ICs used in wireless communication applications, test cost can constitute roughly one third of the final component cost and RF testing makes up the bulk of it. Other factors which contribute toward driving up the cost of RF test are:

- Testers with RF capabilities are significantly more expensive than testers without such capabilities.
- Engineering resources required to develop RF test plans cost much more.

As an example, an RF tester can cost $2 million in tester capital. The engineering costs to develop a test solution for an RF part include engineering time ranging from 2 to 6 months, several thousand dollars in RF circuit board design and 1 or 2 month efforts to fully characterize the RF part and transfer it to manufacturing [2][3][4]. In addition, these costs are non-recurring engineering (NRE) costs because of the uniqueness of each RF part.

In this paper, alternatives to utilizing RF testers are sought by implementing RF test solutions on existing mixed-signal test equipment. In the past, customized RF circuits, including RF sources, receivers and switching circuits, have been tried to allow mixed signal ATE to test RF ICs [5][6]. In this paper, a more universal test structure utilizing RF building blocks is proposed to improve the solution to the uniqueness problem discussed above. The goal is to make the test solution (or at least the RF building blocks) more portable across multiple IC projects and test platforms.

The "on-board design for test" structure we present in this example of RF testing consists of 5 sections: (1) programmable RF synthesizer, (2) RF switching matrix, (3) measurement circuits for gain, power and noise figure, (4) calibration circuits and (5) circuits connecting these RF building block circuits to a general ATE interface. This novel test solution has been applied to several RF products manufactured within IBM. In this paper, we present a GPS device as an example to illustrate such a test system.

2. Mixed-signal tester solution

2.1 Overall RF Test Circuitry

Mixed signal ATE typically contains equipment that can handle digital testing (voltage and current measurements, pattern testing, timing measurements), low frequency analog testing (digitizing, arbitrary waveform generation), interface/support circuitry on the DUT board, and power supplies and DC measurement capabilities for the DUT. We enhance the on-board circuitry to interface with the tester using the test structure shown in figure 1. The main signal path for testing the LNA input (S11 for example) is illustrated in figure 1 with (highlighted) heavy black lines.

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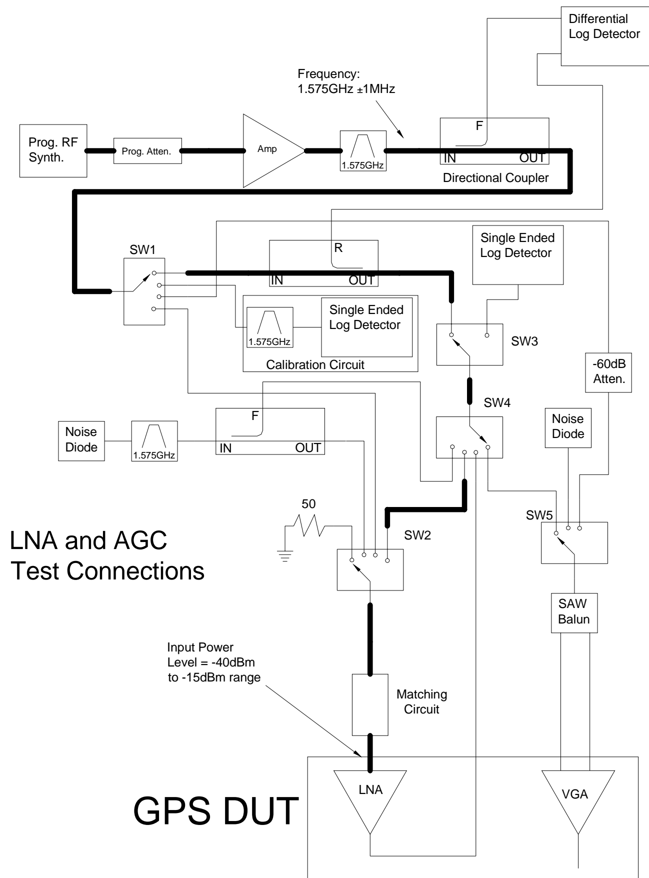


Figure 1 Block Diagram of On-Board Design for Test Circuitry

In this GPS example, all of the RF testing involves the testing of the front end low noise amplifier (LNA) and the following receiver variable gain amplifier (VGA) input circuits. Beyond the VGA, in this example, the signal is down converted internally by the GPS device to frequencies below RF so that testing reduces to digital and mixed signal testing. For the LNA, however, the test specification requires that S11, S22, S21, gain compression and noise figure to be measured at RF frequencies. For the VGA and receiver circuits that follow, the tested measurements are VGA S11 (RF test), automatic gain control (AGC) loop sensitivity (lower frequency digital test), AGC noise sensitivity (lower frequency digital test), AGC image rejection (lower frequency fast Fourier transform (FFT)), AGC gain (lower frequency FFT), and AGC dynamic range (lower frequency digital test). The stimuli for these tests are be either the RF frequency synthesizer outputs or noise signals that have been band-pass filtered. The frequencies of interest in both cases are in the vicinity of 1.575GHz.

2.1.1 Programmable RF Synthesizer

In our implementation, we use an integrated RF synthesizer with integrated VCOs. Such devices are commercially available and they simplify the design of RF sources tremendously. Tuning of the onboard VCOs is required for any application employing such devices. The on-board PLL can typically control the output frequency within a +/-5% variation of the designed center frequency, which is set by an external tuning component. The built in PLL self-tuning algorithm locks the VCO center frequency to the desired output frequency immediately after the device is powered up. This allows the circuit to compensate for the manufacturing tolerances of the external components. The timing reference clock signal for the synthesizer chip is supplied by an externally applied clock, preferably a low phase noise crystal clock or equivalent supplied by the tester. The frequency range of the reference clock is typically up to 30MHz. This application uses a reference clock supplied by a digital channel on the ATE.

Many PLL synthesizers are programmed through a serial port to set internal counter and control registers. The precise output frequency is determined by simple formulae involving the calculation of ratios of the input reference clock, the desired output frequency and the settings of the two internal dividers, N (output) and R (reference). Normally, the values of the N and R dividers are the dependent values once the values of the reference clock and output frequency are known. For our application, the output frequency is nominally 1.575GHz with some tests shifting it by as much as +/-12MHz.

2.1.2 RF Switching Matrix

Referring back to Figure 1, there are 5 RF switches shown on the block diagram. RF switches are readily available in IC form. The insertion loss for these switches is near 1dB at 1.575GHz and can be removed from the measurement error during the calibration process. In addition, compact directional couplers are easily obtained for board mounting. Improved directivity can be obtained by using two directional couplers back-to-back rather than a single bi-directional coupler, although the insertion losses can be greater.

Due to the proliferation of GPS electronics today, inexpensive band-pass filters for GPS frequencies are available in small form factor packages (2x2.5 mm footprint). Manufacturers make various SAW filters that work well in this application. As long as all the RF board traces are laid out using 50 ohm transmission lines, these components work well together.

2.1.3 Measurement Circuits (for gain, power and noise figure)

2.1.3.1 Logarithmic Power Detectors

Single IC logarithmic power detectors are available commercially to convert RF power level to a DC voltage output. There are single ended detectors that measure absolute power of the input signal as well as differential detectors that measure the power ratio between two RF input signals. The differential detectors are very useful for measuring S parameters. Single ended devices are useful for measuring noise figure.

For this project, we employ both types of detectors. The differential detectors are used for the S parameter measurements. This detector is capable of measuring the gain and phase ratios between two input signals up to 2.7GHz, which is suitable for many wireless communications applications. The acceptable input RF signal power levels can be as low as -60dBm and as high as 0dBm. Although the input signals can vary in power level over 60dB, the two input signals cannot vary from each other by more than +/-30dB.

For our GPS application, referring to the block diagram in Figure 1, the differential detector is shown in the upper right corner. Two directional couplers direct the signals to be measured by this detector. It then becomes a simple matter for the ATE to measure the voltage output from the detector to determine the ratio of the two input signals.

A logarithmic power detector measures all of the input power being applied to its RF inputs regardless of input frequency. A band-pass filter must be placed on the input signal path to block out unwanted frequencies in the power measurement. As long as the two directional couplers have good directivity, the accuracy of the measurement can be guaranteed with calibration of the coupling ratios and the sensitivity of the logarithmic power detector.

For our LNA noise figure measurements, we measure only the output of the LNA with a single channel logarithmic detector. The specification for this device is similar to that of the differential detector described earlier, with a frequency range up to 2.5GHz and an input signal power level between 0dBm and -70dBm. The sensitivity of the output voltage to input power is varies with frequency and so we use the device over a narrow band of frequencies for which it is calibrated.

As in the differential log detector case, a band-pass filter is placed on the signal path prior to the input connection of the log detector so that the output voltage will not include measurements of frequencies outside the GPS frequency range of interest.

2.1.3.2 Noise Figure Circuits

Noise figure is a sensitive test that requires good calibration and involves measuring very low level signals that are easily corrupted through external RF interference. We designed two competing circuits to allow us the opportunity of selecting the one with better sensitivity and stability in our test environment. Both are presented here.

The first method is called "hot/cold method" that is commonly used in the industry. It involves applying a hot and cold noise signal to the circuit under test [7] [8]. In our case, the noise figure of the LNA inside the DUT is to be measured. Referring to Figure 1, the noise diode is shown midway down the left side of the block diagram. A portion of the circuit is redrawn in figure 2 in a simplified form to show how it operates.

The noise diode is biased with a constant current from a DC source in the tester. The DC voltage at the noise diode cathode is monitored with a voltmeter supplied by the ATE to insure that the diode does not drift with time. Once calibrated, a shift in the measured voltage indicates a loss of calibration.

The diode output passes through a band pass filter to the LNA input. The RF switches and directional couplers on the path are not shown. The output of the LNA is routed to a single ended logarithmic power detector for measurement of the RF output power.

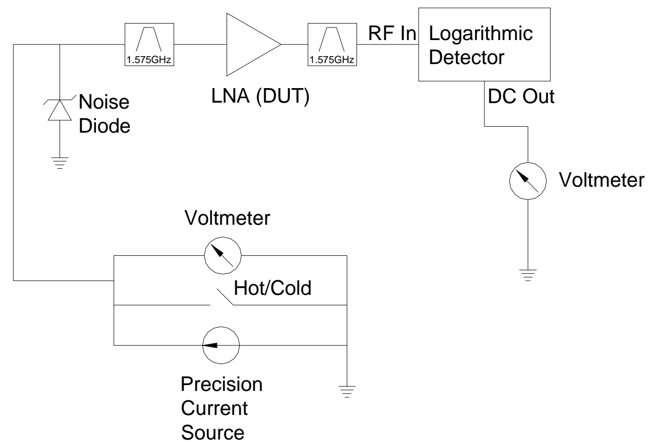


Figure 2: Noise Figure Equivalent Circuit

For the hot/cold method of measuring the LNA noise figure, the current source is switched on and off to turn the noise diode on and off. This is shown schematically in figure 2 as the Hot/Cold switch that is used to shunt the current from the precision current source away from the noise diode. The LNA output measurement made with the noise diode biased on is the "hot" measurement. With the diode current set to 0, the LNA output measurement is the "cold" measurement.

For the noise figure calculations by this method, we employ the Y factor method [8] [9]. The equivalent noise temperature is determined by the hot and cold LNA output power measurements. The equivalent noise temperature is then used in a standard equation to determine the noise figure.

Things to note are:

- The signal levels at the output of the DUT LNA are very low and require amplification to provide enough input power to the logarithmic detector, which must be at least -70dBm.
- The amplifiers used to amplify the DUT LNA output contribute to the overall noise figure and their effect must be removed (through calibration) to obtain the DUT LNA noise figure.

One of the concerns of switching the current source on and off to create the hot and cold measurements is the shifting of the noise diode temperature as it heats up while being biased on and cools off while the bias current is turned off. When turned on, the diode conducts 1/3 ma with a drop of 7.4 volts, dissipating less than 3mW. It is likely that the heating and cooling is negligible when compared with the heating and cooling attributable to ambient air temperature fluctuations at the test floor.

Nonetheless, a second circuit is proposed to keep the diode biased constantly to stabilize the power dissipation. This simplified schematic of the circuit is shown Figure 3.

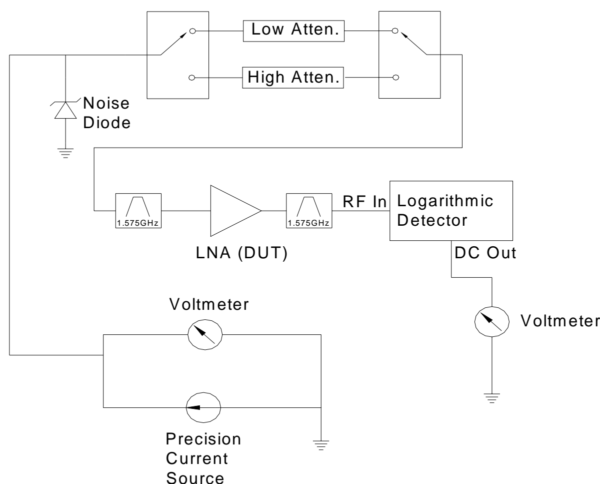


Figure 3: Constant Bias Noise Diode Circuit

In this circuit, the DC source supplies a constant current to the noise diode. The ATE voltmeter monitors the noise diode voltage and assures that the diode has not drifted out of calibration. The output of the noise diode is routed through a switch network that selects either a high attenuation path (for the cold measurement) or a low attenuation path (for the hot measurement). The attenuated signal is then passed through a band-pass filter before being applied to the input of the DUT LNA. The output signal from the DUT LNA is routed on through a band-pass filter to the logarithmic detector for measurement of the signal power in the frequency band of interest.

As in the first method described earlier, the equivalent noise temperature of the noise source through each of the two attenuation paths must be determined by calibration before the noise figure calculation can be performed on the LNA. The noise figure calculation is performed as before using the Y factor method. Since the signals out of the DUT LNA are at very low power levels, additional amplifier stages must be inserted before the logarithmic detector to boost the signal power level. When calibrating the noise figure measurement circuitry, the additional noise from these amplifiers must be compensated to give a true calculation of the noise figure of the DUT LNA alone.

2.1.4 Calibration Circuits

Calibration of the signal sources and detectors used in this design must be performed initially. It is always a good practice to calibrate periodically, in order to make sure that both the calibration monitoring circuits are functioning properly and that the test measurement circuitry is still within calibration limits.

There are two RF sources that are calibrated. One is the programmable RF source and the other is the noise diode. The RF switching matrix is configured to allow connection of these sources to the RF detectors during calibration. If drift is detected, the test program stops testing and alerts the operator that possible board repairs and manual calibration must occur to bring it back into specifications. There are several RF test points located on the test board so that RF bench equipment can be plugged into the board to monitor signal power levels and spectra during the calibration process. There are also software routines written to semi-automate the calibration procedure.

There are two RF logarithmic detectors that need calibration. These also have RF test points available for connecting external equipment. Software has also been written to determine the slope and offset of the output DC voltage from these detectors with varying input power levels at the frequency band of interest.

The result of performing the calibration is to verify that the signal sources and detectors are providing predictable behaviors. In addition, there are several switches, directional couplers, amplifiers, filters and programmable attenuators that are part of the support circuitry that have to operate correctly. The calibration procedure will insure

that these components are functioning correctly within specifications. The programmable nature of the board (through the programmable source, programmable attenuators, etc.) allows some variation in the performance of these support components from board to board. The calibration factors that are measured during the calibration process are used to cancel this variation. The result is that a GPS part will have the same test results regardless of the test board on which it is measured.

2.1.5 Miscellaneous RF Components

As mentioned earlier, there are additional components that are on the RF signal path between the stimulus, the DUT, and the detectors. Figure 1 shows some of these circuits. These components are used to allow the same test board to be configured using software to perform different types of RF test. They also are included to condition the RF signal so that it is set to the proper power levels and frequencies for the proper operation of the circuits that follow.

Directional Couplers:

Directional couplers are necessary for the measurement of incident and reflected signals when calculating the S parameter values for the DUT. Bi-directional couplers are available but better directivity can be obtained by using two single directional couplers placed back to back in the circuit path. The penalty is a loss of signal power for each coupler that it passes through but the improved directivity for more accurate signal measurement makes up for this loss.

Programmable attenuators:

Most RF frequency sources do not have controllable output signal power levels. Typically, the output is in the range of -10dBm to 0dBm. In addition, RF connections (SMP connectors), coaxial jumper cables, amplifiers, RF switches and couplers all have variable gains and losses from board to board. By using programmable attenuators, the signal power levels applied to the DUT can be controlled to a much higher degree using software.

Amplifiers:

Most of the components on the RF signal path have losses in signal power associated with them. In addition, the signal power levels required for some of the tests have to be very low levels. Amplifiers are necessary to boost these signals to proper levels for reliable power measurement. Almost all of the amplifiers used in this paper are fixed gain (approx 18dB) amplifiers. In the noise figure detection circuitry, a low noise amplifier is used in the chain to improve the noise figure measurement performance according to Friis's formula [7] [8].

Band-pass Filters:

GPS filters in small form factor footprints are used throughout the board to help isolate successive stages and to block out other signal frequencies that would otherwise interfere with the measurements being made.

Fixed Attenuators:

Like the band-pass filters, small form factor attenuators are available in single dB increments from 0dB to 20dB. They are used to set the RF signal to the proper power level. For example, we use different attenuators for the hot and cold measurement paths in the LNA noise figure measurement. The attenuators also are effective in isolating amplifiers from other components connected to them so that the risk of oscillation will be reduced.

2.1.6 Tester Interface

In order to port the RF test solution from one ATE platform to another, IBM has developed a system of interface boards that bridge the uniqueness of various testers. An inner common design RF board surrounded by an outer unique "patch" board is employed. The patch board contains the connections to the ATE using the form factor dictated by the ATE.

The RF DUT test board (inner board) contains the test socket and test circuits. It's shape is not dictated by the ATE and so it is designed to mate only with the outer boards. Its circuits are designed specifically for each RF product and independently of the tester platform. The outer board and inner board are connected together by several high-density, controlled impedance ribbon cables. The key benefit of doing this is that it allows RF development on one specific model of tester with manufacturing production occurring on another model without redesign. This opens up the number of test houses available to perform testing for this product. This technique is currently in use within IBM and works very well.

Using a third-party tester as an example, Figure 4 shows the "Outer-board/ Inner board" arrangement:

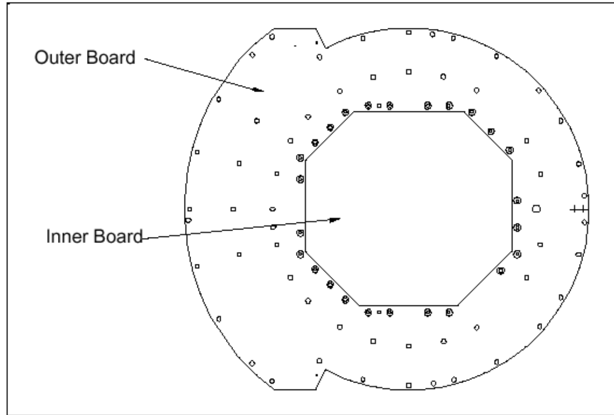
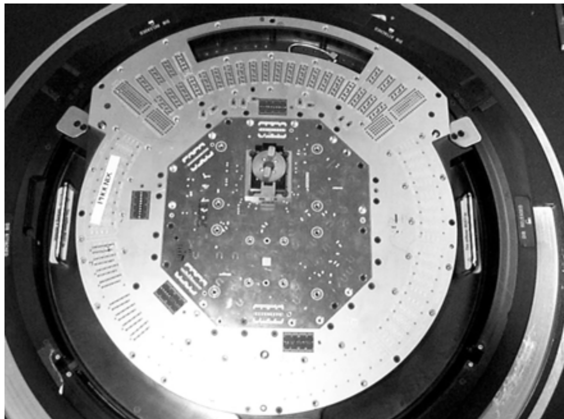


Figure 4: Universal Test Board and Daughter Board

A photograph of such a test board is shown in Figure 5. The product is currently in volume production within IBM.



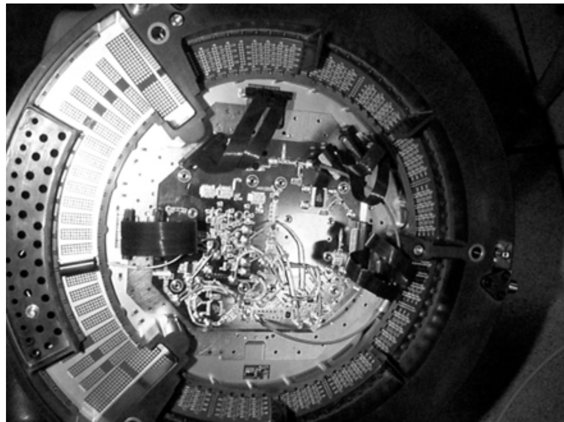


Figure 5: Pictures of DUT Test Board (viewed from top and bottom)

3. Test improvements:

The common building block approach for on-board design for test has been tried on more than one test project at IBM. A library of RF building block circuits is being built over time and proven out. Reuse of circuits that work well allows new projects to pick up the design with reduced development time and cost of implementation. In addition, for those tests where RF measurements are implemented with software algorithms, such as discrete Fourier transform (DFT) algorithms, there have been improvement factors of 7 times in test time and factors of 2 times in standard deviation [6].

Focusing specifically on test time reduction, the use of these building block circuits over the "as-delivered" solution on RF ATE is tabulated in table 1 for typical RF tests:

Parameter	Test time using ATE	Test Time using On-Board DFT
Gain	40ms	10ms
S11	60ms	10ms
S22	60ms	10ms
NF	80ms	20ms
IIP3 85db dynamic range 800Khz spacing	384ms	120ms

Table 1: Test Time Measurement Data

Table 2 shows the benefits of this methodology for a complete suite of tests applied to a particular device type:

Product	Test Time Reduction:
Si bipolar preamp	70%
SiGe integrated transmitter	25%
SiGe integrated receiver	25%
802.11a,b WLAN	40%

Table 2: Test Time Improvements by Product

Data on the improved repeatability of test when utilizing these methods has been obtained and is presented in table 3 for various RF measurements. The ATE standard deviation is the measured standard deviation of testing a

single part repetitively using a conventional ATE outfitted with RF measurement capability. The on-board DFT column shows the standard deviation obtained on the same part utilizing a similar ATE without the RF measurement capability but employing the on-board design for test methods of this paper. In all cases, improvements were observed.

Parameter	ATE standard deviation	On-Board DFT Standards deviation
Gain	0.010db	0.0038db
S11	0.031db	0.0066db
S22	0.031db	0.0062db
NF	0.084db	0.0160db
IIP3	0.280db	0.090db

Table 3: Test Repeatability Data

4. Limitations of this method:

There are some negative impacts of using this methodology over the conventional RF ATE solution. These negative impacts do not erase the gains made by employing this methodology but should be listed for completeness to show a truer picture.

The DUT interface board is considerably more complex by this technique. Many active and passive RF components must be selected and built into the board. Building a library of known good circuits and their limitations is a requirement for this to succeed. In addition, calibration is no longer the worry of the ATE vendor but must be designed and implemented by the test engineer. Insuring calibration can be as difficult as making the actual test measurement. This work can add significantly to the normal design and development time for a DUT interface board.

In addition, board space is limited by the overall space allowed by the ATE. It has been necessary on occasion to build auxiliary boards to contain circuitry and components that do not fit on the main DUT interface board. Power and cooling restrictions also limit this and novel ways of circumventing these limitations are always being sought.

Although we strive to reuse circuits with a common building block library of parts, the math must be done with every new test project to insure that all signals moving between building blocks are at the correct amplitudes and frequencies for expected operation. Unexpected losses or limited dynamic ranges of parts have caused redesign of test boards to include additional amplifiers or switched paths to accommodate a test that has unique signal parameters. Early on in the development of this methodology, there were multiple design iterations required before the circuitry was “right”. As the library and experience base grew, though, the number of redesigned boards has dropped dramatically.

Maintenance of DUT interface boards requires special test and diagnostic software. Under a conventional model, the ATE vendor supplies a maintenance contract that insures calibration and correct operation of the ATE. The DUT interface boards are typically simple in nature containing no active components and including some power and switching circuits. With the on-board design for test methodology, the complexity of the circuitry has increased to the point where the ATE maintenance and calibration procedures are no longer sufficient to include the DUT interface board. The most noticeable impact of utilizing this method is that more spare boards need to be built and calibrated since the turnaround time for such activities is longer.

5. Conclusions:

In this paper, we have discussed the implementation of RF test on a mixed signal tester. By putting various RF source and measurement circuits on the DUT test board, we have been able to build a mixed signal tester solution for RF products. And by proposing a universal test structure utilizing RF building blocks described in this paper, we are able to reduce the development effort in designing RF DIB circuitry. This methodology also has been successfully applied to several other RF projects within IBM Microelectronics. The GPS device is used in this paper as one of the examples to illustrate the success of this methodology.

Ongoing improvements in the test time have been identified by employing hardware DSP accelerator circuitry on the inner board electronics. In addition, the RF source and measurement capability is being expanded to allow multi-tone testing of RF products [6].

Acknowledgment:

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Ray Dicceco and Pat O'Brien were key to writing test software for developing this method. Annette Kalinoski was able to supply the necessary hardware to make this project a success.

References:

[1] International Technology Roadmap for Semiconductors: Executive Summary, ITRS, 2003

[2] Deshaves, "Cost of Test Reduction", Proceedings International Test Conference, Washington D.C., Oct. 1998.

[3] M. Soma, "Challenges and approaches in mixed signal RF testing", 10th Annual IEEE International ASIC conference, Portland, Oregon, Sept. 1997.

[4] M. Awad, and J. Li,"Reducing RF Parameter Tests for Cost Reduction: Device Modeling, Hypothesis Testing and Experiment Verification", the 53rd Electronic Components and Technology Conference, May 2003.

[5] J. Ferrario, R. Wolf and S. Moss, "Architecting Millisecond Test Solutions for Wireless Phone RFIC's", Proceedings International Test Conference, Washington D.C., Oct. 2002.

[6] J. Bhagat, J. Ferrario, R. Wolf, and M. Slamani, "Challenges of incorporating an RF test system on a board", 3rd workshop on test of wireless circuits and systems, 2004

[7] Behzad Razavi, "RF Microelectronics", Prentice Hall, 1998

[8] D. M. Pozar, "Microwave Engineering", John&Wiley, 2004.

[9] Fundamentals of RF and Microwave: Noise Figure Measurement, Application Note 57-1, Hewlett Packard, 1983.