I/O Self-Leakage Test

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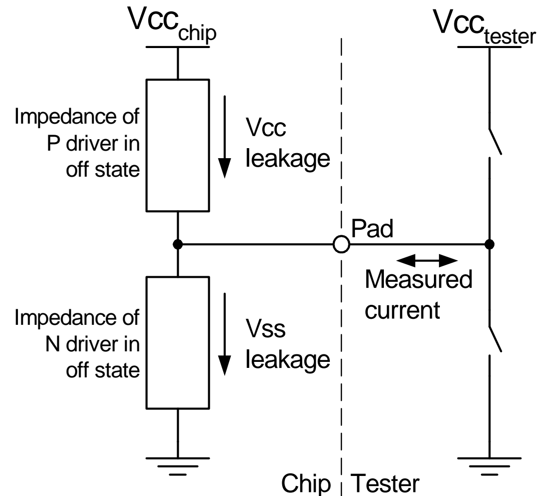
Abstract

This paper presents the implementation of the Self-Leakage Test, a new approach for unconnected I/O leakage testing. It provides a path for leakage current through the on-chip leakers and uses the voltage drop at the pad to detect a pass/fail condition. A detailed methodology for defining the self-leakage test specifications has been developed. Preliminary silicon data shows that self-leakage test methodology provide a viable method for high-volume monitoring of I/O leakage at minimal on-die DFT (Design-For-Test) overhead.

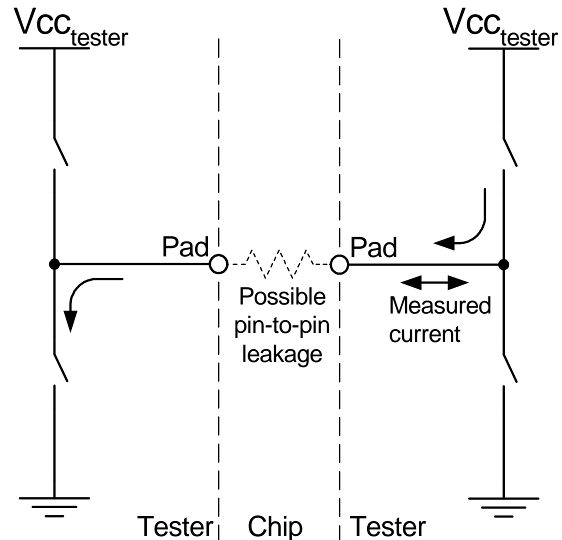
1. Introduction

Manufacturing process technology scaling has led to higher leakage for the digital and analog circuits. Higher than expected leakage at the IO pads can cause logic functionality and bus speed problems. It is also indicative of higher process defect density. For these two reasons, IO leakage testing continues to be an important parametric test and an indicator of the product health. On the other hand, cost pressures have led the industry to move to more cost effective testers by reducing the pin electronics and the number of connected pins between the tester and the product. This method of testing with less connectivity is generally referred to as structural testing.

A sort (wafer level) test for continuity and leakage saves the cost of packaging defective silicon. Traditional leakage tests are performed by connecting each pin to the tester channel and doing a DC measurement. The first step is to pre-condition each pin to tri-state (Fig. 1a). Then, all pins are forced to one of the supply rails and the current sourcing from/sinking to each pad is measured. The second step covers pin-to-pin (P2P) leakage. In this case, all drivers are again tri-stated (Fig. 1b). The neighboring pads are driven to opposite supply voltages and the P2P leakage current is measured through one of the pads. Although simple, the traditional test method requires a connection between the tester and every pin.



a) Single Pin Test



b) Pin-to-Pin Test

Fig. 1 Traditional Leakage Test

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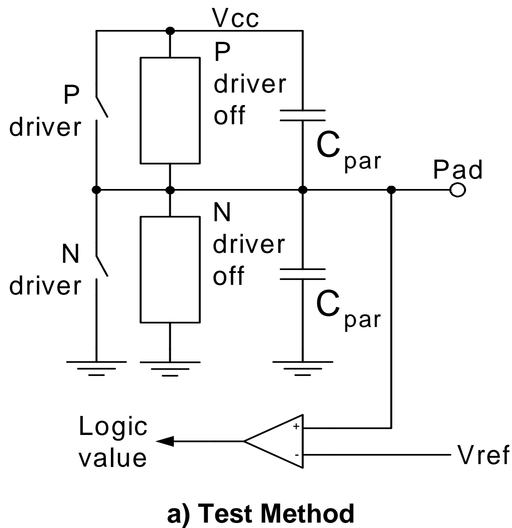
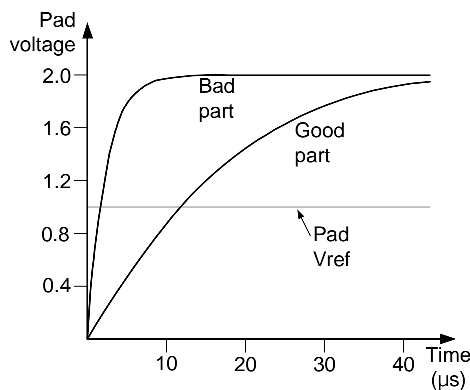
Techniques have been proposed [1, 2] for an AC leakage test that gets around the pin connectivity to the tester by using the JTAG interface. It tests leakage by measuring the time constant of the current discharge thru the pad capacitance (Fig. 2a). The pad is pre-charged through the drivers (switches in the picture) and then tri-stated. Voltage stored in parasitic capacitances at the pad discharges trough the drivers and other leakage sources (Fig. 2b). The driving and sensing of the pad is done through the JTAG tap access, eliminating the need for a tester channel.



a) Test Method



b) Difference between Good and Bad Parts

Fig. 2 AC Leakage methodology

This test has the major disadvantage of relying on the speed of the JTAG interface to separate a good from a bad part. Therefore the discharge time constant of a passing device must be slower than the discharge of a bad device by few JTAG clocks. This means that the test is effective only if the distribution of “good” devices is distinct from and separated by several JTAG clocks from the distribution of “bad” devices. If it is desired to test a continuous distribution for a specific test limit, then the AC leakage test proposed in [1,2] is not adequate.

In this paper we present an alternative DC test approach to unconnected pins that is based on a concept described in [3]. The proposed test adds minimal on-chip DFT circuitry and takes advantage of the JTAG port.

2. Self-Leakage DFT Implementation

Fig. 3 depicts a typical I/O. The driver is a buffer driving the pad, package trace, pin and external load (not shown). The receiver is a comparator with an externally generated reference Vref common to all pads. The Self-Leakage (SL) components $R_{leakp<h,m,l>}$, and $R_{leakn<h,m,l>}$ (leakers), S_P and S_N (switches) represent the added DFT. The leakers are small devices designed with large “ON” resistance in order to form a voltage divider with the equivalent “OFF” resistance of the opposite driver. Variable size of leakers, depicted in Fig. 3 as independent leakers, allow the detection of a wide leakage range. The existing pad input comparator and the Vref control to this comparator are re-used to evaluate pass/fail decision. The added leakers, comprised of small devices, are susceptible to ESD events. Therefore, their placement with respect to the pad and ESD protection circuits is very critical. In this implementation the leakers are connected to the input path between the pad ESD circuits (not shown in Fig. 3) and the input comparator.

In self-leakage test mode, the pre-driver is first configured such that both drivers are off, and one of the two switches, S_P or S_N, is closed. An R_{leakp} or R_{leakn} device is turned on depending on the desired (high, medium, low) leaker resistance for the path to Vcc or GND respectively. If the leaker resistance is equal to the equivalent resistance of the opposite driver (in off state), then the pad voltage will be half way between V_{CC} and Gnd. By comparing the pad voltage with a pre-defined value, one can determine if the leakage through the tested driver is too large.

For example, consider the scenario when S_P is closed and R_{leakph} is turned on. The pad voltage will be determined by the voltage divider formed by R_{leakph} and the N driver. If the N driver is too leaky, the pad voltage will be lower than expected, forcing the comparator to generate logic 0 on “test result”.

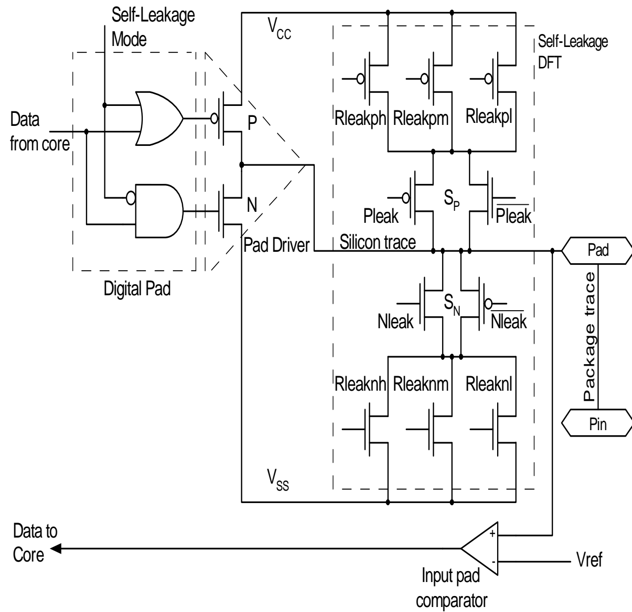


Fig. 3 Self-Leakage DFT integrated into a typical I/O

One challenge with the approach is the fact that the leakage path to the power rail *not* being tested in Fig. 3 is always present, and adds an extra current path to the configuration. Another challenge is the process variation associated with each component (drivers and R_{leak}) across the tested units. These challenges dictate a methodology for selecting the optimum leaker and Vref value as a function of characterized component variations, and pad leakage specification.

The control to the DFT as well as the pass/fail results are interfaced through the JTAG port. Since it takes two JTAG instructions to configure the pad and read back test results, the test time associated with this technique is equivalent to previous unconnected I/O leakage test methods. Since the technique is based on DC measurement, the test limit and accuracy is not dependent on any time constants unlike the AC leakage test methods.

3. Test Limit Generation

The methodology depends on silicon measurements to build characterization curves and determine the optimal leaker and Vref value. A P(N) leaker is selected, and a current excitation I_F is applied to the pad, with the drivers tri-stated. Pad voltage Vpad, is measured as the response. The tested leakage current I_{LN} to Vss and I_{LP} to Vcc can be approximated as follows:

$$I_{LN} \cong \frac{V_{CC}}{R_N} + \frac{I_F}{V_{PAD}} \times V_{CC} \qquad (1)$$

$$I_{LP} \cong \frac{V_{CC}}{R_P} + \frac{I_F}{V_{CC} - V_{PAD}} \times V_{CC} \qquad (2)$$

where R_N and R_P represent the "OFF" resistance for the leakage path to Vss and Vcc respectively, when a voltage level of the opposite rail is applied to the pad in the traditional test method. The SL characterization used to determine the test limits consists of building $I_{LP,N}$ vs. Vpad curves for each leaker on the "good" units. These curves can then be used to determine the expected Vpad value for any specific test limit, and for any leaker. This in turn allows the selection of the optimal leaker. The value of Vref must be set to the minimum Vpad when R_N (R_P) is at the test spec, taking into account the expected DC offset of the comparator.

Fig. 4 illustrates the approach for on-chip pin-to-pin (P2P) testing using SL DFT. If the leaker is not connected, all Vpads are biased similarly. Connecting the high leaker to pad 2 drives the pad voltage closer to Vcc. P2P leakage is detected by comparing Vpad3 with a carefully positioned Vref based on a minimum $RP2P_{leak}$ limit. Although the SL methodology is based on the single-fault assumption, multiple faults are very likely to be detected since defective leakage variations on P and N pad drivers are unlikely to compensate perfectly.

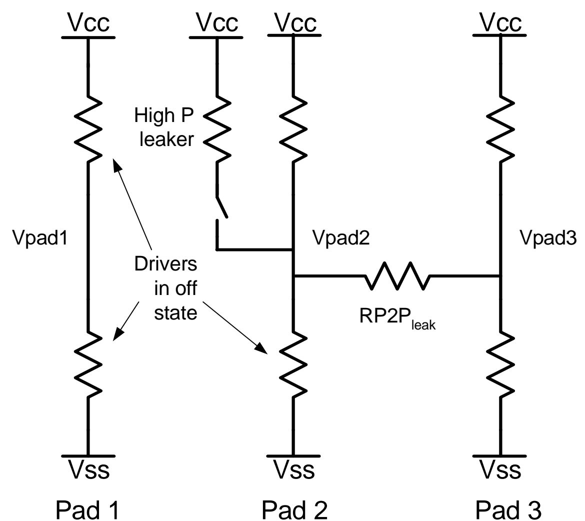


Fig. 4 Self-leakage Approach for on-chip pin-to-pin testing.

4. Validation

No special process compensation circuits were implemented in SL DFT in order to optimize design cost. As a fundamental assumption in the methodology, SL devices are more process-independent than the Device-Under-Test (DUT). Pre-silicon simulations show twice as much variation in the driver leakage than in the leakers due to process and environment variations. The variations affect the test accuracy and are taken into account as inaccuracy guard-bands for generating test limits. In addition, the developed defect test spec methodology accounts for deviation in test setup from traditional functional leakage method and optimal common mode range of the input comparator. Table I shows preliminary silicon validation results across multiple pins and units. Different leakage magnitudes to Vss and Vcc were prototyped by forcing current in or out of the DUT pins. For a given test spec of 60µA to either rail, all pins passed and failed as expected.

5. Conclusions

A new unconnected I/O leakage test method is described in this paper. DFT design and associated test limit derivation method have been presented in detail. The method has the advantage of being DC in nature, unlike the previous methods that are cumbersome to maintain across technology generations. Preliminary silicon results confirm SL can be used for I/O leakage pass/fail test in high-volume monitoring without the need for functional testers, which results in significant test costs reductions.

Table I Preliminary Self-leakage Test results

Leakage tested	Leakage to Vcc Vref=400mV			Leakage to Vss Vref=600mV		
	Min. pin voltage	Max. pin voltage	P/F	Min. pin voltage	Max. pin voltage	P/F
2µA	29mV	40mV	All Pass	962mV	970mV	All Pass
60µA	330mV	379mV	All Pass	637mV	680mV	All Pass
100µA	417mV	477mV	All Fail	519mV	570mV	All Fail
200µA	566mV	662mV	All Fail	455mV	516mV	All Fail
100µA	414mV	476mV	All Fail	554mV	593mV	All Fail
200µA	455mV	542mV	All Fail	493mV	545mV	All Fail

6. Acknowledgements

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7. References

[1] T.R. Arabi *et al*, “A JTAG based AC leakage self-test”, Symposium on VLSI Circuits, pp 205-206, June 2001.

[2] S. Sunter *et al*, “Contactless digital testing of IC pin leakage currents”, Proceedings of the International Test Conference, pp. 204-210, Oct. 2001

[3] T. Frodsham *et al*, “Apparatus for I/O leakage self-test in an integrated circuit”, US patent 6262585, July 2001.