A HIGH-RESOLUTION FLASH TIME-TO-DIGITAL CONVERTER AND CALIBRATION SCHEME

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Abstract

Flash time-to-digital converters (TDCs) are well-suited for use in on-chip timing measurement systems because they can be operated at high speeds, offer low test time, and are relatively easy to integrate. However, clock jitter in modern integrated circuits is often on the same order of magnitude as the temporal resolution of the TDC itself. Therefore, techniques are required to increase the resolution of these devices, while ensuring timing accuracy. This paper presents a high-resolution flash TDC that exploits the random offsets on flip-flops or arbiters to perform time quantization. It also describes a novel technique based on additive temporal noise to accurately calibrate the measurement device. Simulation and experimental results reveal that the latter method can calibrate the high-resolution flash TDC down to 5 ps within reasonable error limits. In addition, accurate timing measurement of jitter below 14 ps has been experimentally validated using a high-resolution flash TDC fabricated in a 0.18-μm CMOS process.

1. Introduction

On-chip measurement of electrical phenomena using custom mixed-signal test cores is an attractive method for overcoming the bandwidth limitations and interconnect timing-related uncertainties common in traditional off-chip test systems [1]. In particular, on-chip timing measurement of clock jitter has become increasingly important as clock frequencies approach 10 GHz [2]. At these speeds, a peak-to-peak jitter of only 10 ps translates to a 10% uncertainty in clock-edge placement. This demonstrates the need for on-chip timing measurement devices that possess resolutions below this level.

Time-to-digital converters (TDCs) have traditionally been used to evaluate timing performance in on-chip test systems [3]. But because these are implemented in the same semiconductor technology as the device-under-test (DUT), the fine temporal resolutions needed in modern applications often require circuits that occupy a large silicon area or consume a great deal of power [4]. In addition, temporal nonlinearity in the TDC caused by process variation must often be corrected with additional complex tuning circuitry. Therefore, a TDC that has high temporal resolution, is small in size, and perhaps exploits the effects of process variation, would be a valuable component in any on-chip test system.

This paper presents a high-resolution flash TDC suitable for clock jitter measurement. Such a TDC traditionally uses flip-flops or arbiters to compare signal phases and relies upon buffer delays to quantize a time interval. However, one way to save silicon area and achieve higher resolution is to remove the delay buffers completely and instead use only flip-flop temporal offsets caused by process variation for time quantization. This type of flash converter, known as a "sampling offset" TDC [5], can be implemented easily in any standard CMOS process and has the potential for very-high-speed operation. Although such a TDC lacks wide dynamic range, it can be used to quantify clock jitter in which the timing uncertainty is a small percentage of the clock period.

Calibration is an important procedure that every measurement instrument must undergo before use. TDC calibration is normally done by exciting the converter with a series of known time intervals and then correlating the digital output with the input each time. However, such a scheme becomes more difficult as the desired resolution falls below 10 ps. This is because the accuracy of on-chip timing generators [often implemented using delay-locked loops (DLLs)] is limited by the jitter and mismatch of the circuitry itself. Conversely, off-chip pulse generators can produce such time intervals accurately, but these may be too costly for a production-test environment.

Since the sampling offset TDC is known to have resolutions which vary from a few picoseconds to tens of picoseconds [6], calibration of this device is extremely challenging. Therefore, to reduce the demands on the timing generation circuitry, a novel calibration technique based on additive temporal noise will be introduced.

This paper is organized as follows: Section 2 presents the necessary background for understanding flash TDCs in general and the sampling offset TDC in particular. Section 3 discusses traditional techniques for calibrating the sampling offset TDC while Section 4 describes a new calibration method involving added temporal noise. Simulation results showing the viability of the proposed technique, as

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well as experimental results obtained using a programmable logic device, are also included in the latter section. Section 5 discusses the design of a custom sampling offset TDC integrated circuit (IC) fabricated in a 0.18-μm CMOS process. Experimental results from calibration of this device are included in addition to jitter measurement results. Conclusions are drawn and future work is discussed in Section 6.

2. Flash Time-to-Digital Converters

Flash TDCs are analogous to flash analog-to-digital converters for voltage amplitude encoding and operate by comparing a signal edge to various reference edges all displaced in time. The elements which compare the input signal to the reference are usually flip-flops or arbiters (note that an arbiter is a circuit that decides which of two input signals arrived first). For simplicity, flip-flops and arbiters will be referred to interchangeably in this paper. The three main types of flash TDC are described next.

2.1. Single Delay Chain

In the single delay chain flash TDC shown in Fig. 1, each buffer produces a delay equal to τ [7]. To ensure that τ is known accurately, the delay chain is often controlled by a DLL [8].

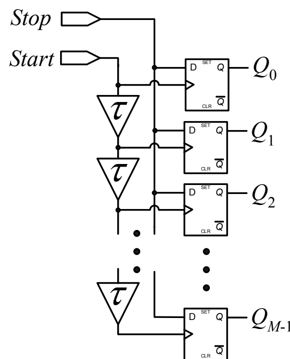

Fig. 1. Delay chain flash converter.

Suppose it is desired to determine the time difference ΔT between the rising edges of pulses P_{start} and P_{stop} using the 8-level delay chain converter in Fig. 2. Each flip-flop compares the displacement in time of the delayed P_{start} to that of P_{stop}. The thermometer-encoded output indicates the value of ΔT, assuming the flip-flops are given sufficient time to resolve. The drawback to this implementation is that the temporal resolution can be no smaller than a single gate delay.

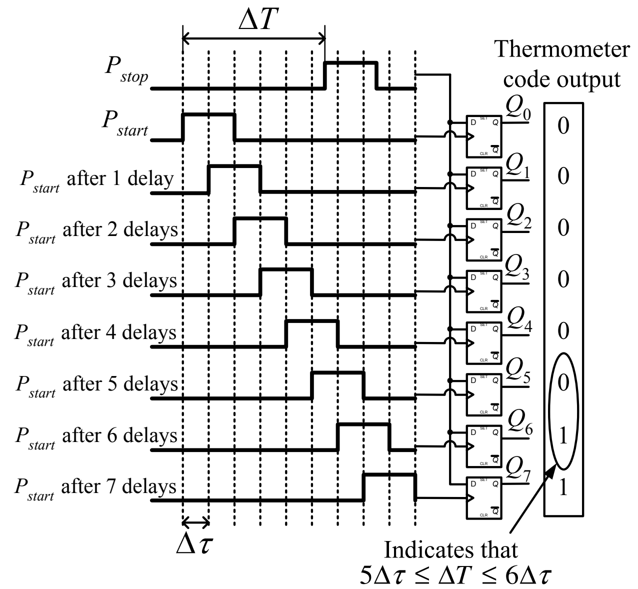

Fig. 2. Operation of an 8-level delay chain flash converter.

2.2. Vernier Delay

To achieve sub-gate time resolution, the flash converter can be constructed with a Vernier delay line as shown in Fig. 3 [8]. This architecture achieves a resolution of $\tau_1 - \tau_2$, where $\tau_1 > \tau_2$.

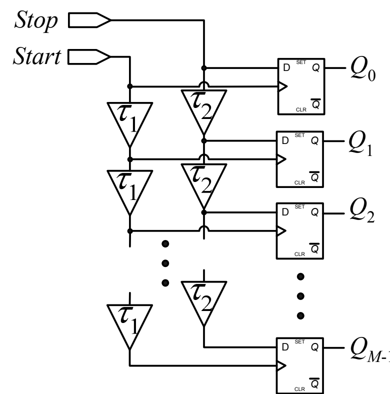

Fig. 3. Vernier delay flash converter.

2.3. Sampling Offset

A flash converter that relies solely on flip-flop transistor mismatch can be used to obtain fine time resolution without separate delay buffers. This type of converter is known as a "sampling offset" TDC (SOTDC) [5] and Fig. 4 shows how it is related to the basic Vernier delay TDC. As displayed in the diagram, the Vernier delay flash converter is first represented as a single delay chain in which each buffer has

delay $\Delta\tau = \tau_1 - \tau_2$. Note that all flip-flops are assumed to be ideal (i.e., they possess no transistor mismatch and are free from noise). An alternative form of the delay chain flash, in which each buffer has a cumulative delay, can then be drawn. Finally, the latter model can be replaced by the SOTDC, in which each ideal flip-flop has been substituted for one with transistor mismatch. Note that the offsets of the non-ideal flip-flops will be random, and not monotonic or multiples of a fundamental offset as Fig. 4 might seem to suggest.

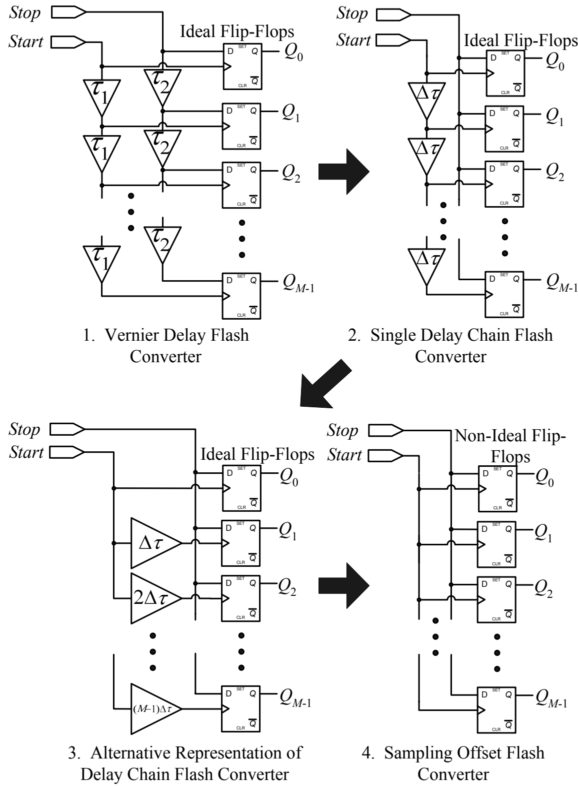

Fig. 4. Relationship of sampling offset flash TDC to basic Vernier delay TDC.

Simulations and experiments conducted in [6] and [9] confirm that mismatches due to process variation can produce time offsets from 30 ps down to 2 ps, depending on the flip-flop architecture and semiconductor technology used. Of course, calibration is required to determine these offsets before the flip-flops can be used for time measurement. Common calibration procedures are described next.

3. Traditional TDC Calibration

The goal of calibration is to determine the time offset t_{os} of each flip-flop or arbiter in the TDC. For purposes of analysis, a flip-flop model is defined first.

3.1. Flip-Flop Model

An ideal rising-edge-triggered flip-flop has $t_{os} = 0$ and is free from noise. A non-ideal flip-flop can be modeled as an ideal flip-flop with $t_{os} \neq 0$ as well as a source of thermal noise as shown in Fig. 5(a) [10]. The noise voltage V_{noise} is assumed to follow a Gaussian distribution with zero mean and standard deviation σ.

An alternative flip-flop model, which is more appropriate in the context of time measurement, is shown in Fig. 5(b). Here, the ideal flip-flop takes a time difference ΔT_{eff} as input and produces a '1' if $\Delta T_{eff} > 0$ and a '0' otherwise. The input ΔT is equal to $t_{clock} - t_{data}$, where t_{clock} and t_{data} are the times of the rising edges of ϕ_{clock} and ϕ_{data} in Fig. 5(a), respectively. In addition, V_{noise} in the original model is expressed as the temporal noise t_{noise}. Assuming a linear relationship between these two variables, t_{noise} follows a Gaussian distribution with zero mean and standard deviation σ_{FF}.

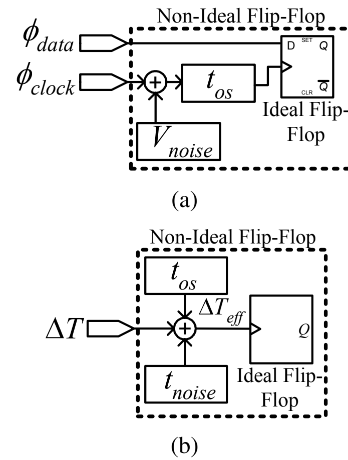

Fig. 5. Flip-flop models. (a) Voltage model (b) Time model

3.2. Indirect Calibration

An indirect calibration technique, involving the use of uncorrelated signals to find the relative offsets of the flip-flops in an SOTDC, was experimentally verified in [6]. An implementation of this is displayed in Fig. 6(a), where ϕ_1 and ϕ_2 are square waves with constant frequencies f_1 and f_2. These are input to two flip-flops having offsets t_{os_1} and t_{os_2}. The relative flip-flop offset is given by $\Delta_{12} = t_{os_1} - t_{os_2}$ and it is assumed that $\Delta_{12} \gg t_{noise}$.

Fig. 6(b) shows how Δ_{12} can be found empirically. Assuming that f_2 is only slightly greater than f_1, ϕ_1 will appear to "move past" ϕ_2 in time. This ensures that the rising edge of ϕ_1 is uniformly distributed over the interval defined by the period of ϕ_2. Therefore, the probability P_{12} that the circled rising edge of ϕ_1 in Fig. 6(b) will land in the shaded

interval Δ_{12} is given by

$$P_{12} = \frac{\Delta_{12}}{1/f_2}. \quad (1)$$

When this occurs, flip-flop output Q_1 in Fig. 6(a) will be '0' while Q_2 will be '1'. Furthermore, measurements with the circled edge of ϕ_1 residing in Δ_{12} will occur with a frequency f_p of

$$f_p = \frac{\Delta_{12}}{1/f_2} f_1 = \Delta_{12} f_1 f_2. \quad (2)$$

Therefore, the periodic output from the AND gate in Fig. 6(a) will have a frequency given by (2). This equation can then be solved for Δ_{12} to obtain the relative time offsets of the flip-flops.

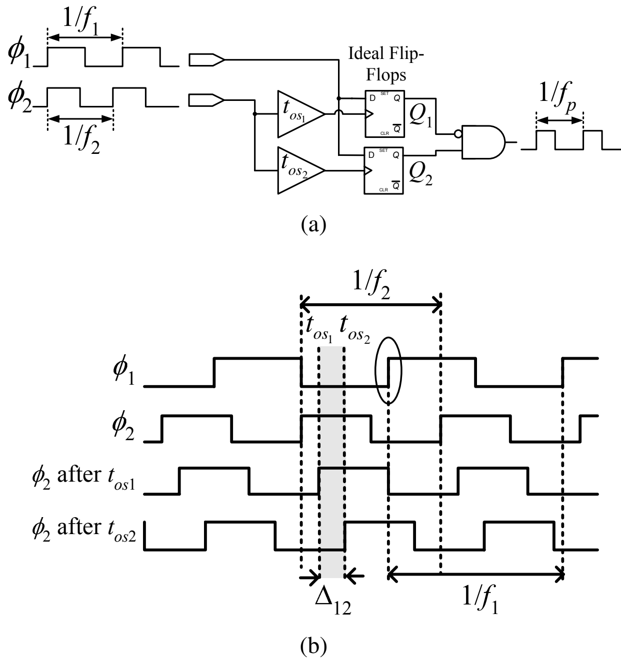

Fig. 6. Indirect calibration of two flip-flops. (a) System used to determine relative flip-flop offset (noise sources are not shown for simplicity) (b) Clocks in the indirect calibration system.

Knowledge of the relative flip-flop offsets can be used to obtain a TDC transfer function like that shown for a 5-level converter in Fig. 7. In this curve, the flip-flop offsets are all expressed relative to the same flip-flop. However, the time from the absolute reference [which is ϕ_2 in Fig. 6(a)] to the first offset cannot be surmised from the indirect calibration. Consequently, if it is desired to measure jitter having a Gaussian distribution using an SOTDC calibrated this way, only the standard deviation (or equivalently, the rms value) of the jitter can be found. Furthermore, no information about the mean value of the jitter (i.e., how far the

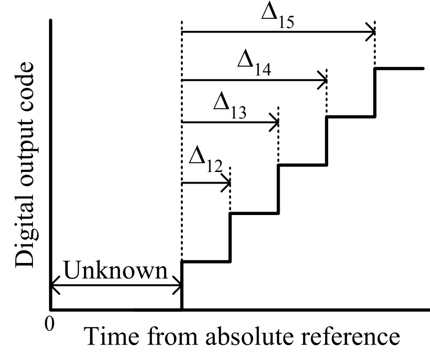

Fig. 7. Transfer curve of a TDC determined using an indirect calibration.

jittery clock deviates, on average, from the reference signal) can be surmised.

However, to acquire both the mean and standard deviation of the timing uncertainty, the absolute values of the offsets must be ascertained. To determine the absolute offsets using the indirect calibration, some information about the offset statistics must be known. Although it could be assumed that the mean offset of a large number of flip-flops constructed on the same die will be zero, this may be invalid unless care is taken in the layout to ensure that all flip-flops experience similar process variation. Since this may be difficult to achieve in practice, the direct calibration technique described next can be used.

3.3. Direct Calibration

In a direct calibration, t_{os} of a single flip-flop is found by setting ΔT to M different values in the range $(-\infty, +\infty)$ and recording the flip-flop output each time as shown in Fig. 8. This process is then repeated N times.

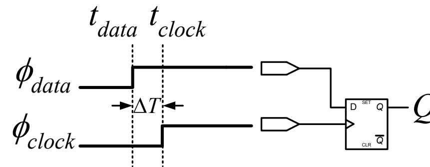

Fig. 8. Direct calibration of a flip-flop.

For simplicity, assume that a flip-flop under calibration has $t_{os} = 0$. The data collected from each of the N trials, as described above, may appear as in Fig. 9. Note that the presence of thermal noise causes the flip-flop output to be different on each trial. By summing the number of times n the output from the flip-flop is '1' for each ΔT, the histogram in Fig. 10 can be plotted. Next, the histogram can be expressed as a cumulative distribution function (cdf) by dividing each n by N and then curve-fitting, as shown in Fig. 11(a). In the

cdf, the probability P of the event $\{\Delta\tau \le \Delta T\}$ is given by

$$P(\Delta\tau \le \Delta T) = \Phi\left[\frac{\Delta T - (-t_{os})}{\sigma_{FF}}\right], \quad (3)$$

where $\Delta\tau$ is a random time and $\Phi(\cdot)$ is the standard Gaussian cdf. Inspection of the cdf reveals that $P(\Delta\tau \le \Delta T = 0) = 0.5$ for a flip-flop having $t_{os} = 0$.

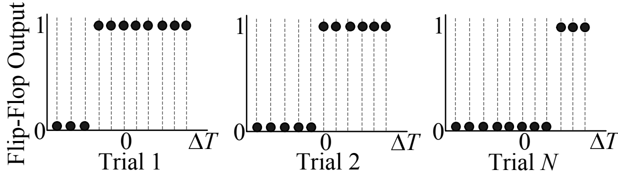

Fig. 9. Results from each trial of flip-flop calibration.

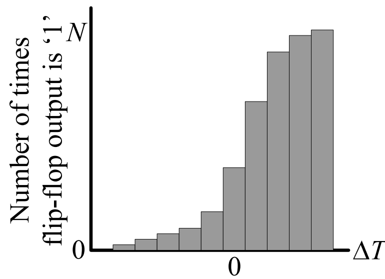

Fig. 10. Histogram result of flip-flop calibration.

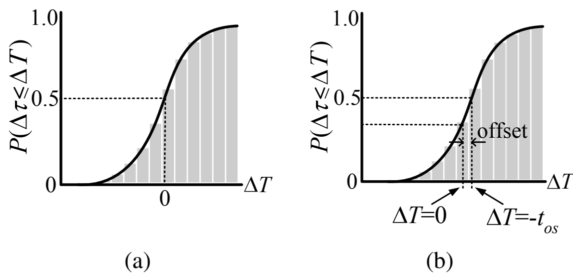

Fig. 11. Calibration cdfs of flip-flops having different offsets. (a) Zero offset (b) Non-zero offset

Now consider the calibration of a flip-flop for which $t_{os} \neq 0$. Fig. 11(b) shows the cdf of such a device and it is apparent that $P(\Delta\tau \le 0) \neq 0.5$.

The main drawback to this calibration method is that to accurately produce the cdf in Fig. 11(b) and obtain t_{os}, ΔT may have to be set to values on the order of a few picoseconds. Such accuracy is difficult to achieve with on-chip signal generators. Furthermore, use of high-resolution off-chip generators may be too impractical or expensive. Therefore, an improved direct calibration method is described next.

4. Improved TDC Calibration Based on Added Noise

Performing a direct calibration on a flip-flop with a t_{os} of a few picoseconds and a σ_{FF} of a few hundred femtoseconds is difficult because ΔT cannot be made small enough to accurately produce a cdf curve. It would be helpful if σ_{FF} was much larger, say in the order of tens or even hundreds of picoseconds, so that points on the cdf could be measured accurately. With this data, t_{os} could be found by curve-fitting.

Fortunately, it is possible to increase σ_{FF} by adding a temporal noise to that already present on the flip-flop inputs. A model for this is shown in Fig. 12, where $t_{noise_{added}}$ is a Gaussian noise source with zero mean and standard deviation σ_{added} and $t_{noise_{FF}}$ is the thermal noise. Assuming the summed random variables are independent, the total noise on the flip-flop will have zero mean and a standard deviation that is the square root of the sum of squares of σ_{added} and σ_{FF}. Furthermore, if $\sigma_{added} \gg \sigma_{FF}$, the total noise standard deviation will be very close to σ_{added}.

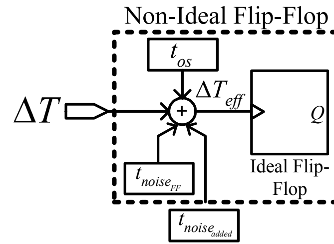

Fig. 12. Flip-flop model with added noise source.

The sum of the time ΔT and the noise $t_{noise_{added}}$ is simply a set of times which follow a Gaussian distribution with mean ΔT and standard deviation σ_{added}. Calibration using these times is performed just like a traditional direct calibration, however the need to set ΔT to very small values is eliminated. To see why, consider the top graph in Fig. 13 where each set of input times is expressed as a probability density function (pdf). As ΔT is increased in discrete steps from $-\infty$ to $+\infty$, a certain number of input times cross the offset threshold of the flip-flop (represented by the dark vertical dashed line in the figure), forcing the output to '1'. If N points are collected from each set of distribution, a histogram can be produced as before. Fitting a Gaussian cdf to the data, the standard deviation of the curve will equal σ_{added}, while the mean will correspond to $-t_{os}$, as shown in the bottom graph in Fig. 13.

4.1. Simulation Results

Simulations were carried out to demonstrate the viability of the proposed calibration technique. The flip-flop model in Fig. 12 was built using MATLAB with $\sigma_{FF} = 0.35$ ps (this was the measured value reported in [6]). The value of σ_{added} was set to 250 ps while ΔT was moved from -400 ps

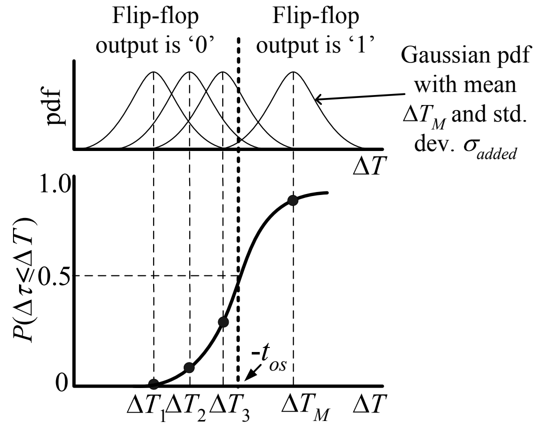

Fig. 13. Direct calibration based on addition of temporal noise.

to +400 ps in steps of 40 ps. Such temporal resolution can be handled with good accuracy by modern pulse generators or on-chip DLLs. Time t_{os} was set to various values in the range (−40 ps,+40 ps) and $N = 10^5$.

Fig.14 shows the result from a single flip-flop calibration. A χ^2 fitting algorithm [11] was used and it is clear that the fitted cdf and the actual flip-flop curve described by (3) nearly coincide at the value of ΔT for which $P = 0.5$.

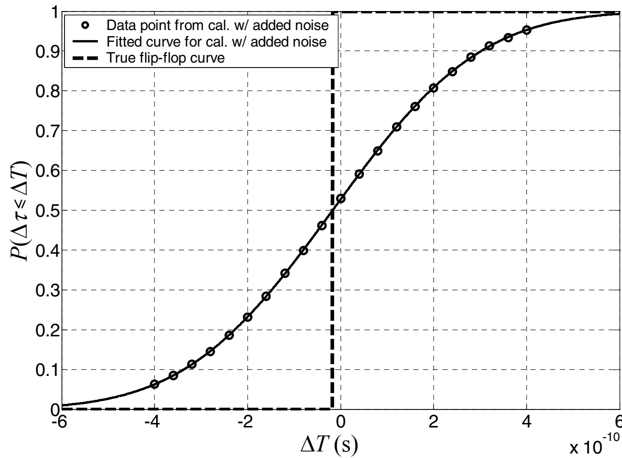

Fig. 14. Simulated calibration result. Actual t_{os} was +17.4 ps while offset from fitted curve was +17.1 ps.

Table 1 compares the actual t_{os} of a flip-flop to that determined through calibration. The results for each calibrated t_{os} are within acceptable error levels. Note that the fitted σ values (not shown) were very close to 250 ps in all cases.

4.1.1. Calibration Time

Calibration of the SOTDC using the method based on added noise depends on the number of values M of ΔT used, the number of trials N run for each of these values, and the rate f at which the trials are executed. Since all levels of the SOTDC can be characterized simultaneously for each ΔT, the calibration time t_{cal} is given by

$$t_{cal} = MN/f. \tag{4}$$

As an example, a calibration with $M = 21$, $N = 10^5$, and $f = 25$ MHz, takes 84.0 ms. Of course, additional time is needed to perform the curve-fitting procedure.

Since the calibration technique is based on a statistical method, decreasing the test time by reducing N will also reduce the accuracy in finding t_{os}. This fact is revealed in Table 2, in which the mean of the absolute value of the percentage errors from the simulated calibration of a flip-flop having $t_{os} = +2.0$ ps is determined for N varying from 10^6 down to 10^3.

Table 1. Comparison of calibrated to actual offset from simulation.

Actual Offset (ps)	Calibrated Offset (ps)	% Error
−35.0	−34.6	−1.1
−2.2	−2.3	4.5
5.0	5.3	6.0
17.4	17.1	−1.7

Table 2. Comparison of mean of absolute value of percentage errors from calibration of a flip-flop for different values of N

N	% Error (Mean of 30 Runs)
10^6	2.83
10^5	12.2
10^4	34.3
10^3	85.2

4.2. Preliminary Experimental Results

To gain preliminary experimental evidence in support of the proposed calibration technique, one level of an SOTDC was synthesized using an Altera EPM7128SLC84-7 complex programmable logic device (CPLD). As shown in the circuit schematic in Fig. 15, the leftmost flip-flop performs the timing measurement by comparing the highly accurate reference ϕ_{clock} with the signal under test ϕ_{data}. The two additional flip-flops attached in series to the main flip-flop are used to reduce the probability that a metastable value is latched by the counter. The 20-bit counter is enabled when the output from the third flip-flop is high.

To perform the direct calibration discussed in Section 3.3, the apparatus shown in Fig. 16(a) was constructed. The

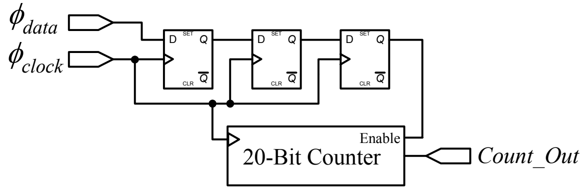

Fig. 15. Single-level SOTDC synthesized on a CPLD.

CPLD containing the synthesized TDC resided on a multi-layer Altera UP1 development board. This was interfaced with an Agilent 81334A dual-channel pulse/pattern generator having a delay resolution of 1 ps, a delay accuracy of ±20 ps, and a total jitter of 2 ps rms [12] (although the latter specification was empirically verified to be lower). The generator was used to produce two calibration clocks and control their phase relationship in order to generate the necessary ΔT.

Calibration involving added noise was performed using the experimental setup in Fig. 16(b). This is similar to that in (a), however an Agilent 33120A function generator, set in noise mode, was connected to the delay control input of the pulse generator. This allowed the phase of the clock signal from one channel to be varied according to the amplitude of a band-limited Gaussian noise signal.

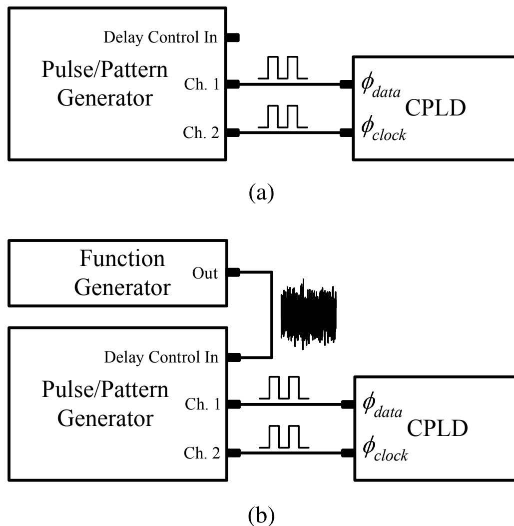

Fig. 16. Experimental setups to perform TDC calibration. (a) Basic direct calibration technique. (b) Calibration technique based on added noise.

Under both calibration techniques, the clock and data frequencies were set to 20 MHz. The number of cycles considered for each value of ΔT was N =1,048,575. In the direct calibration technique, ΔT was adjusted in 1-ps increments in order to find the flip-flop offset. In the technique based on added noise, ΔT was adjusted in increments of 40 ps. Finally, σ_{added} was found to be around 250 ps according to an external oscilloscope.

Results from the calibration techniques are shown in Fig. 17. A t_{os} of -81 ps was found using the basic direct calibration while an offset of -71 ps was determined from the technique based on added noise. This results in an error of -12.3%. The larger error compared to the simulation results is likely due to nonlinearities in the delay control circuitry of the pulse generator. Such nonlinearities can cause the variation in ΔT to be less Gaussian, which in turn can produce a bias error in the results. The fitted value of σ_{added} was 264 ps, which is within the expected range. In addition, the fitted value of σ_{FF} was approximately 0.75 ps.

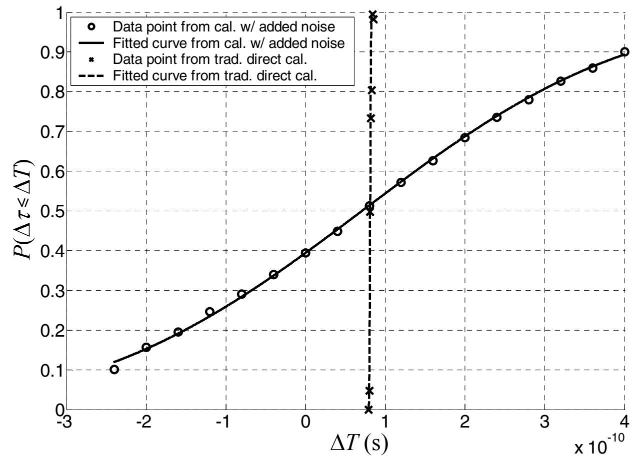

Fig. 17. Experimental results of calibration of a single flip-flop.

5. Custom IC Implementation

To obtain better timing resolution than what can be achieved using a CPLD, a 64-level SOTDC was designed and fabricated in a standard 0.18-μm CMOS process. Each level of the SOTDC was built as shown in Fig. 18 and consists of an arbiter, flip-flops to latch the arbiter output, and a counter. Some additional circuitry to take the contents of the counter off chip was also implemented, but this is not shown for simplicity.

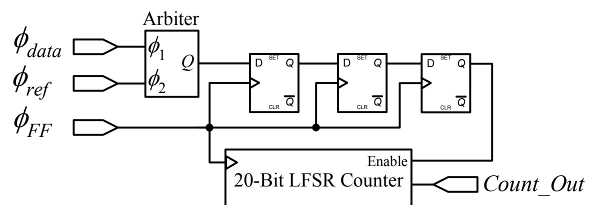

Fig. 18. Single level of custom flash SOTDC.

The arbiter displayed in Fig. 19 is used to compare the rising edge of the highly accurate reference signal ϕ_{ref} to

that of ϕ_{data} [6]. If ϕ_{data} arrives before ϕ_{ref}, positive feedback causes the output Q to go to '1'; otherwise it goes to '0'. Also, this arbiter has the property that its output is not held throughout the entire period of ϕ_{ref}. As a result, the periodic signal ϕ_{FF} in Fig. 18 is required so that the synchronizing flip-flops and counter following the arbiter can successfully latch the data after each rising edge of ϕ_{ref}. Alternatively, ϕ_{FF} could be eliminated and a buffer-delayed ϕ_{ref} used to clock the flip-flops. However, the greater input capacitance seen by ϕ_{ref} compared to ϕ_{data} could skew the timing measurements somewhat.

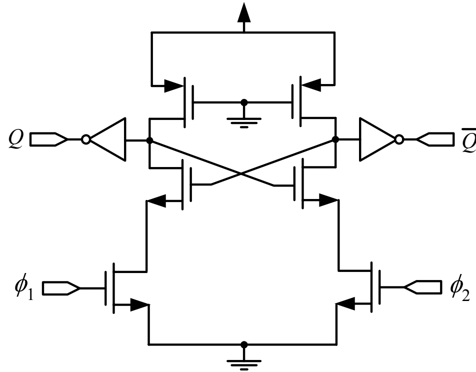

Fig. 19. Arbiter used in SOTDC.

The 20-bit counter is implemented as a two-tap, maximal-length linear feedback shift register (LFSR). Such an architecture employs fewer logic gates and has a simpler routing complexity than a regular ripple-carry counter. In addition, the 20-bit LFSR can be operated at a higher speed than a ripple counter because its critical path consists of only a single XOR gate.

The fabricated SOTDC chip is displayed in Fig. 20. The IC contains two identical sections, each consisting of 32 converter levels. These are distinguished by the dashed outlines in the figure. Since the SOTDC was built using relatively large fully-static CMOS flip-flops, each level occupies an area of approximately 0.024 mm^2. However, in a separate layout of the SOTDC comprised of proprietary standard-cell flip-flops (not shown), this area was reduced to only 0.0032 mm^2.

5.1. Calibration of the Custom IC

The custom IC was mounted on a two-layer printed-circuit board (PCB) and was calibrated using a test apparatus similar to that shown in Fig. 16. A Teradyne A567 mixed-signal production tester was used to assert digital control signals and store output from the IC.

For the calibration based on added noise, ΔT was increased from -100 ps to $+100$ ps in steps of 20 ps. This was done by controlling the phase difference between two clocks running at 25 MHz. The standard deviation of added

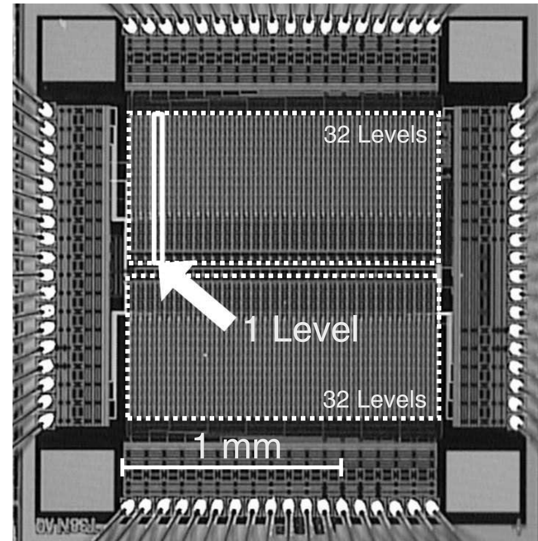

Fig. 20. A 64-level SOTDC implemented in a 0.18-μm CMOS process. Each section consists of 32 levels.

noise was approximately 29.8 ps (as measured using an external oscilloscope) and $N = 10^5$. Both the step size of ΔT and σ_{FF} were reduced compared to the test setup in Section 4.2 because the linear range of the delay control circuitry in the current apparatus was found to be smaller.

Fig. 21 shows the calibration results for one level of the SOTDC. The traditional calibration, in which ΔT was incremented in steps of 5 ps, gives a t_{os} of 9.78 ps while the proposed method produces a t_{os} of 9.80 ps. Best-fit σ using the former method is 9.28 ps and that for the latter is 30.38 ps. Note that the larger σ present in the traditional calibration in the current test setup, compared to the CPLD results, is due to the presence of noise and interference on the PCB. These should be significantly reduced when the IC is tested on a multi-layer board (as in Section 4.2), in which the signal, supply, and ground planes are isolated.

Fig. 22 displays the calibrated offsets for 32 levels in one section of the custom IC. Results from both calibration methods are included and these are ordered from smallest to largest. From the technique based on added noise, the offsets are distributed from about $+3$ ps to $+16$ ps, giving a dynamic range of 13 ps.

The percentage error between each offset, calibrated in the traditional way and using the proposed technique, is shown in Fig. 23. The error on only two offsets exceeds 30% and the average of the absolute value of the percentage errors is 14%. Such an error is reasonable considering the fact that direct measurements using a source without picosecond resolution would produce much higher errors.

It would have been desirable to have the arbiter offsets distributed around zero. This is so that deviations in the edge placement of ϕ_{data} on both sides of the ϕ_{ref} edge could be detected by the SOTDC. Unfortunately, asymmetries in

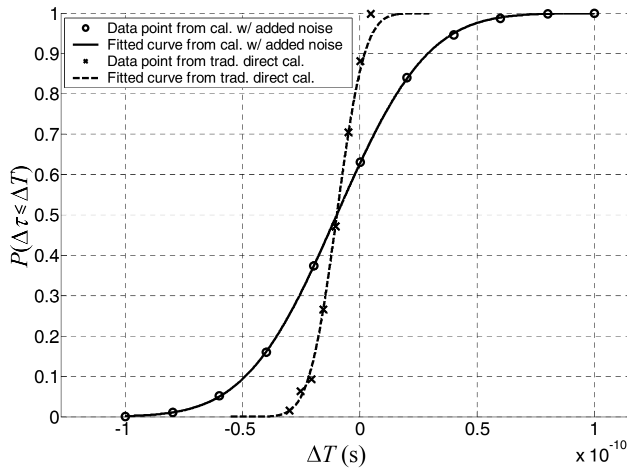

Fig. 21. Calibration of a single level of the custom SOTDC.

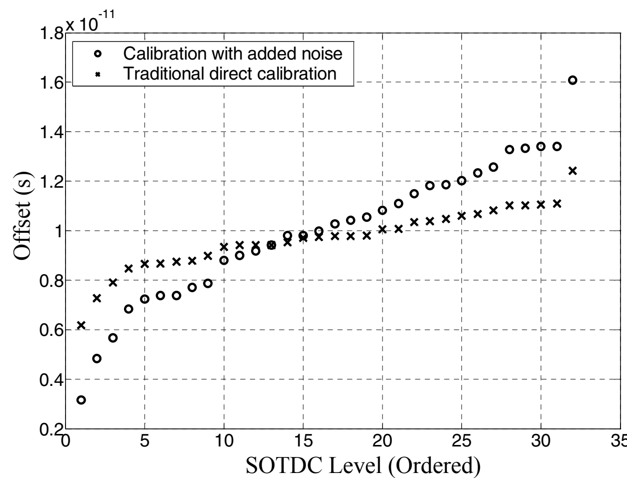

Fig. 22. Ordered offsets from one section of the custom IC determined using traditional and proposed calibration methods.

the original arbiter layout, produced while designing the IC, likely caused all the offsets to favor the same input.

5.2. Jitter Measurement using the Custom IC

The custom SOTDC was used to measure Gaussian jitter. Jitter was produced by varying the phase difference between two 25-MHz clocks according to a Gaussian distribution having a mean of 9.4 ps and a peak-to-peak value of 79.2 ps. These measurements were verified by first connecting the clock generator directly to a LeCroy SDA 6000 serial data analyzer having a jitter noise floor of 1 ps rms [13].

The rms value of the jitter measured by the analyzer was 9.8 ps, however, as discussed in Section 5.1, noise and interference on the PCB adds a jitter component to this. Assuming that this contribution has a mean of zero and adds

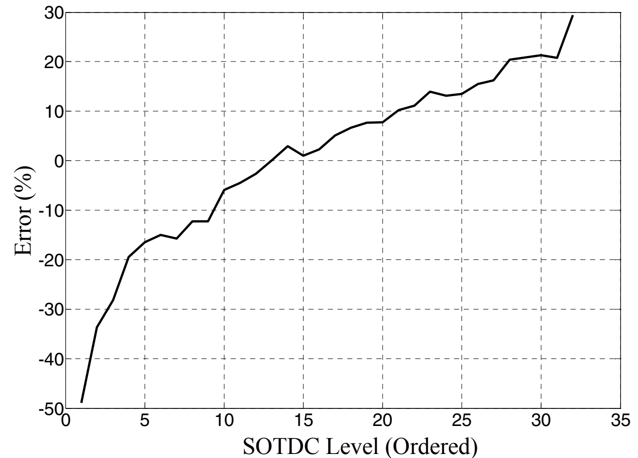

Fig. 23. Percentage error for each offset.

directly to, and is uncorrelated with, the jitter produced by the pulse generator, the jitter under test has an actual σ of $\sqrt{9.8^2+9.28^2} = 13.5$ ps.

Fig. 24 shows the jitter histogram determined using the custom SOTDC. The measured mean of 10^5 samples was 11.0 ps, while the rms value was 14.5 ps. These values are in agreement with those measured by the serial data analyzer.

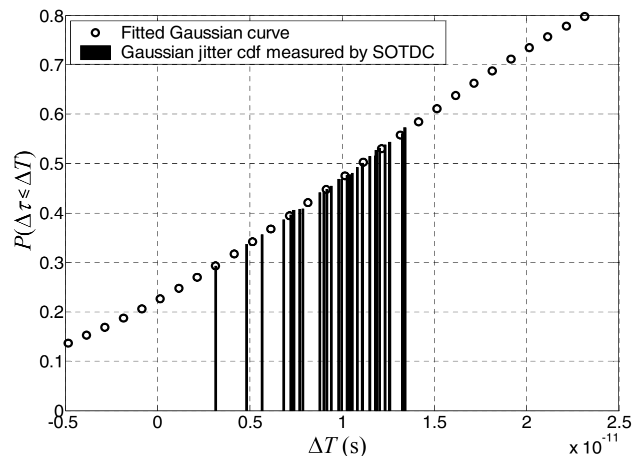

Fig. 24. Gaussian jitter histogram measured using the custom SOTDC. A Gaussian cdf has been fit to the data.

Accurate measurement of the peak-to-peak jitter was not possible because the dynamic range of the SOTDC was limited to only 13 ps. This is the main drawback of the SOTDC architecture in its current form.

5.3. Test Time

Test time for jitter measurement is equal to N/f. Therefore, the measurement carried out in Section 5.2 took only 4.0 ms. This short test time is characteristic of flash TDCs.

6. Conclusions and Future Work

A high-resolution flash TDC for on-chip timing measurement has been presented. A novel technique to calibrate this converter using additive temporal noise has also been described. Simulation results and experimental data obtained from a programmable logic device and custom IC indicate that this method can be used to calibrate the measurement device down to picoseconds. Gaussian jitter measurement was also verified experimentally using a flash SOTDC implemented in a 0.18-μm CMOS process.

6.1. Future Work

The calibration technique based on added noise reduces the resolution requirements on the timing generator needed to calibrate the SOTDC. This feature can be readily applied to production testing of mixed-signal ICs in which the off-chip production tester or on-chip DLL in use cannot produce phase differences with picosecond resolution. To alleviate this shortcoming, two voltage-controlled delay buffers, similar to those used in [8], can be placed on the IC as shown in Fig. 25. With this setup, the delay of clock ϕ_{ref} is modulated according to a voltage signal having Gaussian amplitude statistics V_{noise} while the delay of ϕ_{data} is held constant by dc voltage V_{dc}. As a result, the phase difference between buffer outputs ϕ'_{ref} and ϕ'_{data} can be made to have a Gaussian statistical variation.

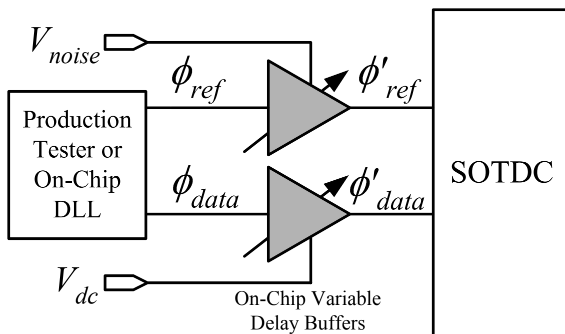

Fig. 25. Proposed hardware implementation of a system to calibrate an SOTDC.

Of course, calibration of the delay buffers is necessary for determining the relationship between the applied control voltage and delay. Although a nonlinear relationship exists between these two variables [8], a region exists where the voltage and delay vary in a linear way. Operation in this region is necessary so that the Gaussian characteristics of the control voltage translate linearly to the resulting delay.

Another issue that must be considered in the proposed system is the additional skew generated by the delay buffers themselves. Since process variation could induce skews in the order of several picoseconds on ϕ'_{ref} and ϕ'_{data}, matching between both buffers is extremely important. Fortunately, the use of larger transistors and careful layout techniques can help ensure a small degree of mismatch. This system has yet to be experimentally verified and is a topic of future work by the authors.

7. Acknowledgements

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